

QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the -48 mA driver and -20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of $200 \mu\text{A}$ at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

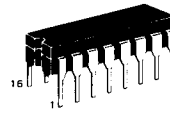
The MC8T26A is identical to the NE8T26A and it operates from a single $+5$ V supply.

- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three State Drivers and Receivers
- Compatible with M6800 Family Microprocessor

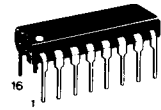
MC8T26A
(MC6880A)

**QUAD THREE-STATE
 BUS TRANSCEIVER**

**MONOLITHIC SCHOTTKY
 INTEGRATED CIRCUITS**

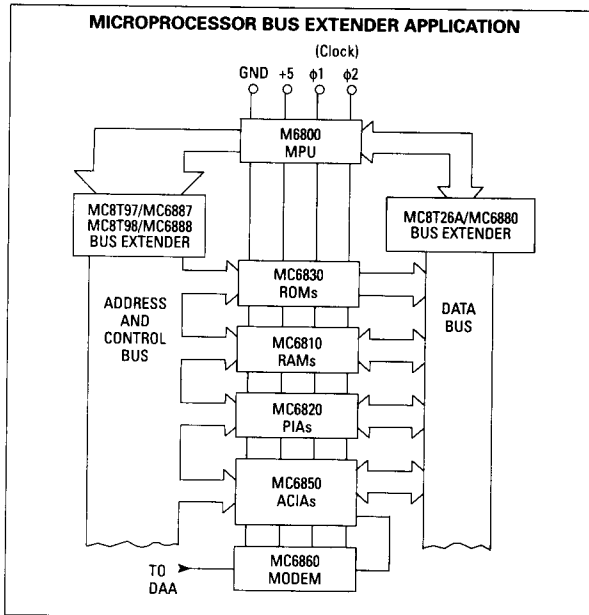


L SUFFIX
 CERAMIC PACKAGE
 CASE 620

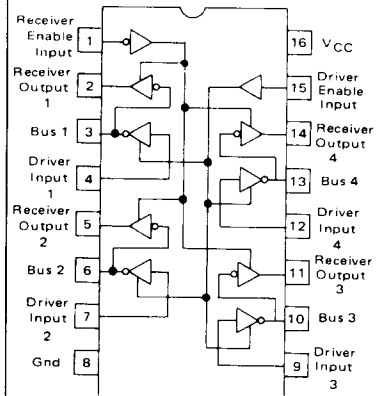


P SUFFIX
 PLASTIC PACKAGE
 CASE 648

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**PIN CONNECTIONS — MC8T26A
 (MC6880A)**



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC8T26AL	MC6880AL	0 to $+75^{\circ}\text{C}$	Ceramic DIP
MC8T26AP	MC6880AP		Plastic DIP

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MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	8.0	Vdc
Input Voltage	V _I	5.5	Vdc
Junction Temperature	T _J		°C
Ceramic Package		175	
Plastic Package		150	
Operating Ambient Temperature Range	T _A	0 to +75	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current – Low Logic State (Receiver Enable Input, V _{IL} (RE) = 0.4 V) (Driver Enable Input, V _{IL} (DE) = 0.4 V) (Driver Input, V _{IL} (D) = 0.4 V) (Bus (Receiver) Input, V _{IL} (B) = 0.4 V)	I _{IL} (RE) I _{IL} (DE) I _{IL} (D) I _{IL} (B)	–	–	-200	μA
Input Disabled Current – Low Logic State (Driver Input, V _{IL} (D) = 0.4 V)	I _{IL} (D) DIS	–	–	-25	μA
Input Current-High Logic State (Receiver Enable Input, V _{IH} (RE) = 5.25 V) (Driver Enable Input, V _{IH} (DE) = 5.25 V) (Driver Input, V _{IH} (D) = 5.25 V) (Receiver Input, V _{IH} (B) = 5.25 V)	I _{IH} (RE) I _{IH} (DE) I _{IH} (D) I _{IH} (B)	–	–	25	μA
Input Voltage – Low Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	V _{IL} (RE) V _{IL} (DE) V _{IL} (D) V _{IL} (B)	–	–	0.85	V
Input Voltage – High Logic State (Receiver Enable Input) (Driver Enable Input) (Driver Input) (Receiver Input)	V _{IH} (RE) V _{IH} (DE) V _{IH} (D) V _{IH} (B)	2.0	–	–	V
Output Voltage – Low Logic State (Bus Driver) Output, I _{OL} (B) = 48 mA) (Receiver Output, I _{OL} (R) = 20 mA)	V _{OL} (B) V _{OL} (R)	–	–	0.5	V
Output Voltage – High Logic State (Bus (Driver) Output, I _{OH} (B) = -10 mA) (Receiver Output, I _{OH} (R) = -2.0 mA) (Receiver Output, I _{OH} (R) = -100 μA, V _{CC} = 5.0 V)	V _{OH} (B) V _{OH} (R)	2.4 2.4 3.5	3.1 3.1 –	–	V
Output Disabled Leakage Current – High Logic State (Bus Driver) Output, V _{OH} (B) = 2.4 V) (Receiver Output, V _{OH} (R) = 2.4 V)	I _{OHL} (B) I _{OHL} (R)	–	–	100	μA
Output Disabled Leakage Current – Low Logic State (Bus Output, V _{OL} (B) = 0.5 V) (Receiver Output, V _{OL} (R) = 0.5 V)	I _{OLL} (B) I _{OLL} (R)	–	–	-100	μA
Input Clamp Voltage (Driver Enable Input I _{ID} (DE) = -12 mA) (Receiver Enable Input I _{IC} (RE) = +12 mA) (Driver Input I _{IC} (D) = -12 mA)	V _{IC} (DE) V _{IC} (RE) V _{IC} (D)	–	–	-1.0 -1.0 -1.0	V
Output Short Circuit Current, V _{CC} = 5.25 V, Note 1 (Bus (Driver) Output) (Receiver Output)	I _{OS} (B) I _{OS} (R)	-50 -30	–	-150 -75	mA
Power Supply Current (V _{CC} = 5.25 V)	I _{CC}	–	–	87	mA

Note 1. Only one output may be short-circuited at a time.

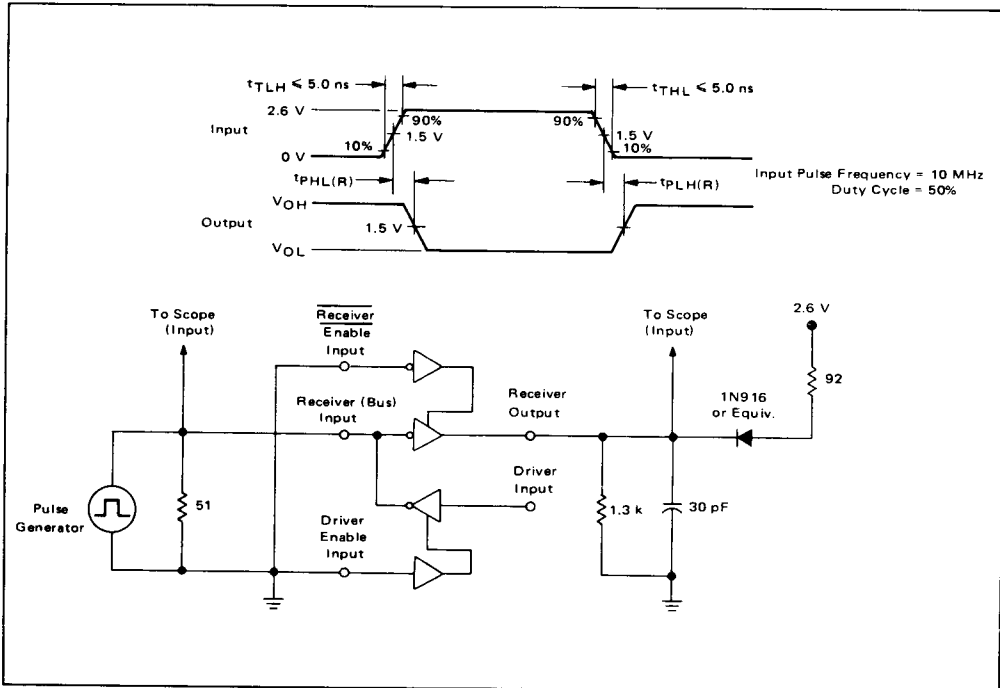
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SWITCHING CHARACTERISTICS (Unless otherwise noted, specifications apply at $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0\text{ V}$)

Characteristic	Symbol	Figure	Min	Max	Unit
Propagation Delay Time from Receiver (Bus) Input to High Logic State Receiver Output	$t_{PLH}(R)$	1	—	14	ns
Propagation Delay Time from Receiver (Bus) Input to Low Logic State Receiver Output	$t_{PHL}(R)$	1	—	14	ns
Propagation Delay Time from Driver Input to High Logic State Driver (Bus) Output	$t_{PLH}(D)$	2	—	14	ns
Propagation Delay Time from Driver Input to Low Logic State Driver (Bus) Output	$t_{PHL}(D)$	2	—	14	ns
Propagation Delay Time from Receiver Enable Input to High Impedance (Open) Logic State Receiver Output	$t_{PLZ}(RE)$	3	—	15	ns
Propagation Delay Time from Receiver Enable Input to Low Logic Level Receiver Output	$t_{PZL}(RE)$	3	—	20	ns
Propagation Delay Time from Driver Enable Input to High Impedance Logic State Driver (Bus) Output	$t_{PLZ}(DE)$	4	—	20	ns
Propagation Delay Time from Driver Enable Input to Low Logic State Driver (Bus) Output	$t_{PZL}(DE)$	4	—	25	ns

FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH}(R)$ AND $t_{PHL}(R)$



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FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$

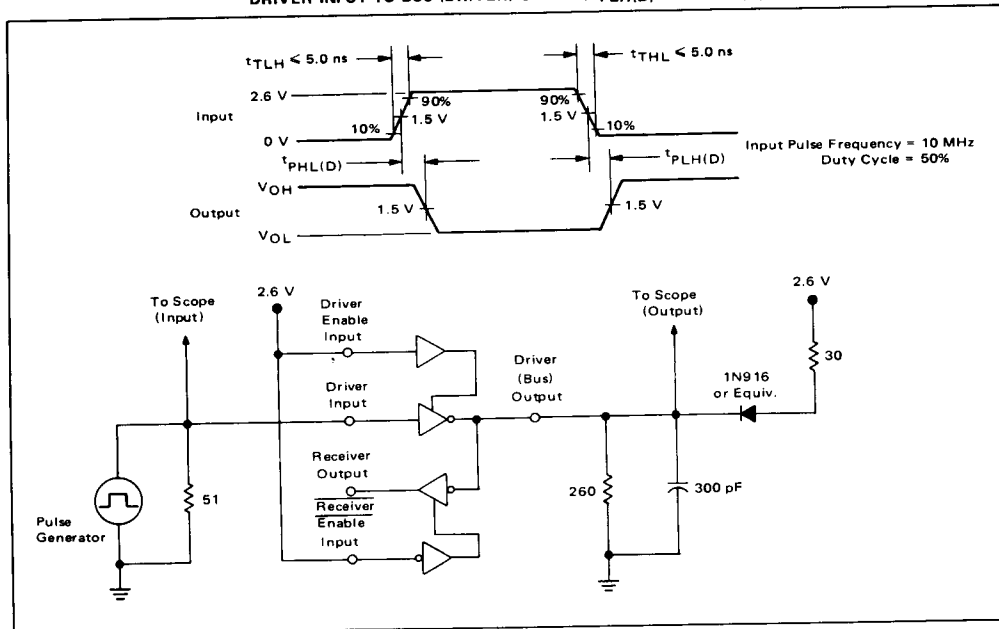
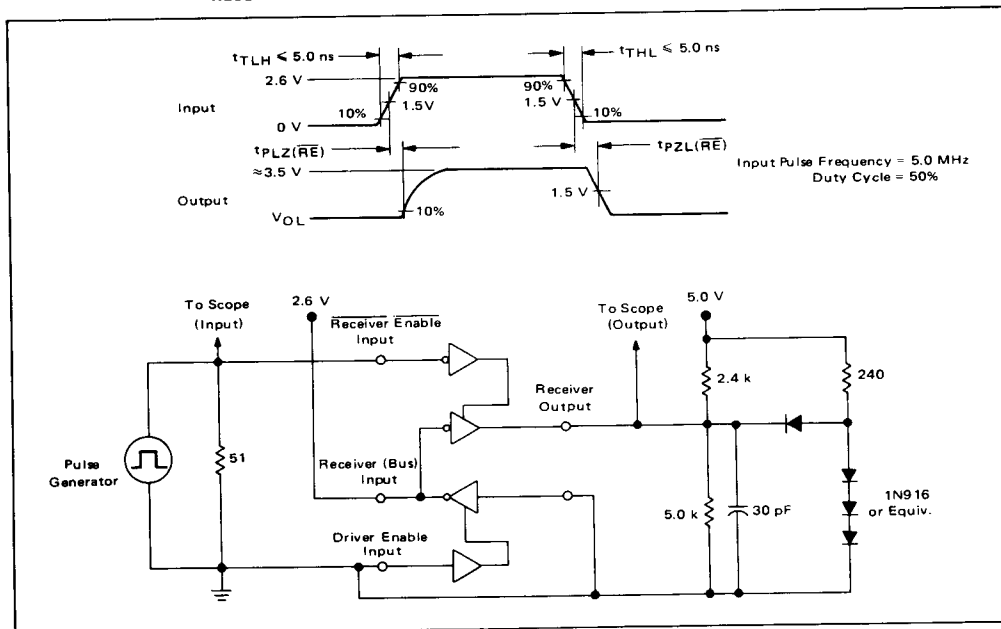


FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$



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FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PLZ(IE)}$

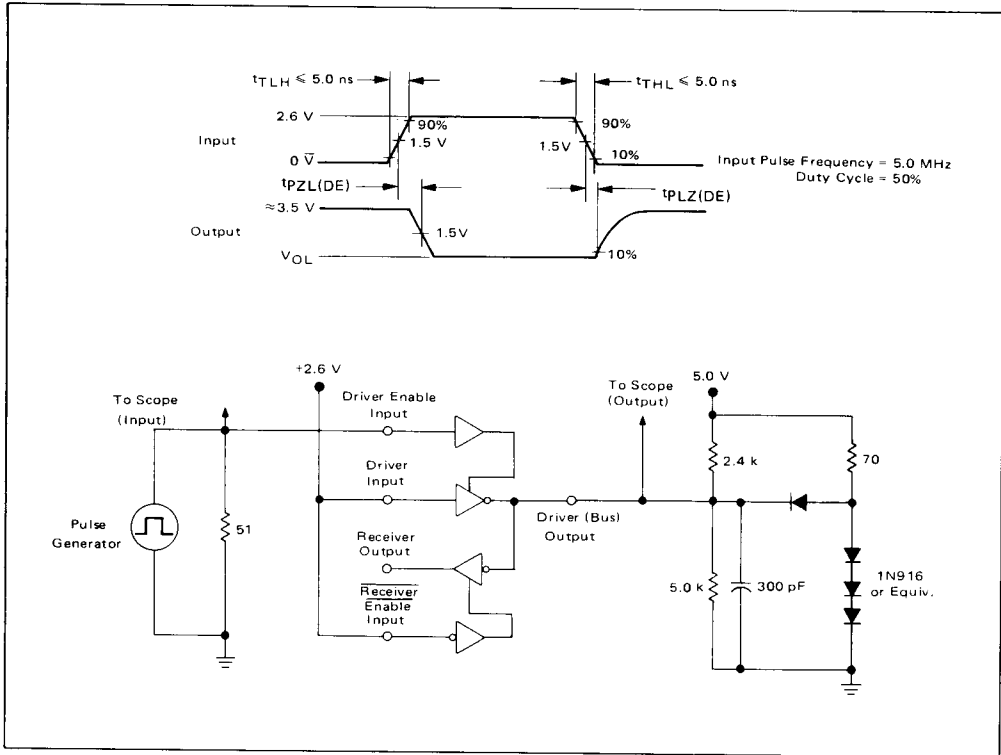


FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS

