FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27205-4E

ASSP Power Supplies

BIPOLAR

Switching Regulator Controller

MB3782

■ DESCRIPTION

The FUJITSU MB3782 is a PWM-type switching regulator controller, designed with open-collector output for connection to external drive transistors and coils, providing a selection of three types of output voltage: step-up, step-down or inverting (inverting output is available on one circuit only).

The MB3782 features identical oscillator output waveforms to enable completely synchronous operation and prevent the occurrence of low-frequency beat between channels.

Also, the MB3782 features low power dissipation (2.1 mA typ) and a built-in standby mode (10 μA), making possible the configuration of a wide variety of high-efficiency, stable power supplies, even with the use of battery power. The MB3782 is an ideal power supply for high-performance portable devices such as video camcorders and cameras.

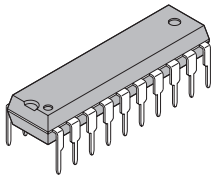
■ FEATURES

- Wide voltage range (3.6 to 18 V)
- Low power dissipation (operating mode: 2.1 mA (typ), standby mode: 10 μA (max)
- Wide range of oscillator frequencies, high-frequency capability (1 to 500 kHz)
- On-chip timer-latch type short detection circuit
- On-chip undervoltage lockout circuit
- On-chip 2.50 V reference voltage circuit (1.25 V output available at R_T pin)
- Dead time adjustment over full duty cycle range
- On-chip standby mode (power on/off function)

(Continued)

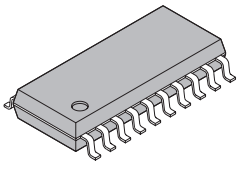
■ PACKAGE

Plastic DIP, 20 pin



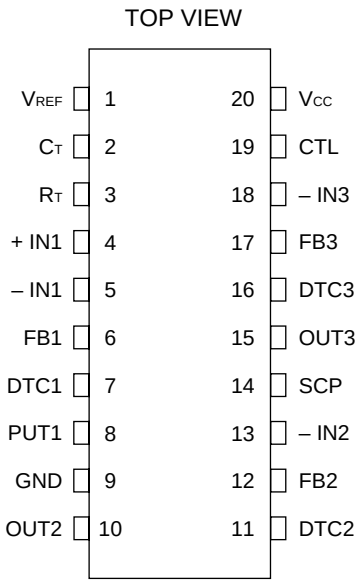
(DIP-20P-M01)

Plastic SOP, 20 pin



(FPT-20P-M01)

■ PIN ASSIGNMENT



(DIP-20P-M01)
(FPT-20P-M01)

■ PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	V_{REF}	O	2.50 V (typ) voltage output: provides load current up to 3 mA, for use as error amplifier reference input and for dead time setting.
2	C_T	—	Oscillator timing capacity connection: should be used in the capacity range 150 to 15000 pF.
3	R_T	—	Oscillator timing resistor connection: should be used in the resistance range 5.1 to 100 kΩ. This pin can also provide output at voltage level $V_{REF}/2$, for use as error amplifier reference input.
4	+IN1	I	Error amplifier 1 non-inverting input pin.
5	–IN1	I	Error amplifier 1 inverting input pin.
6	FB1	O	Error amplifier 1 output pin: connect resistor and capacitor between this pin and the –IN1 pin to set gain and adjust frequency characteristics.
7	DTC1*1	I	OUT1 dead time setting pin: V_{REF} voltage is divided by an external resistor and applied to set dead time. Also, a capacitor may be connected between this pin and the GND pin to perform soft start operations.

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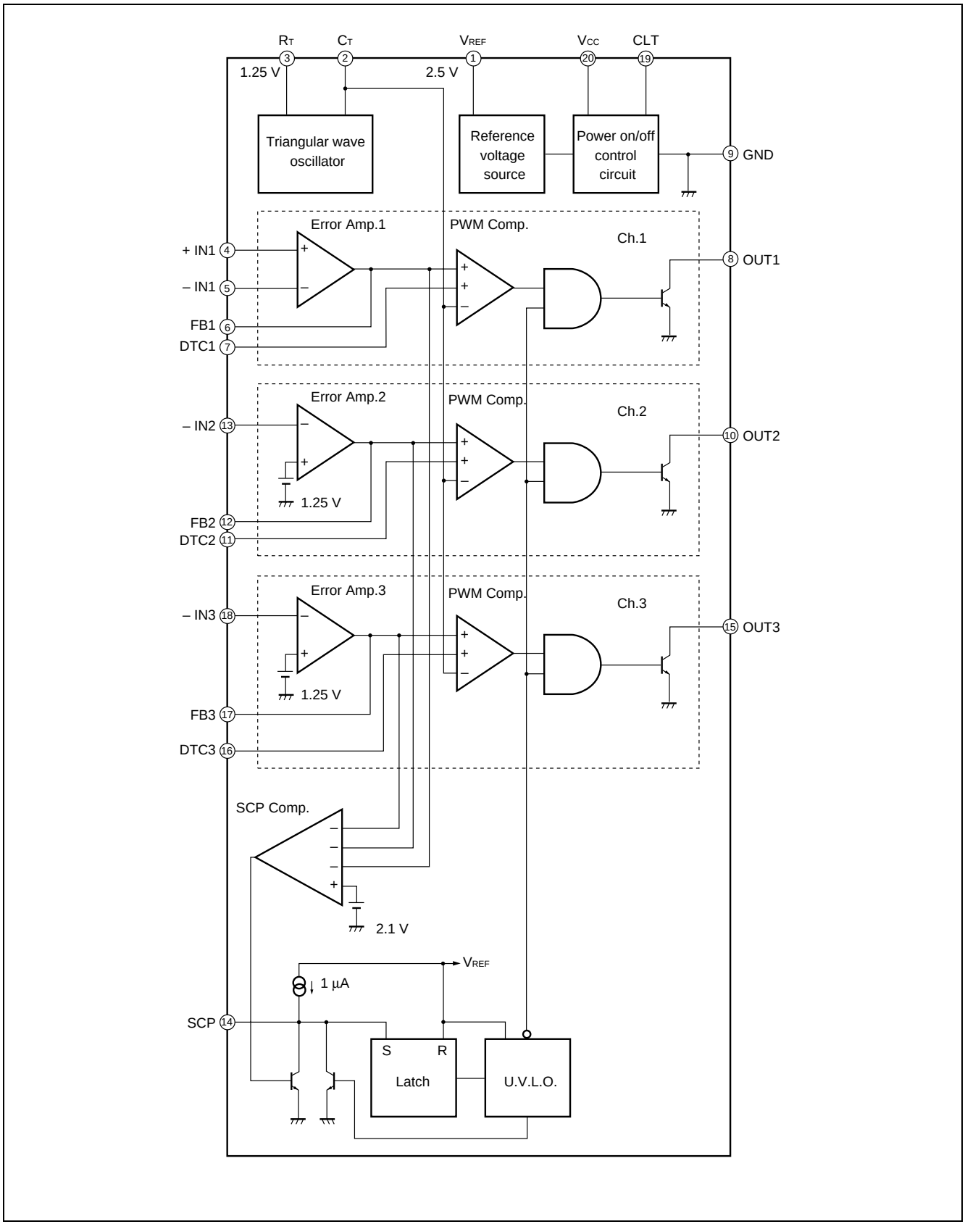
Pin No.	Pin Name	I/O	Description
8	VOUT1	O	Open collector type output pin with an emitter connected to GND. Output current may be up to 50 mA.
9	GND	—	Ground pin
10	OUT2	O	Open collector type output pin with an emitter connected to GND. Output current may be up to 50 mA.
11	DTC2*1	I	Used to set OUT2 pin dead time. V_{REF} voltage is divided by an external resistor and applied to set dead time. Also, a capacitor may be connected between this pin and the GND pin to perform soft start operations.
12	FB2	O	Error amplifier 2 output pin: connect resistor and capacitor between this pin and the –IN2 pin to set gain and adjust frequency characteristics.
13	–IN2	I	Error amplifier 2 inverting input pin.
14	SCP*2	—	Time constant setting capacitor connection for timer-latch type short prevention circuit: a capacitor should be connected between this pin and the GND pin. For details, see "■ Setting the Time Constant for the Timer-Latch Type Short Prevention Circuit."
15	OUT3	O	Open collector type output pin for emitter connected to GND. Output current may be up to 50 mA.
16	DTC3*1	I	Used to set OUT3 pin dead time. V_{REF} voltage is divided by an external resistor and applied to set dead time. Also, a capacitor may be connected between this pin and the GND pin to perform soft start operations.
17	FB3	O	Error amplifier 3 output pin: connect resistor and capacitor between this pin and the –IN3 pin to set gain and adjust frequency characteristics.
18	–IN3	I	Error amplifier 3 inverting input pin.
19	CTL	I	Power supply control pin: low level places the IC in standby mode and reduces power consumption to 10 μA or lower. Input level may be driven by TTL or CMOS.
20	V_{CC}	—	Power supply pin: voltage range is 3.6 to 18 V.

(Continued)

*1: DTC = Dead Time Control
*2: SCP = Short Circuit Protection

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTIONS

1. Reference Voltage Source

The reference voltage source uses the voltage provided at the power supply pin (pin 20) to generate a temperature-compensated reference voltage (≅ 2.50 V), which is used as the operating power supply for the internal circuits of the IC. The reference voltage source can be output through the V_{REF} pin (pin 1).

2. Triangular Wave Oscillator

By connecting a timing capacitor and resistor respectively to the C_T pin (pin 2) and R_T pin (pin 3), the oscillator can provide a triangular waveform at any desired frequency.

The waveform has an amplitude of 1.3 V to 1.9 V, and can be connected to the non-inverting input of the on-chip PWM comparator and also output through the C_T pin.

3. Error Amps

The error amps are amplifiers that detect the output voltage of the switching regulator and send the PWM control signal. The common-mode input voltage range is 1.05 V to 1.45 V, so that the voltage applied to the non-inverting input pin as a reference voltage should be either the voltage obtained by dividing the IC reference voltage output (recommended value: $V_{REF}/2$) or the voltage obtained from the R_T pin (1.25 V). The non-inverting input for the error amps 1 and 2 is internally connected to $V_{REF}/2$ voltage.

Also, a feedback transistor and capacitor can be connected between the error amp output pin and inverting input pin to provide any desired level of loop gain, enabling stable phase compensation.

4. Timer Latch (S-R Latch) Type Short Prevention Circuit

The timer-latch type short prevention circuit detects the output levels from each of the error amps. Whenever one or more error amps produces an output level of 2.1 V or higher, the timer circuit is activated starting the charging of the external protection enabler capacitor.

If the error amp output voltage does not return to normal range before the voltage in this capacitor reaches the transistor's base-emitter junction voltage (V_{BE} (≅ 0.65 V)), the latch circuit will operate to turn the output transistor off and at the same time set the dead time to 100%.

Once the prevention circuit is activated, the power must be switched on again to resume normal operation.

5. Low Input Voltage Fault Prevention Circuit (Under Voltage Lock-Out (UVLO) function)

When power is switched on, excess power or momentary drops in power line current can cause operating faults in the controller IC, which can in turn lead to damage or deterioration in systems.

The low input voltage fault prevention circuit detects the internal reference voltage level with respect to the power supply voltage level and acts to reset the latch circuit, thereby turning the output transistor off and at the same time setting the dead time to 100% and holding the SCP pin (pin 14) at "low." Operation returns to normal when the power supply voltage reaches or exceeds the UVLO threshold voltage level.

6. PWM Comparator

The PWM comparator is a voltage comparator with one inverting and two non-inverting inputs, which acts as a voltage to pulse width converter controlling the on-time of the output pulse according to the input voltage level.

When the triangular waveform produced by the oscillator is lower than either the error amp output or the DTC pin voltage, the output transistor is switched on.

It is also possible to use the DTC terminal to provide a soft start function.

7. Output Transistor

The output is open-collector type, with the emitter of the output transistor connected to the GND pin. The power transistor for external switching can carry a base current of up to 50 mA.

8. Power Supply Control

Power supply on/off control is enabled through the CTL pin (pin 19). (In standby mode, power supply current is 10 μA or less.)

■ SETTING THE TIME CONSTANT FOR THE TIMER-LATCH TYPE SHORT PREVENTION CIRCUIT

Figure 1 shows the configuration of the protection latch circuit.

The output lines from the error amps are each connected to the inverting input lines of the short protection comparator, which constantly compares them with the reference voltage of approximately 2.1 V connected to the non-inverting input.

When load conditions in the switching regulator are stabilized, there is no variation in the output from the error amps, and therefore the short prevention controls are held in equilibrium. In this situation, voltage at the SCP pin (pin 14) is held at approximately 50 mV.

When load conditions change rapidly, as in the case of a load short, high potential signal (greater than 2.1V) from the error amps is input to the inverting signal input of the short protection comparator, and the short protection comparator outputs a “low” level signal. The transistor Q1 is consequently switched off, so that short protection capacitor C_{PE} externally connected to the SCP pin voltage is then charged according to the following formulas.

$$V_{PE} = 50\ mV + t_{PE} \times 10^{-6}/C_{PE}$$

$$0.65 = 50\ mV + t_{PE} \times 10^{-6}/C_{PE}$$

$$C_{PE} = t_{PE}/0.6\ (\mu F)$$

When the short protection capacitor is charged to a level of approximately 0.65 V, the SR latch is set and the low input voltage fault prevention circuit is enabled, turning the output drive transistor off. At the same time, the dead time is set to 100% and the SCP pin (pin 14) is held “low.” This closes the S-R latch input and then discharges the capacitor C_{PE}

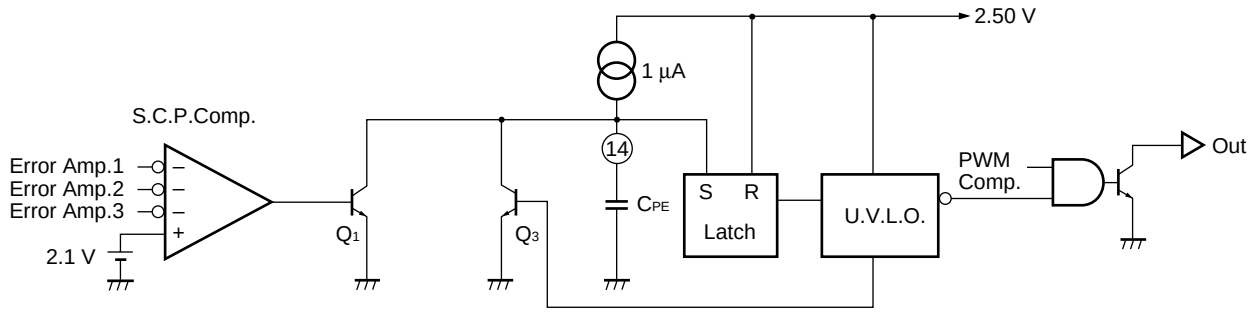


Figure 1 Protection Latch Circuit

■ SETTING OUTPUT VOLTAGE

The following diagrams show the connections used to set the output voltage.

Because the power supply to the error amps is provided by the same reference voltage circuit used for the other internal circuits, the common-mode input voltage range is set at 1.05 V to 1.45 V.

The reference voltage input to the +IN and -IN pins should be set at 1.25 V ($V_{REF}/2$). The method of connection for channel 1 is different from channel 2 and channel 3. In addition, channel 1 is capable of picking up both positive and negative voltages, while channel 2 and channel 3 can pick up only positive output voltages.

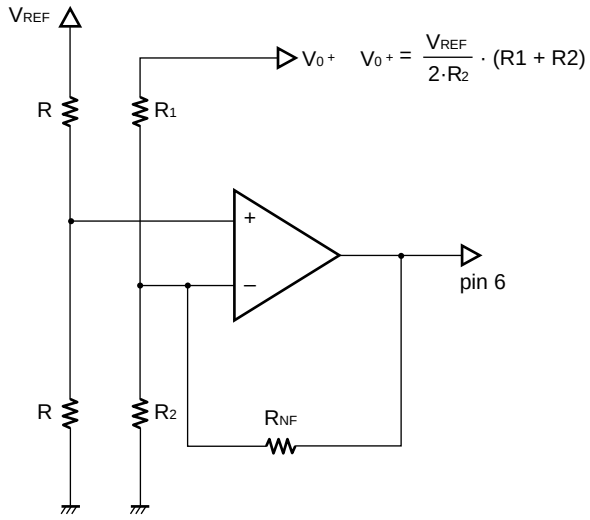


Figure 1 Error amp (channel 1) connection: Output voltage Vo positive

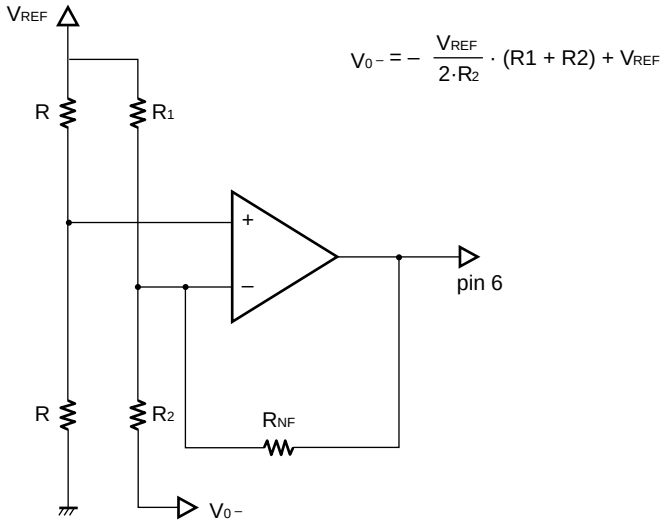


Figure 2 Error amp (channel 1) connection: Output voltage Vo positive

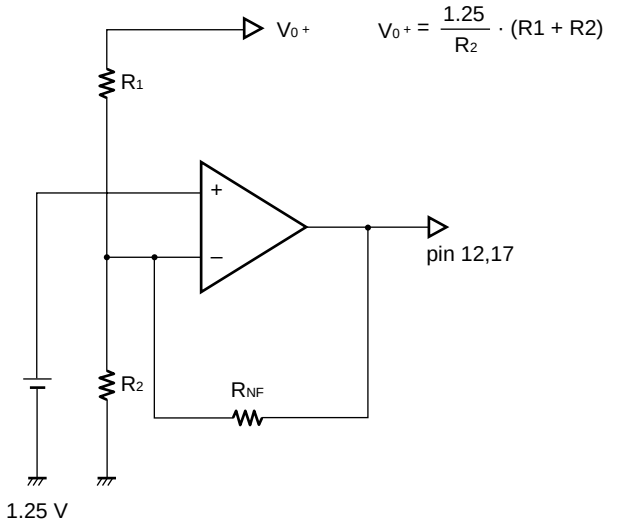


Figure 3 Error amp (channel 2, channel 3) connection

The non-inverting input to the error amps on channel 2 and channel 3 is internally connected to $V_{REF}/2$, and therefore cannot be configured for inverting output.

	ch-1	ch-2	ch-3
Step up	○	○	○
Step down	○	○	○
Inverting	○	×	×

■ USING THE R_T PIN

The triangular waves, as shown in Figure 1, act to set the oscillator frequency by charging and discharging the capacitor connected to the C_T pin using the current value of the resistor connected to the R_T pin.

In addition, when voltage level $V_{REF}/2$ is output to external circuits from the R_T pin, care must be taken in making the external circuit connections to adjust for the fact that I_1 is increased by the value of the current I_2 to the external circuits in determining the oscillator frequency (see Figure 2).

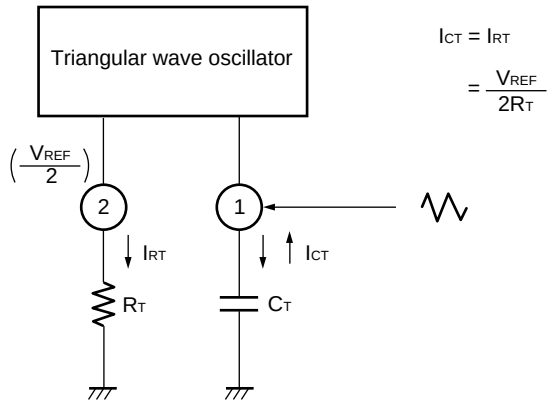


Figure 1 No $V_{REF}/2$ connection to external circuits from R_T pin

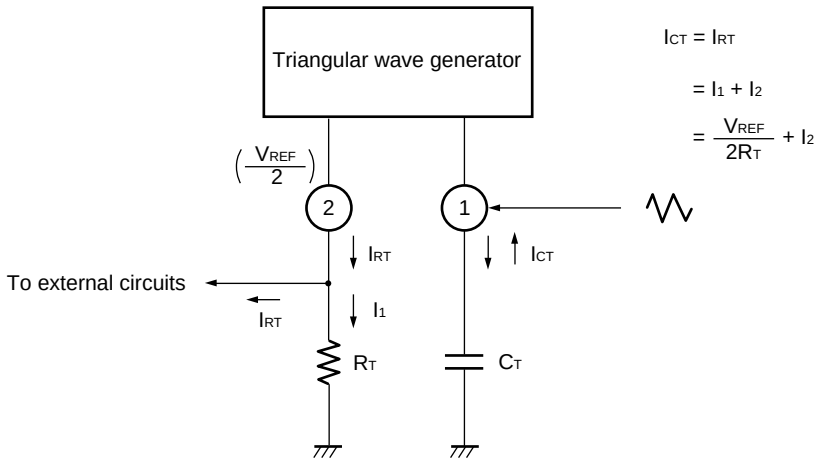


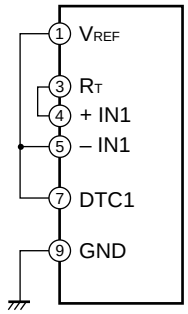
Figure 2 $V_{REF}/2$ connection to external circuits from R_T pin

■ TREATMENT OF UNUSED ERROR AMPS

Any error amps that are not used should be handled as follows.

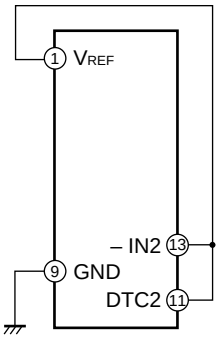
Note that failure to apply proper treatment to error amps will cause the SCP circuit to activate and disable the switching regulator output.

1. Error Amp (channel 1) Not In Use



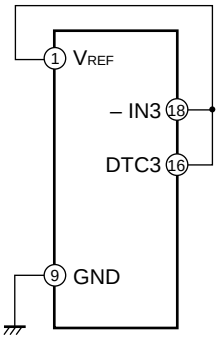
Note: Pin 6 and pin 8 shoud be left open.

2. Error Amp (channel 2) Not In Use



Note: Pin 10 and pin 12 shoud be left open.

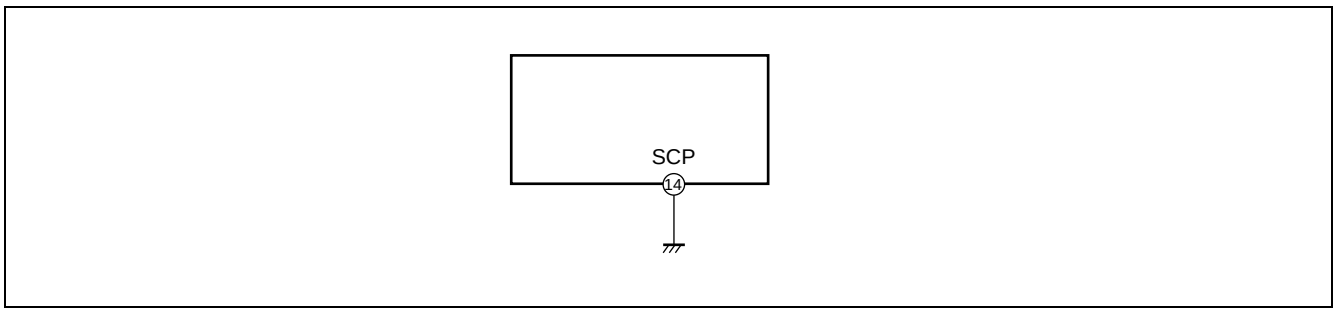
3. Error Amp (channel 3) Not In Use



Note: Pin 15 and pin 17 shoud be left open.

■ TREATMENT OF UNUSED SCP PIN

When the timer latch short protection circuit is not used, the SCP pin should be connected to the GND by the shortest possible path.



■ ABSOLUTE MAXIMUM RATINGS

(Ta = +25°C)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage	V_{CC}	—		20	V
Error amp input voltage	V_{IN}	—		–0.3 to 10	V
Dead time control input voltage	V_{dt}	—		–0.3 to 2.8	V
Control input voltage	V_{CTL}	—		–0.3 to 20	V
Collector output voltage	V_{OUT}	—		20	V
Collector output current	I_{OUT}	—		75	mA
Allowable loss	P_D*1	Ta ≤ +25°C	SOP Version	740*2	mW
			DIP Version	1110	
Operating temperature	Top	—		–30 to 85	°C
Storage temperature	Tstg	—		–55 to 125	°C

*1: For operation in conditions where Ta > +25°C, the SOP version should be derated by 7.4 mW/°C, and the DIP version should be derated by 11.1 mW/°C.

*2: When mounted on a 4 cm-square dual-sided epoxy board.

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min.	Typical	Max.	
Power supply voltage	V_{CC}	—	3.6	6.0	18.0	V
Error amp input voltage	V_{IN}	—	1.05	—	1.45	V
Control input voltage	V_{CTL}	—	0	—	18	V
Collector output voltage	V_{OUT}	—	—	—	18	V
Collector output current	I_{OUT}	—	0.3	—	50	mA
Reference voltage output current	I_{REF}	—	–3	–1	0	mA
Timing capacitance	C_T	—	150	—	15000	pF
Timing resistance	R_T	—	5.1	—	100	kΩ
Oscillator frequency	f_{OSC}	—	1	—	500	kHz
Operating temperature	Top	—	–30	25	85	°C

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 6 V, Ta = +25°C)

	Parameter	Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Reference voltage	Output voltage	V_{REF}	I_{OR} = –1 mA	2.45	2.50	2.55	V
	Output voltage temperature variation	V_{RTC}	Ta = –30 to 85°C	–2	±0.2	2	%
	Input stability	Line	V_{CC} = 3.6 to 18 V	—	2	10	mV
	Load stability	Load	I_{OR} = –0.1 to –1mA	—	1	7.5	mV
	Short output current	I_{OS}	V_{REF} = 2 V	–30	–10	–3	mA
Undervoltage lock out circuit (UVLO)	Threshold voltage	V_{tH}	I_{OR} = –0.1 mA	—	2.72	—	V
		V_{tL}	I_{OR} = –0.1 mA	—	2.60	—	V
	Hysteresis width	V_{HYS}	I_{OR} = –0.1 mA	80	120	—	mV
	Reset voltage (V_{CC})	V_R	—	1.5	1.9	—	V
Short circuit protection (SCP)	Input threshold voltage	V_{tPC}	—	0.60	0.65	0.70	V
	Input standby voltage	V_{STB}	No pull-up	—	50	100	mV
	Input latch voltage	V_{IN}	No pull-up	—	50	100	mV
	Input source current	I_{bpc}	—	–1.4	–1.0	–0.6	µA
	Comparator threshold voltage	V_{tC}	Pin 6, pin 12, pin 17	—	2.1	—	V
Triangular wave oscillator	Oscillator frequency	f_{OSC}	C_T = 330 pF, RT = 15 kΩ	160	200	240	kHz
	Frequency deviation	f_{dev}	C_T = 330 pF, RT = 15 kΩ	—	±5	—	%
	Frequency deviation (V_{CC})	f_{dV}	V_{CC} = 3.6 to 18 V	—	±1	—	%
	Frequency deviation (Ta)	f_{dT}	Ta = –30 to 85°C	–4	—	+4	%
Dead time controller (DTC)	Input threshold voltage	V_{t0}	Duty cycle = 0 %	1.05	1.3	—	V
		V_{t100}	Duty cycle = 100 %	—	1.9	2.25	V
	ON duty cyclet	D_{tr}	V_{dt} = V_R/1.45 V	55	65	75	%
	Input bias current	I_{bdt}	—	—	0.2	1	µA
	Latch mode sink current	I_{dt}	V_{dt} = 2.5 V	150	500	—	µA
	Latch input voltage	V_{dt}	I_{dt} = 100 µA	—	—	0.3	V

(Continued)

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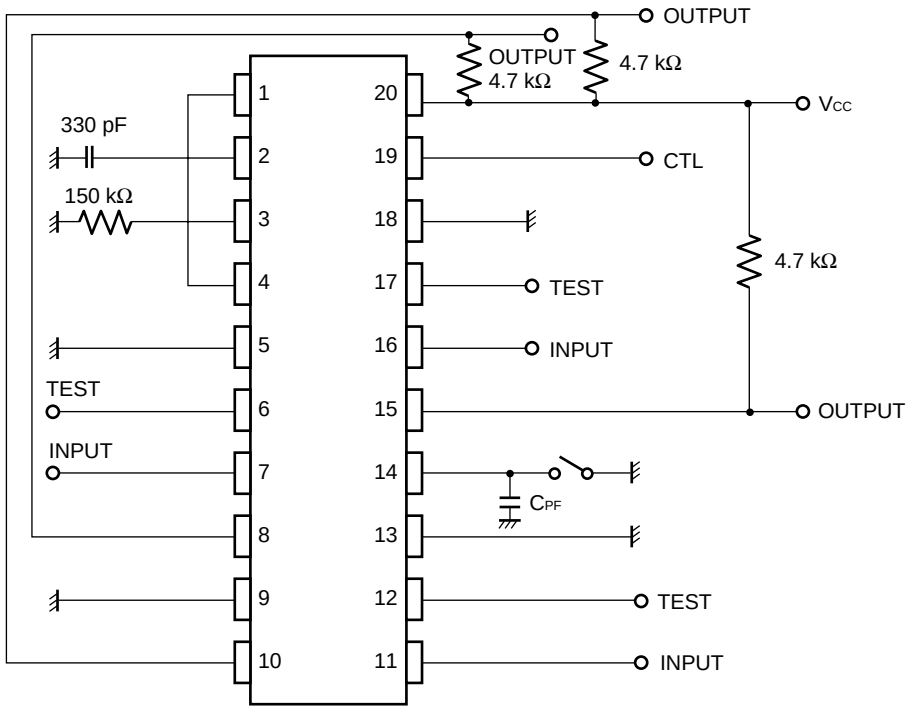
(V_{CC} = 6 V, Ta = +25°C)

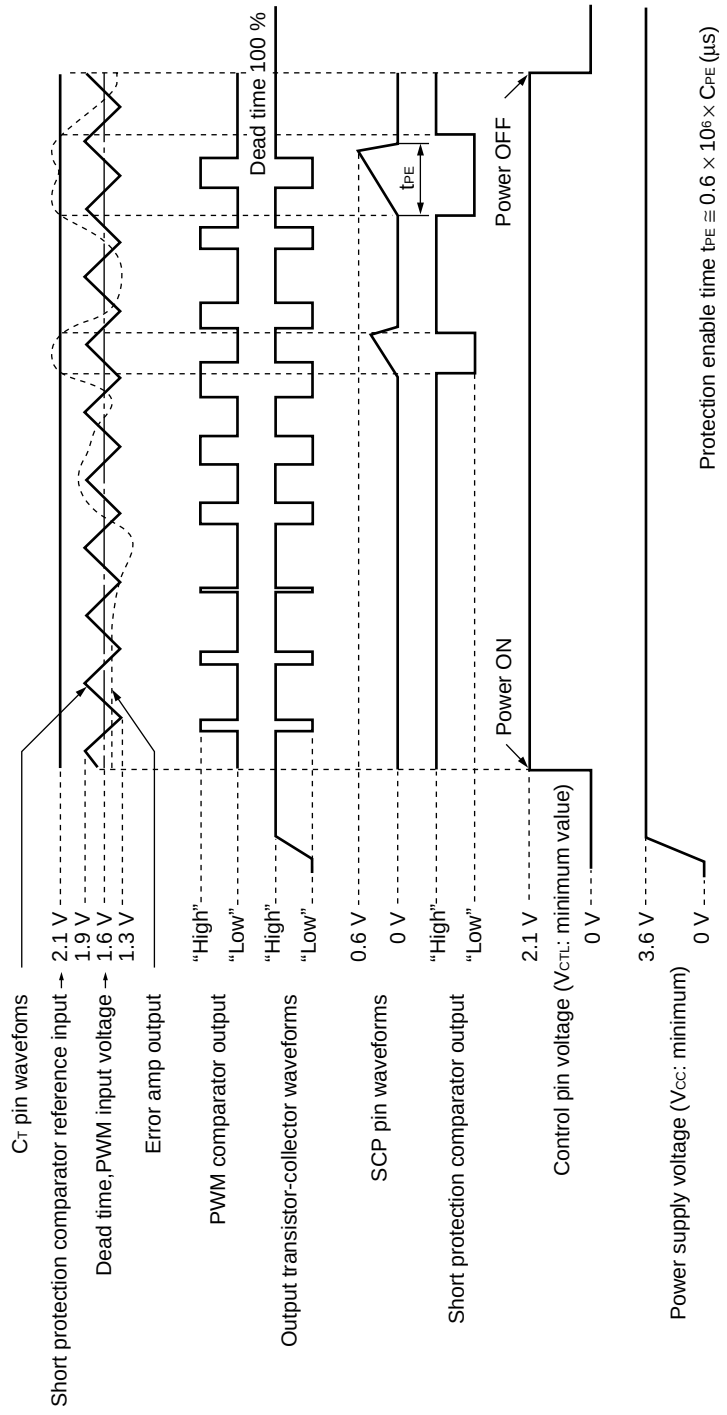
	Parameter	Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Error amps	Input offset voltage	V_{IO}	V_{OUT} = 1.6 V	–6	—	6	mV
	Input offset current	I_{IO}	V_{OUT} = 1.6 V	–100	—	100	nA
	Input bias current	I_B	V_{OUT} = 1.6 V	–500	–100	—	nA
	Common mode input voltage range	V_{ICR}	V_{CC} = 3.6 to 18 V	1.05	—	1.45	V
	Voltage gain	Av	—	70	80	—	dB
	Frequency bandwidth	BW	Av = 0 dB	—	0.8	—	MHz
	Common mode rejection ratio	CMRR	—	60	80	—	dB
	Maximum output voltage range	V_{OM}+	—	V_{REF} –0.3	—	—	V
		V_{OM}-	—	—	0.7	0.9	V
	Output sink current	I_{OM}+	V_{OUT} = 1.6 V	—	1.0	—	mA
	Output source current	I_{OM}-	V_{OUT} = 1.6 V	—	–60	—	µA
PWM comparator	Input threshold voltage	V_{t0}	Duty cycle = 0 %	1.05	1.3	—	V
		V_{t100}	Duty cycle = 100 %	—	1.9	2.25	V
	Input sink current	I_{IN}+	Pin 6, pin 12, pin 17	—	1.0	—	mA
	Input source current	I_{IN}-	Pin 6, pin 12, pin 17	—	–60	—	µA
Control block	Input OFF conditions	V_{OFF}	—	—	—	0.7	V
	Input ON conditions	V_{ON}	—	2.1	—	—	V
	Control pin current	I_{CTL}	V_{CTL} = 10 V	—	200	400	µA
Output block	Output leak current	Leak	V_{OUT} = 18 V	—	—	10	µA
	Output saturation voltage	V_{SAT}	I_{OUT} = 50 mA	—	1.1	1.4	V
Entire device	Standby current	I_{CCS}	V_{CTL} = 0 V	—	—	10	µA
	Average feed current	I_{CCa}	V_{CTL} = V_{CC}, no output load	—	2.1	3.2	mA

- Voltage control on channel 1 may be positive or negative.
- The non-inverting input to the error amps on channel 2 and channel 3 is internally connected to V_{REF}/2, and therefore voltage control is positive only.
- V_{REF}/2 output can be obtained from the R_T pin.

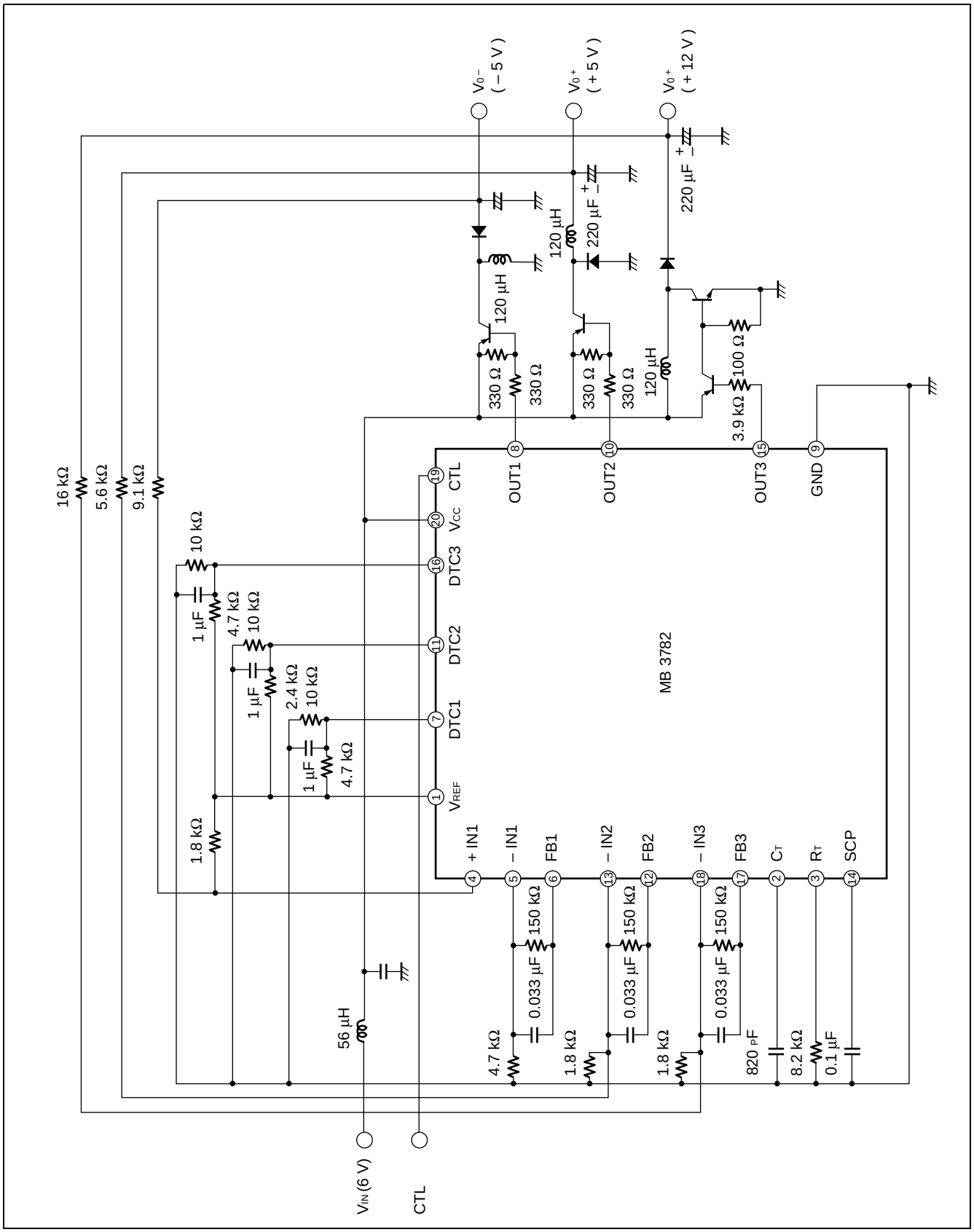
■ TEST CIRCUIT



■ TIMING CHART (INTERMAL WAVEFORMS)

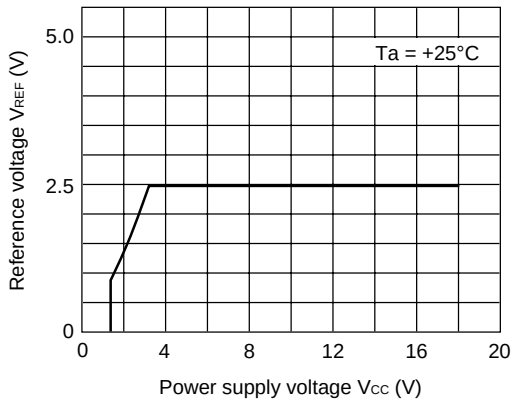


■ EXAMPLE OF APPLICATION

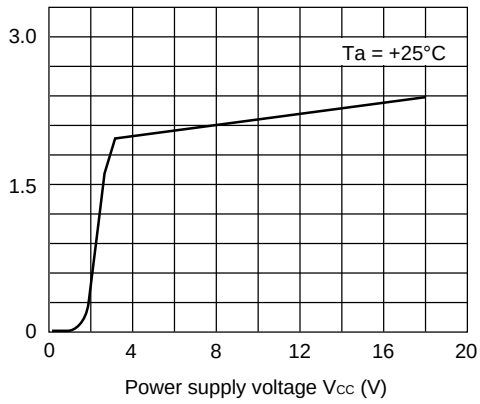


■ TYPICAL CHARACTERISTICS CURVES

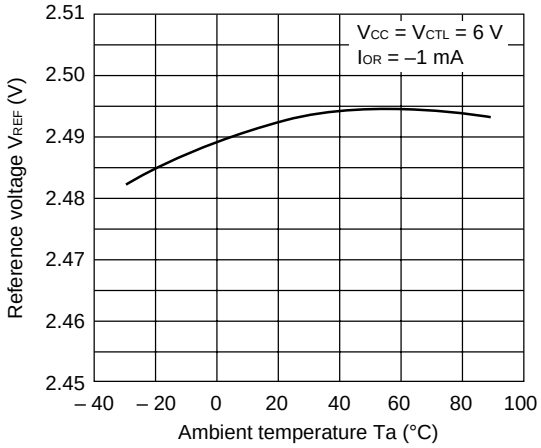
Power supply voltage vs.reference voltage



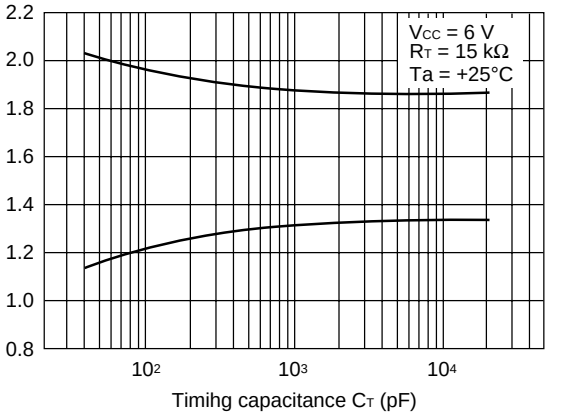
Power supply voltage vs.average feed current



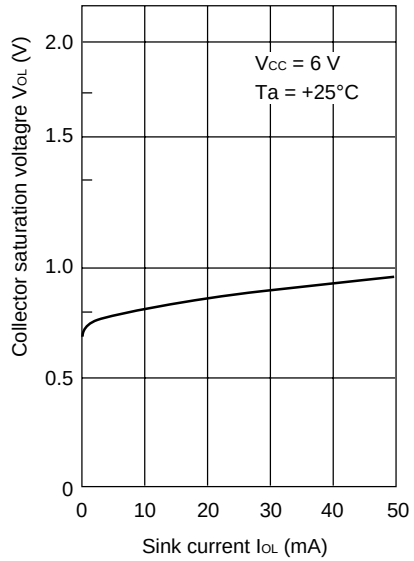
Ambient temperature vs.reference voltage



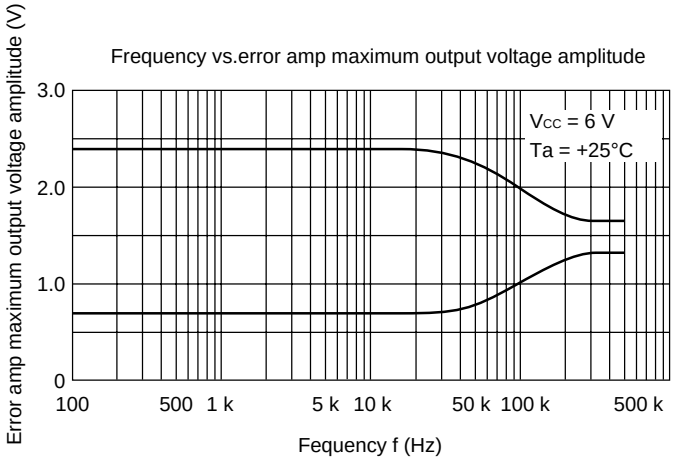
Timing capacity vs.triangular wave maximum amplitude voltage



Sink current vs.collector saturation voltage

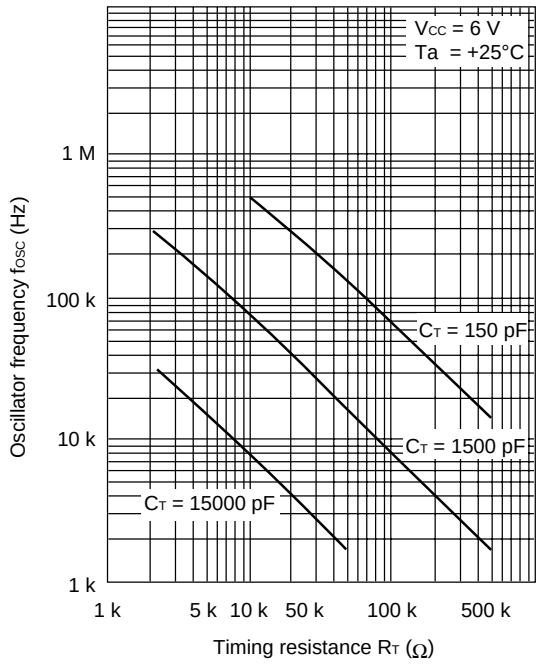


Frequency vs.error amp maximum output voltage amplitude

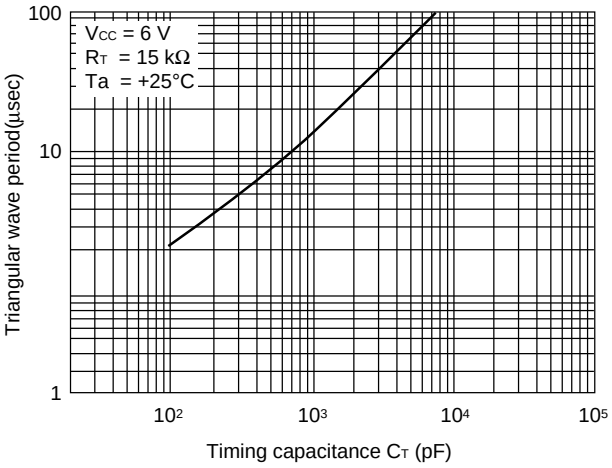


(Continued)

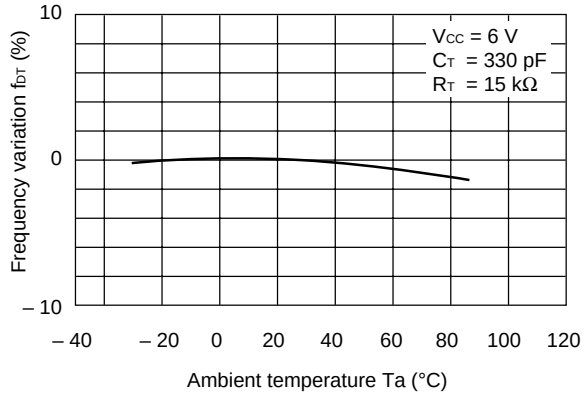
Timing resistance vs.oscillator frequency



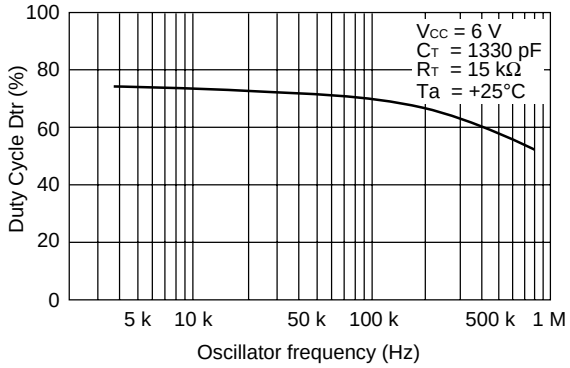
Power supply voltage vs.averege feed current



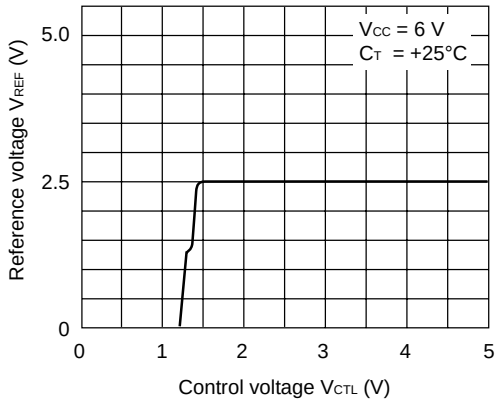
Ambient temperature vs.oscillator frequency



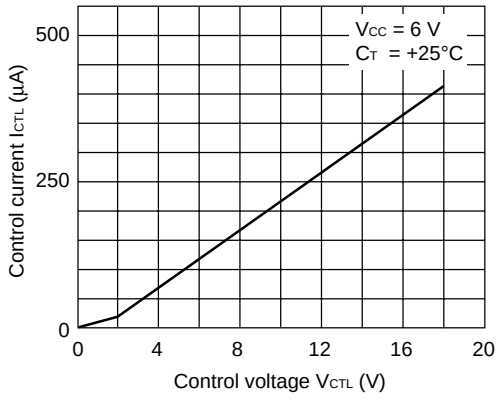
Oscillator frequency vs.duty cycle



Control voltage vs.reference voltage

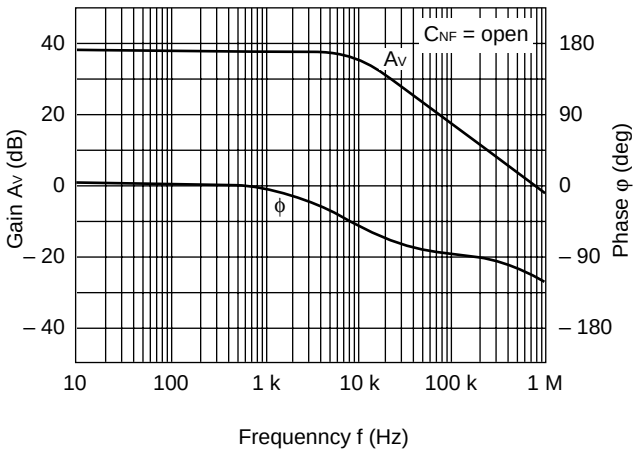


Control input current

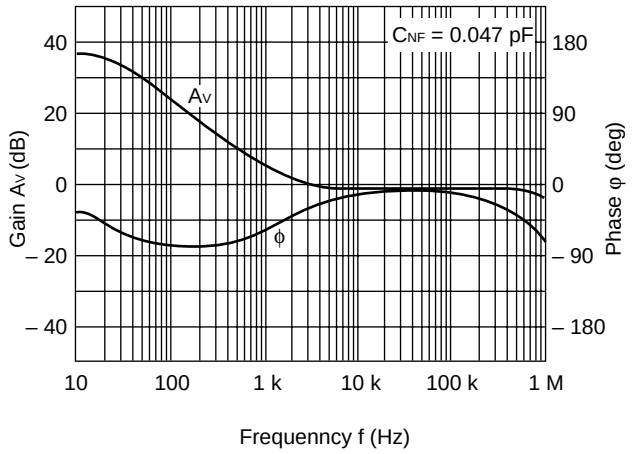


(Continued)

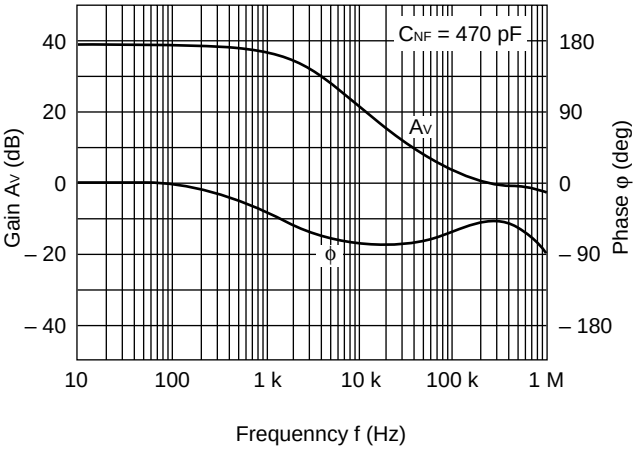
Frequenncy vs.gain and phase



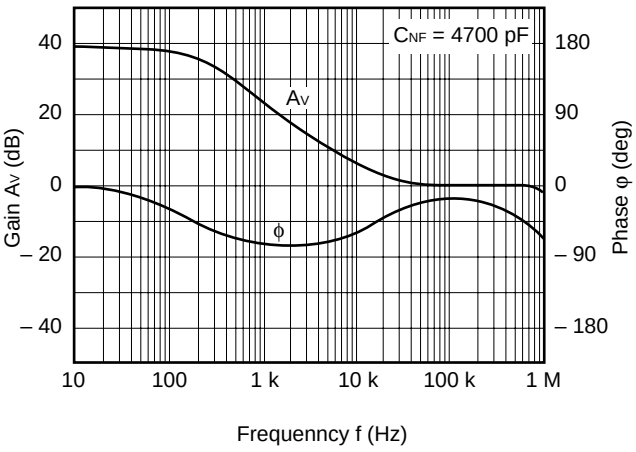
Frequenncy vs.gain and phase



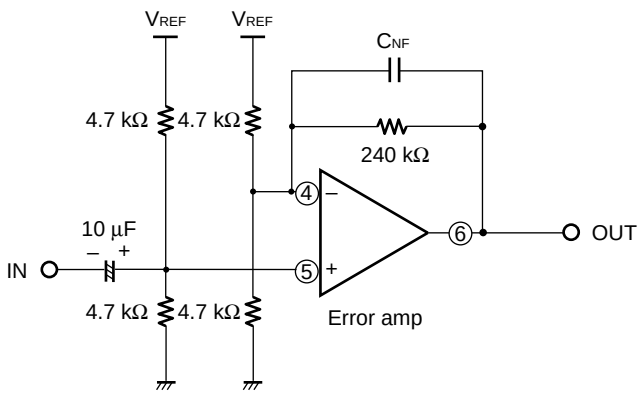
Frequenncy vs.gain and phase



Frequenncy vs.gain and phase



Test Circuit



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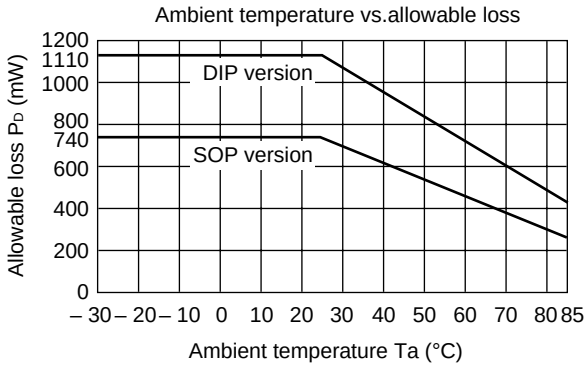

Ambient temperature vs.allowable loss
Allowable loss P_D (mW)
1200
1110
1000
800
740
600
400
200
0
DIP version
SOP version
– 30 – 20 – 10 0 10 20 30 40 50 60 70 80 85
Ambient temperature Ta (°C)

■ APPLICATIONS

3. Concerning Equivalent Series Resistance and Stability of Smoothing Capacitors

In DC/DC converters, the equivalent series resistance value (ESR) of smoothing capacitors has a major influence on loop phase characteristics.

The ESR is a means by which phase characteristics approximate phase relationships to ideal capacitors in high-frequency bands (see Graph 1-1), thus improving system stability. At the same time, the use of smoothing capacitors with low ESR reduces system stability, so that care must be taken when using semiconductor electrolytic capacitors (OS capacitors) or tantalum capacitors with low ESR.

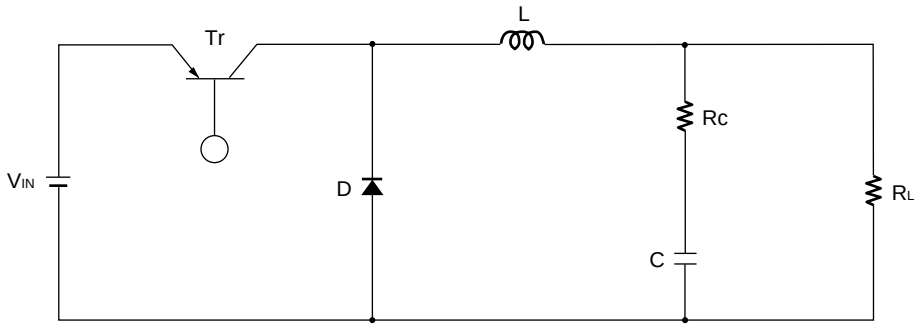
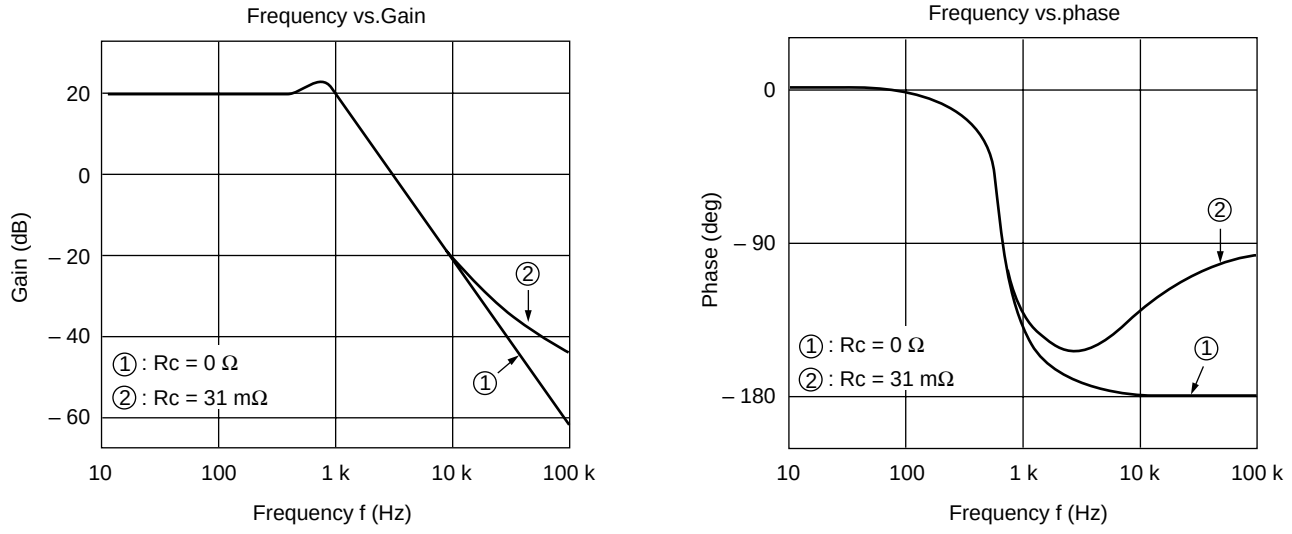


Figure 1 Basic circuit for step-down voltage DC/DC converter



Graph 1 Frequency vs. gain and phase

- **Reference data**

Changing the smoothing capacitor from an aluminum electrolytic capacitor (RC ≅ 1.0Ω) to a lower-ESR semiconductor electrolytic capacitor (OS capacitor: RC ≅ 0.2 Ω) decreases the phase margin (see Graphs 1-2, 1-3).

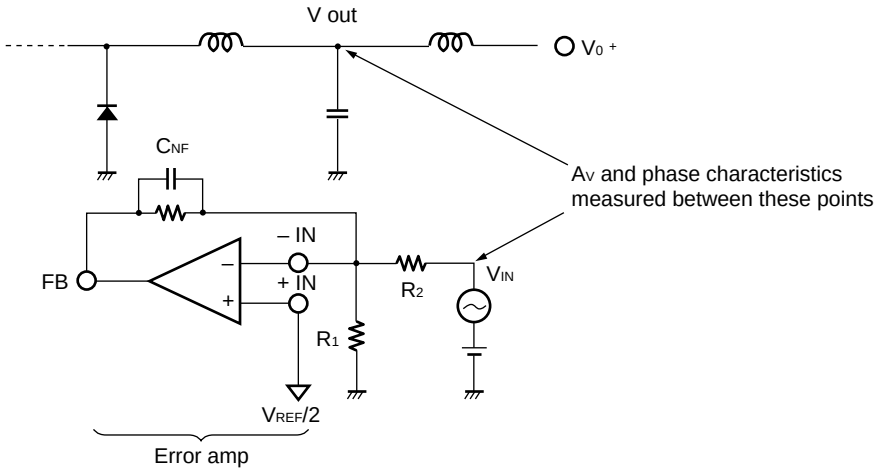
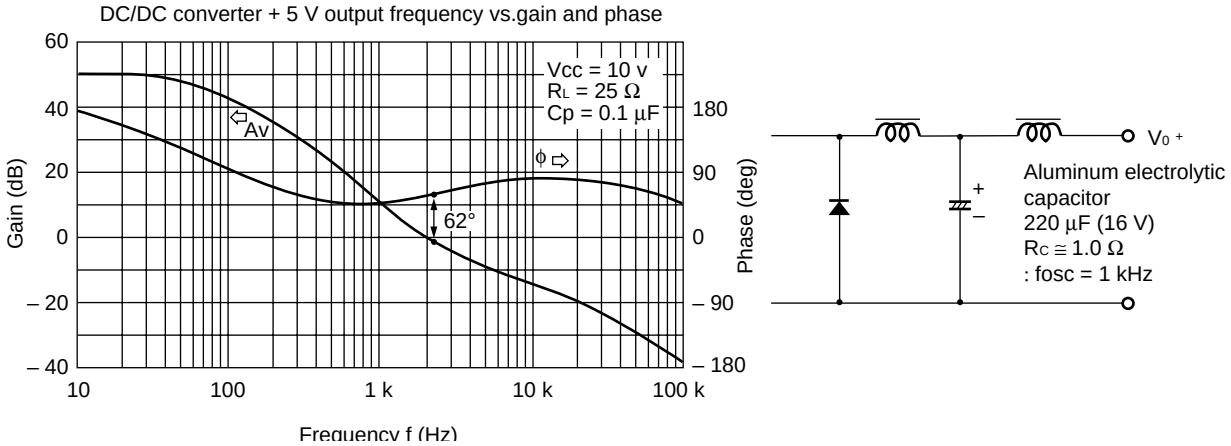
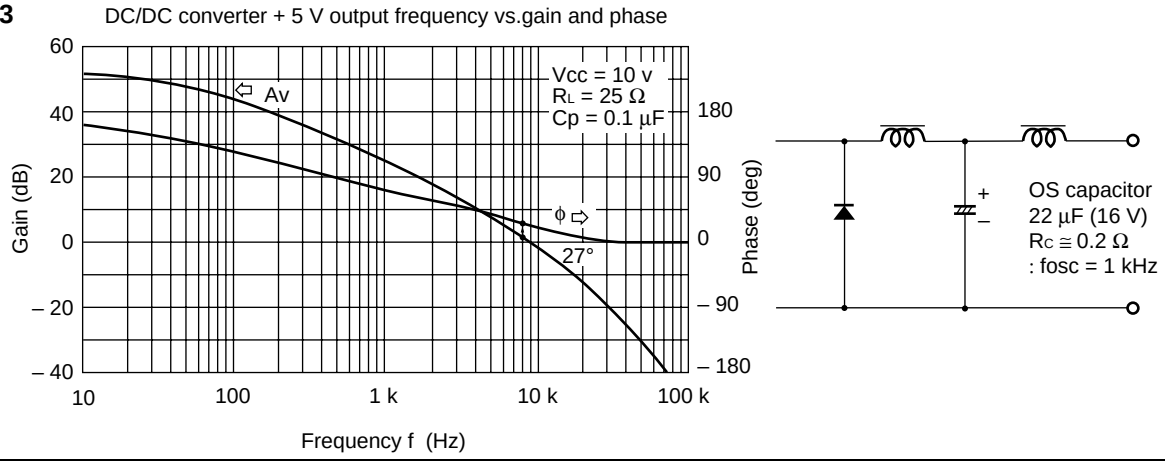


Figure 2 Measurement of DC/DC Capacitor AV and Phase (Ψ) Characteristics

Graph



Graph 3

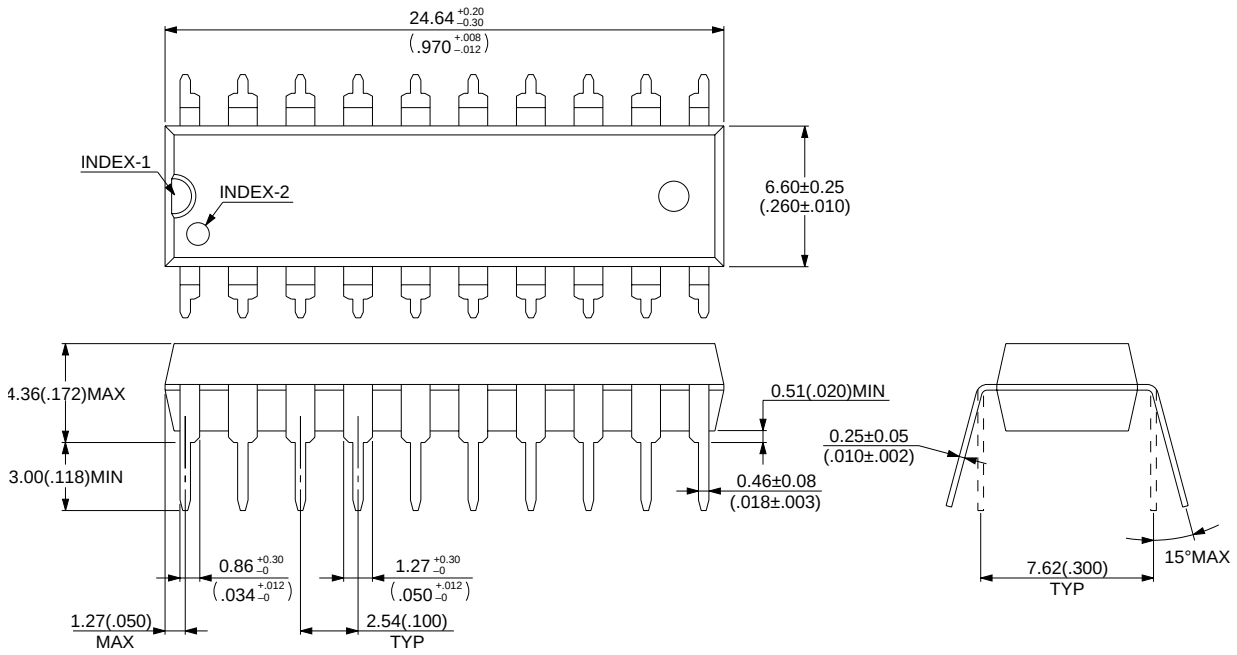


■ ORDERING INFORMATION

Part number	Package	Remarks
MB3782P	Plastic DIP, 20 pin (DIP-20P-M01)	
MB3782PF	Plastic SOP, 20 pin (FPT-20P-M01)	

■ PACKAGE DIMENSIONS

Plastic DIP, 20 pin
(DIP-20P-M01)

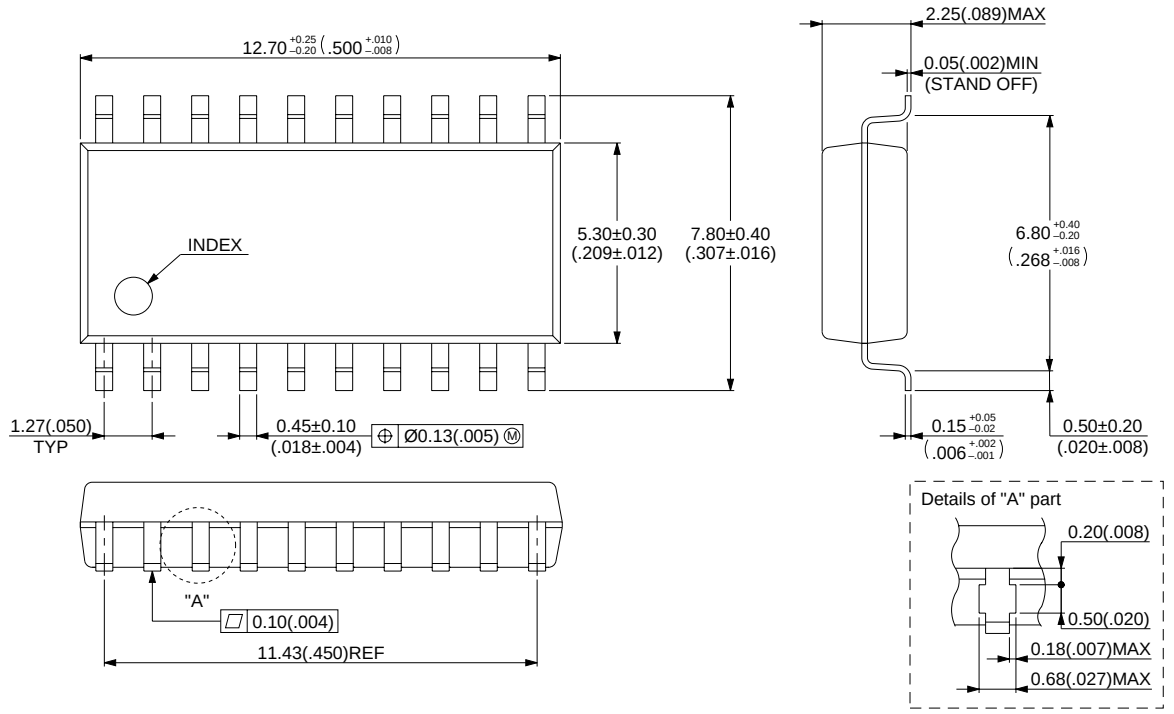


Dimensions in mm (inches)

(Continued)

(Continued)

Plastic SOP, 20 pin
(FPT-20P-M01)



Dimensions in mm (inches)

FUJITSU LIMITED

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