PRELIMINARY SPECIFICATIONS

SHARP®

Integrated Circuits Group

LRS1337

Stacked Chip

32M Flash Memory and 4M SRAM

(Model No.: LRS1337)

Spec No.: MFM2-J11504A

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- Office electronics
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- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

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- Other safety devices and safety equipment, etc.

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(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

● Please direct all queries regarding the products covered herein to a sales representative of the company.

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Part 1 Overview

1. Description

The LRS1337 is a combination memory organized as 2,097,152×16 bit flash memory and 262,144×16 bit static RAM in one package.

Features

○Power supply .... 2.7 V to 3.6 V
○Operating temperature .... −25 ℃ to +85 ℃
○Not designed or rated as radiation hardened
○ 72 pin CSP (LCSP072-P-0811) plastic package
○Flash memory has P-type bulk silicon, and SRAM has P-type bulk silicon.

Flash Memory

○Access Time .... 90 ns (Max.)

○Operating current (The current for F-V_{CC} pin and F-V_{CCW} pin)
- Read .... 25 mA (Max. t_{CYCLE}=200ns)
- Word write .... 57 mA (Max.)
- Block erase .... 42 mA (Max.)

○Standby current (The current for F-V_{CC} pin) .... 20 μA (Max. F-V_{CCW}≦0.2V F-$\overline{BE}$, F-$\overline{RP}$≧F-V_{CC}-0.2V)

○Optimized Array Blocking Architecture for each Bank.
- Two 4k-word Boot Blocks
- Six 4k-word Parameter Blocks
- Thirty-one 32k-word Main Blocks
- Bottom Boot Location

○ Extended Cycling Capability
- 100,000 Block Erase Cycles

○ Enhanced Automated Suspend Options
- Word Write Suspend to Read
- Block Erase Suspend to Word Write
- Block Erase Suspend to Read

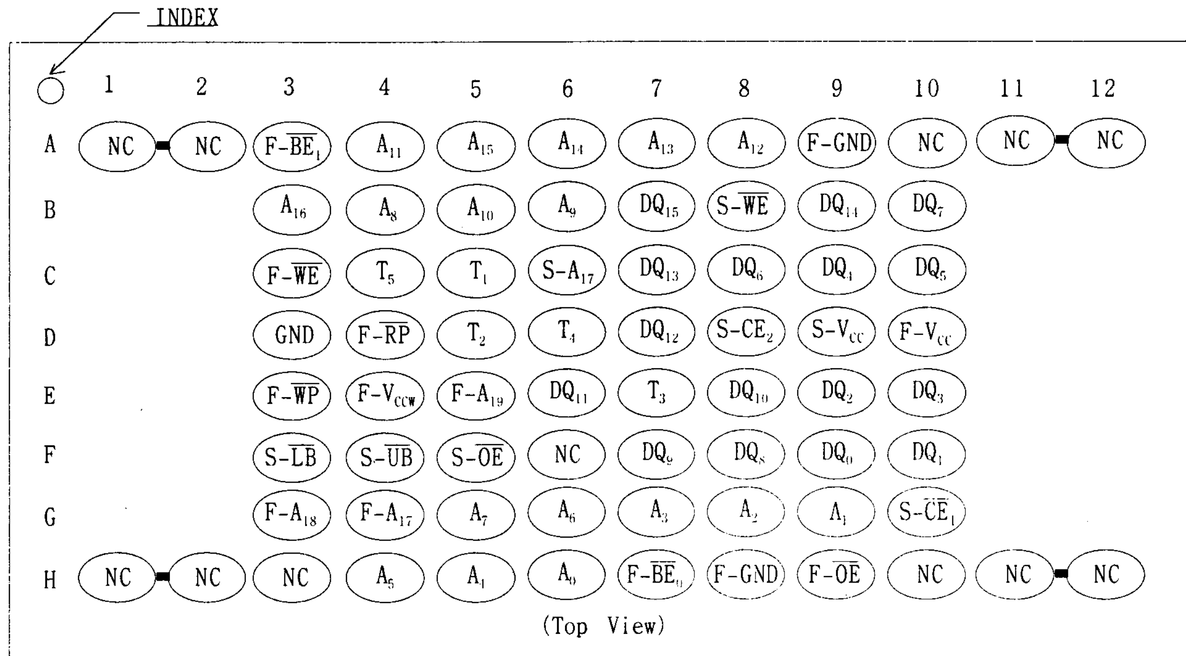
SRAM

○Access Time .... 85 ns (Max.)

○Operating current .... 45 mA (Max.)
.... 8 mA (Max. t_{RC}, t_{WC}=1 μs)

○Standby current .... 15 μA (Max.)
○Data retention current .... 15 μA (Max. V_{CCDR}=3.0V)

2. Pin Configuration



Note: Two pins of corner are connected.
From T_1 to T_5 are needed to be open.

Pin	Description	Type
A_0 to A_{16}	Address Inputs (Common)	Input
F-A_{17} to F-A_{19}	Address Inputs (Flash)	Input
S-A_{17}	Address Input (SRAM)	Input
F-$\overline{BE}_0$, F-$\overline{BE}_1$	Bank Enable Inputs (Flash)	Input
S-$\overline{CE}_1$, S-CE_2	Chip Enable Inputs (SRAM)	Input
F-$\overline{WE}$	Write Enable Input (Flash)	Input
S-$\overline{WE}$	Write Enable Input (SRAM)	Input
F-$\overline{OE}$	Output Enable Input (Flash)	Input
S-$\overline{OE}$	Output Enable Input (SRAM)	Input
S-$\overline{LB}$	SRAM Byte Enable Input (DQ_0 to DQ_7)	Input
S-$\overline{UB}$	SRAM Byte Enable Input (DQ_8 to DQ_{15})	Input
F-$\overline{RP}$	Reset Power Down Input (Flash) Block erase and Write : V_{HH} Read : V_{IH} Reset Power Down : V_{IL}	Input
F-$\overline{WP}$	Write Protect Input (Flash) Two Boot Blocks Locked : V_{IL}	Input
DQ_0 to DQ_{15}	Data Inputs and Outputs (Common)	Input/Output
F-V_{CC}	Write, Erase Power Supply (Flash)	Power
S-V_{CC}	Power Supply (SRAM)	Power
F-V_{CCW}	Write, Erase Power Supply (Flash) Block Erase and Write : F-V_{CCW}=V_{CCWLK} All Blocks Locked : F-V_{CC}<V_{CCWLK}	Power
F-GND	GND (Flash)	Power
GND	GND (Common)	Power
NC	Non Connection	—
T_1 to T_5	Test pins (Should be open)	—

3. Truth Table (*1)

Flash	SRAM	Note	F-$\overline{BE}_{0,1}$	F-$\overline{RP}$	F-$\overline{OE}$	F-$\overline{WE}$	S-$\overline{CE}_1$	S-CE_2	S-$\overline{OE}$	S-$\overline{WE}$	S-$\overline{LB}$	S-$\overline{UB}$	DQ_0 to DQ_{15}
Read	Standby	*3, 5, 6	L	H	L	H	*7		X	X	*7		Dout
Output Disable		*5, 6			H								High-Z
Write		*2, 3, 4, 5, 6				L							Din
Standby	Read		H	H	X	X	L	H	L	H	*8		
	Output Disable								H	H	X	X	High-Z
									X	X	H	H	
	Write								L	L	*8		
Reset Power Down	Read		X	L	X	X	L	H	L	H	*8		
	Output Disable								H	H	X	X	High-Z
									X	X	H	H	
	Write								L	L	*8		
Standby	Standby	*5	H	H	X	X	*7		X	X	*7		High-Z
Reset Power Down		*5	X	L									

Notes) *1. L=V_{IL}, H=V_{IH} , X=H or L. Refer to DC Characteristics.

*2. Command writes involving block erase, bank erase, word write or lock-bit configuration are reliably executed when F-V_{CCW}=V_{CCWH} and F-V_{CC}=2.7 V to 3.6 V.

*3. Never hold F-$\overline{OE}$ low and F-$\overline{WE}$ low at the same timing.

*4. Refer Section 5. Flash Memory Comand Definition for valid DIN during a write operation.

*5. F-$\overline{WP}$ set to V_{IL} or V_{IH}.

*6. Both F-$\overline{BE}_0$ and F-$\overline{BE}_1$ must not be low at the same time.

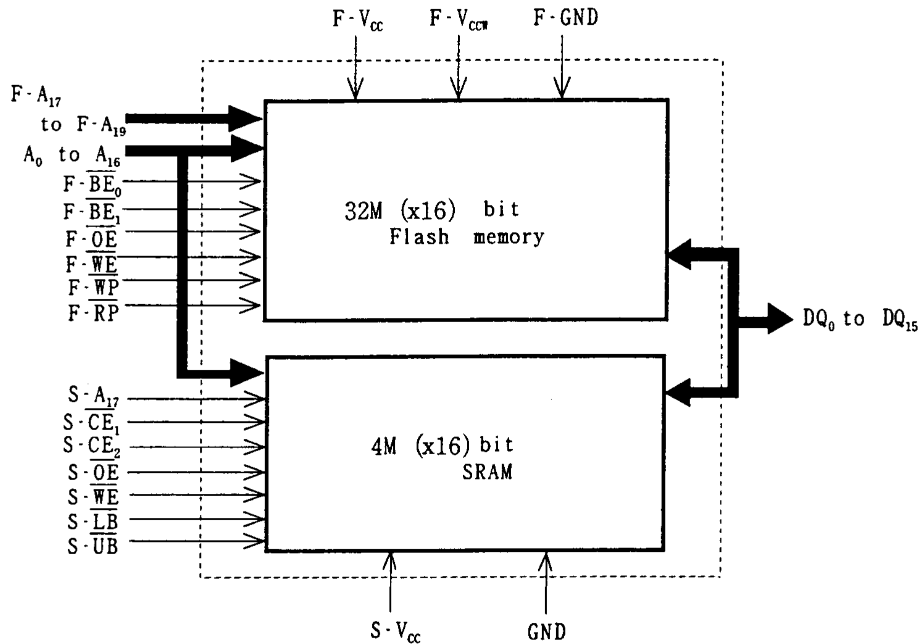
*7) SRAM Standby Mode

Mode	Pin			
	S-$\overline{CE}_1$	S-CE_2	S-$\overline{LB}$	S-$\overline{UB}$
Standby (SRAM)	H	X	X	X
	X	L	X	X
	X	X	H	H

*8) S-$\overline{LB}$, S-$\overline{UB}$ Control Mode

Mode (SRAM)	S-$\overline{LB}$	S-$\overline{UB}$	DQ_0 to DQ_7	DQ_8 to DQ_{15}
Read/Write	L	L	Dout/Din	Dout/Din
	L	H	Dout/Din	High-Z
	H	L	High-Z	Dout/Din

4. Block Diagram



5 Command Definitions for Flash Memory (*1)

Command	Bus Cycles Req'd.	Note	First Bus Cycle			Second Bus Cycle		
			Oper(*2)	Address (*3)	Data (*3)	Oper(*2)	Address (*3)	Data (*3)
Read Array/Reset	1		Write	XA	FFH			
Read Identifier Codes	≧2	*4	Write	XA	90H	Read	IA	ID
Read Status Register	2		Write	XA	70H	Read	XA	SRD
Clear Status Register	1		Write	XA	50H			
Block Erase	2	*5	Write	BA	20H	Write	BA	DOH
Bank Erase	2		Write	XA	30H	Write	XA	DOH
Word Write	2	*5	Write	WA	40H or 10H	Write	WA	WD
Block Erase and Word Write Suspend	1	*5	Write	XA	BOH			
Block Erase and Word Write Resume	1	*5	Write	XA	DOH			
Set Block Lock-Bits	2	*7	Write	BA	60H	Write	BA	01H
Clear Block Lock-Bits	2	*6,7	Write	XA	60H	Write	XA	DOH
Set Permanent Lock-Bits	2	*8	Write	XA	60H	Write	XA	F1H

Note)

*1. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

*2. BUS operations are defined in 3. Truth Table.

*3. XA=Any valid address within the device.
IA=Identifier Code Address.
BA=Address within the block being erased.
WA=Address of memory location to be written.
SRD=Data read from status register.See the next section "Status Register Definition"
WD=Data to be written at location WA. Data is latched on the rising edge of F-$\overline{WE}$ or F-$\overline{BE}$ [F-$\overline{BE}_0$ .F-$\overline{BE}_1$] (whichever goes high first).
ID=Data read from identifier codes.

*4. See Identifier Codes at the next page.

*5. See Write Protection Alternatives at the next page.

*6. The clear block lock-bits operation simulatneoulsy clears all block lock-bits.

*7. If the permanent lock-bit is set, Set Block Lock-Bit and Clear Block Lock-Bits commands can not be done.

*8. Once the permanent lock-bit is set, it cannot be cleared.

Identifier Codes

Codes		Address $[A_{19}-A_0]$	Data $[DQ_{15}-DQ_0]$
Manufacture Code		00000H	00B0H
Device Code		00001H	00E1H
Block Lock Configuration	Unlocked	BA(*1)+2	DQ_0=0 (*2)
	locked	BA(*1)+2	DQ_0=1 (*2)
Permanent Lock Configuration	Unlocked	00003H	DQ_0=0 (*2)
	locked	00003H	DQ_0=1 (*2)

NOTE: 1. BA selects the specific block lock configuration code to be read.
2. $DQ_{15}-DQ_1$ are reserved for future use.

Write Protection Alternatives

Operation	F-V_{CCW}	F-$\overline{RP}$	Permanent Lock-Bit	Block Lock-Bit	F-$\overline{WP}$	Effect
Block Erase or Word Write	$\leqq V_{CCWLK}$	X	X	X	X	All Blocks Locked.
	$>V_{CCWLK}$	V_{IL}	X	X	X	All Blocks Locked.
		V_{IH}	X	0	V_{IL}	2 Boot Blocks Locked.
					V_{IH}	Block Erase and Word Write Enabled.
				1	V_{IL}	Block Erase and Word Write Disabled.
					V_{IH}	Block Erase and Word Write Disabled.
Bank Erase	$\leqq V_{CCWLK}$	X	X	X	X	All Blocks Locked.
	$>V_{CCWLK}$	V_{IL}	X	X	X	All Blocks Locked.
		V_{IH}	X	X	V_{IL}	All Unlocked Blocks are Erased. 2 Boot Blocks and Locked Blocks are NOT Erased.
					V_{IH}	All Unlocked Blocks are Earsed. Locked Blocks are NOT Erased.
Set Block Lock-Bit	$\leqq V_{CCWLK}$	X	X	X	X	Set Block Lock-Bit Disabled.
	$>V_{CCWLK}$	V_{IL}	X	X	X	Set Block Lock-Bit Disabled.
		V_{IH}	0	X	X	Set Block Lock-Bit Enabled.
			1	X	X	Set Block Lock-Bit Disabled.
Clear Block Lock-Bits	$\leqq V_{CCWLK}$	X	X	X	X	Clear Block Lock-Bits Disabled.
	$>V_{CCWLK}$	V_{IL}	X	X	X	Clear Block Lock-Bits Disabled.
		V_{IH}	0	X	X	Clear Block Lock-Bits Enabled.
			1	X	X	Clear Block Lock-Bits Disabled.
Set Permanent Lock-Bit	$\leqq V_{CCWLK}$	X	X	X	X	Set Permanent Lock-Bit Disabled.
	$>V_{CCWLK}$	V_{IL}	X	X	X	Set Permanent Lock-Bit Disabled.
		V_{IH}	X	X	X	Set Permanent Lock-Bit Enabled.

6. Status Register Definition

WSMS	BESS	ECBLBS	WWSLBS	VCCWS	WWSS	DPS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS(WSMS) 1 = Ready 0 = Busy	Check SR.7 to determine block erase, bank erase, word write or lock-bit configuration completion. SR.6-0 are invalid while SR.7="0".
SR.6 = BLOCK ERASE SUSPEND STATUS(BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS(ECBLBS) 1 = Error in Block Erase, Bank Erase or Clear Block Lock-Bits 0 = Successful Block Erase, Bank Erase or Clear Block Lock-Bits	If both SR.5 and SR.4 are "1"s after a block erase, bank erase or lock-bit configuration attempt, an improper command sequence was entered.
SR.4 = WORD WRITE AND SET LOCK-BIT STATUS (WWSLBS) 1 = Error in Word Write or Set Block /Permanent Lock-Bit 0 = Successful Word Write or Set Block /Permanent Lock-Bits	
SR.3 = V_{CCW} STATUS (VCCWS) 1 = V_{CCW} Low Detect, Operation Abort 0 = V_{CCW} OK	SR.3 does not provide a continuous indication of F-V_{CCW} level. The WSM interrogates and indicates the F-V_{CCW} level only after Block Erase, Bank Erase, Word Write or Lock-Bit Configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when F-V_{CCW}≠F-$V_{CCWH1/2}$.
SR.2 = WORD WRITE SUSPENDED STATUS (WWSS) 1 = Word Write Suspended 0 = Word Write in Progress/Completed	
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Block Lock-Bits, Permanent Lock-Bit and/or F-$\overline{WP}$ Lock Detected, Operation Abort 0 = Unlock	SR.1 does not provide a continuous indication of permanent and block lock-bit and F-$\overline{WP}$ values. The WSM interrogates the permanent lock-bit, block lock-bit and F-$\overline{WP}$ only after Block Erase, Bank Erase, Word Write or Lock-Bit Configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, permanent lock-bit is set and/or F-$\overline{WP}$ is F-V_{IL}. Reading the block lock and permanent lock configuration codes after writing the Read Identifier Codes command indicates permanent and block lock-bit status.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.

7. Memory Map for Flash Memory

Memory Map

Bottom Boot — Bank0 (F-$\overline{BE}_0$="L", F-$\overline{BE}_1$="H")

Address [A_{19}-A_0] (top)	Address [A_{19}-A_0] (bottom)	Block	No.
FFFFF	F8000	32K-word Main Block	30
F7FFF	F0000	32K-word Main Block	29
EFFFF	E8000	32K-word Main Block	28
E7FFF	E0000	32K-word Main Block	27
DFFFF	D8000	32K-word Main Block	26
D7FFF	D0000	32K-word Main Block	25
CFFFF	C8000	32K-word Main Block	24
C7FFF	C0000	32K-word Main Block	23
BFFFF	B8000	32K-word Main Block	22
B7FFF	B0000	32K-word Main Block	21
AFFFF	A8000	32K-word Main Block	20
A7FFF	A0000	32K-word Main Block	19
9FFFF	98000	32K-word Main Block	18
97FFF	90000	32K-word Main Block	17
8FFFF	88000	32K-word Main Block	16
87FFF	80000	32K-word Main Block	15
7FFFF	78000	32K-word Main Block	14
77FFF	70000	32K-word Main Block	13
6FFFF	68000	32K-word Main Block	12
67FFF	60000	32K-word Main Block	11
5FFFF	58000	32K-word Main Block	10
57FFF	50000	32K-word Main Block	9
4FFFF	48000	32K-word Main Block	8
47FFF	40000	32K-word Main Block	7
3FFFF	38000	32K-word Main Block	6
37FFF	30000	32K-word Main Block	5
2FFFF	28000	32K-word Main Block	4
27FFF	20000	32K-word Main Block	3
1FFFF	18000	32K-word Main Block	2
17FFF	10000	32K-word Main Block	1
0FFFF	08000	32K-word Main Block	0
07FFF	07000	4K-word Parameter Boot Block	5
06FFF	06000	4K-word Parameter Boot Block	4
05FFF	05000	4K-word Parameter Boot Block	3
04FFF	04000	4K-word Parameter Boot Block	2
03FFF	03000	4K-word Parameter Boot Block	1
02FFF	02000	4K-word Parameter Boot Block	0
01FFF	01000	4K-word Boot Block	1
00FFF	00000	4K-word Boot Block	0

Bottom Boot — Bank1 (F-$\overline{BE}_0$="H", F-$\overline{BE}_1$="L")

Address [A_{19}-A_0] (top)	Address [A_{19}-A_0] (bottom)	Block	No.
FFFFF	F8000	32K-word Main Block	30
F7FFF	F0000	32K-word Main Block	29
EFFFF	E8000	32K-word Main Block	28
E7FFF	E0000	32K-word Main Block	27
DFFFF	D8000	32K-word Main Block	26
D7FFF	D0000	32K-word Main Block	25
CFFFF	C8000	32K-word Main Block	24
C7FFF	C0000	32K-word Main Block	23
BFFFF	B8000	32K-word Main Block	22
B7FFF	B0000	32K-word Main Block	21
AFFFF	A8000	32K-word Main Block	20
A7FFF	A0000	32K-word Main Block	19
9FFFF	98000	32K-word Main Block	18
97FFF	90000	32K-word Main Block	17
8FFFF	88000	32K-word Main Block	16
87FFF	80000	32K-word Main Block	15
7FFFF	78000	32K-word Main Block	14
77FFF	70000	32K-word Main Block	13
6FFFF	68000	32K-word Main Block	12
67FFF	60000	32K-word Main Block	11
5FFFF	58000	32K-word Main Block	10
57FFF	50000	32K-word Main Block	9
4FFFF	48000	32K-word Main Block	8
47FFF	40000	32K-word Main Block	7
3FFFF	38000	32K-word Main Block	6
37FFF	30000	32K-word Main Block	5
2FFFF	28000	32K-word Main Block	4
27FFF	20000	32K-word Main Block	3
1FFFF	18000	32K-word Main Block	2
17FFF	10000	32K-word Main Block	1
0FFFF	08000	32K-word Main Block	0
07FFF	07000	4K-word Parameter Boot Block	5
06FFF	06000	4K-word Parameter Boot Block	4
05FFF	05000	4K-word Parameter Boot Block	3
04FFF	04000	4K-word Parameter Boot Block	2
03FFF	03000	4K-word Parameter Boot Block	1
02FFF	02000	4K-word Parameter Boot Block	0
01FFF	01000	4K-word Boot Block	1
00FFF	00000	4K-word Boot Block	0

8. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (*1)	V_{CC}	−0.2 to +4.6	V
Input voltage (*1, 2)	V_{IN}	−0.2 (*3) to 3.9	V
Operating temperature	T_{opr}	−25 to +85	℃
Storage temperature	T_{stg}	−65 to 125	℃
F-V_{CCW} voltage (*1)	F-V_{CCW}	−0.3 (*3) to +4.6	V

Notes) *1. The maximum applicable voltage on any pins with respect to GND.
*2. Except F-V_{CC}, F-V_{CCW}.
*3. −2.0V undershoot is allowed when the pulse width is less than 20nsec.

9. Recommended DC Operating Conditions

(T_a= −25℃ to +85 ℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
Input voltage	V_{IH}	2.0		V_{CC}+0.2 (*1)	V
	V_{IL}	−0.2 (*2)		0.4	V

Notes) *1. V_{CC} is the lower one of S-V_{CC} and F-V_{CC} .
*2. −2.0V undershoot is allowed when the pulse width is less than 20nsec.

10. Pin Capacitance

(T_a=25℃, f=1MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	V_{IN}=0V			30	pF	*1
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V			34	pF	*1

Note) *1 Sampled but not 100% tested

11.DC Characteristics

DC Characteristics (T_a= −25℃ to +85℃, V_{CC}= 2.7 V to 3.6 V)

Parameter		Symbol	Conditions	Min.	Typ. (*1)	Max.	Unit
Input leakage current (I_{LI})		I_{LI}	V_{IN} = V_{CC} or GND	−2		+2	μA
Output leakage current (I_{LO})		I_{LO}	V_{OUT} = V_{CC} or GND	−2		+2	μA
F-V_{CC}	V_{CC} Standby Current	I_{CCS} (*3)	F-$\overline{BE}$=F-$\overline{RP}$=F-V_{CC} ±0.2V F-$\overline{WP}$=F-V_{CC} ±0.2V or F-GND±0.2V		4	20	μA
			F-$\overline{BE}$=F-$\overline{RP}$=V_{IH} F-$\overline{WP}$=V_{IH} or V_{IL}		0.4	4	mA
	Auto Power-Save Current	I_{CCAS} (*2,3)	F-$\overline{BE}$=GND±0.2V		4	20	μA
	Reset Power-Down Current	I_{CCD}	F-$\overline{RP}$=F-GND±0.2V, I_{OUT}(F-RY/$\overline{BY}$)=0mA		4	20	μA
	V_{CC} Read Current	I_{CCR} (*3)	CMOS Input F-$\overline{BE}$=F-GND, f=5MHz, I_{OUT} =0mA		15	25	mA
			TTL Input F-$\overline{BE}$=F-GND, f=5MHz, I_{OUT} =0mA			30	mA
	V_{CC} Word Write or Set Lock-Bit Current	I_{CCW}	F-V_{CCW} = V_{CCWH}		5	17	mA
	V_{CC} Block Erase, Bank Erase or Clear Block Lock-Bits Current	I_{CCE}	F-V_{CCW} = V_{CCWH}		4	17	mA
	V_{CC} Word Write Block Erase Suspend Current	I_{CCWS} I_{CCES}	F-$\overline{BE}$=V_{IH}		1	6	mA
F-V_{CCW}	V_{CCW} Standby or Read Current	I_{CCWS}	F-V_{CCW} = F-V_{CC}		±4.0	±20	μA
		I_{CCWR}	F-V_{CCW} > F-V_{CC}		10	200	μA
	V_{CCW} Auto Power-Save Current	I_{CCWAS} (*2,3)	F-$\overline{BE}$=GND±0.2V		0.2	5	μA
	V_{CCW} Reset Power-Down Current	I_{CCWD}	F-$\overline{RP}$=F-GND±0.2V		0.2	5	μA
	V_{CCW} Word Write or Set Lock-Bit Current	I_{CCWW}	F-V_{CCW} = V_{CCWH}		12	40	mA
	V_{CCW} Block Erase, Bank Erase or Clear Block Lock-Bits Current	I_{CCWE}	F-V_{CCW} = V_{CCWH}		8	25	mA
	V_{CCW} Word Write or Block Erase Suspend Current	I_{CCWWS} I_{CCWES}	F-V_{CCW} = V_{CCWH}		10	200	μA
S-V_{CC}	Standby Current	I_{SB}	S-$\overline{CE}_1$, S-CE_2≧S-V_{CC}−0.2V or S-CE_2≦0.2V		1.0	15	μA
		I_{SB1}	S-$\overline{CE}_1$=V_{IH} or S-CE_2=V_{IL}			3	mA
	Operation Current	I_{CC1}	S-$\overline{CE}_1$=V_{IL}, S-CE_2=V_{IH} V_{IN}=V_{IL} or V_{IH} / t_{CYCLE}=Min. $I_{I/O}$=0mA			45	mA
		I_{CC2}	S-$\overline{CE}_1$=0.2V, S-CE_2=S-V_{CC}−0.2V V_{IN}=S-V_{CC}−0.2V or 0.2V / t_{CYCLE}=1μs $I_{I/O}$=0mA			8	mA

DC Characteristics (Continue) (T_a= −25℃ to +85℃ , V_{CC}= 2.7 V to 3.6 V)

Parameter	Symbol	Test Conditions	Min.	Typ. (*1)	Max.	Unit
Input Low Voltage	V_{IL}		−0.2		0.4	V
Input High Voltage	V_{IH}		2.0		V_{CC}+0.2	V
Output Low Voltage	V_{OL}	I_{OL} =0.5mA			0.4	V
Output High Voltage (CMOS)	V_{OH1}	I_{OH} =−0.5mA	2.0			V
F-V_{CCW} Lockout during Normal Operations	V_{CCWLK} (*4)				1.5	V
F-V_{CCW} during Block Erase, Bank Erase, Word Write or Lock-Bit Configuration Operations	V_{CCWH}		2.7		3.6	V
F-V_{CC} Lockout Voltage	V_{LKO}		2.0			V

Notes)

1. Reference values at V_{CC}=3.0V and T_a =+25°C.
2. The Automatic Power Savings (APS) feature is placed automatically power save mode that addresses not switching more than 300ns while read mode.
3. CMOS inputs are either V_{CC} ±0.2V or GND±0.2V. TTL inputs are either V_{IL} or V_{IH}.
4. Block erases, bank erases, word writes and lock-bits configurations are inhibited when F-V_{CCW} ≦V_{CCWLK} and not guaranteed in the range between V_{CCWLK} (Max) and V_{CCWH} (Min), and above V_{CCWH} (Max).

12. Flash memory AC Characteristics

AC Test Condtions

Input pulse level	0 V to 2.7 V
Input rise and fall time	10 ns
Input and Output timing Ref. level	1.35 V
Output load	1TTL+C_L (50pF)

Read Cycle (T_a= −25℃ to +85℃, V_{CC}= 2.7V to 3.6 V)

Parameter	Sym.	Min.	Max.	Unit	
Read Cycle Time	t_{AVAV}	90		ns	
Address to Output Delay	t_{AVQV}		90	ns	
F-$\overline{BE}$ to Output Delay	t_{ELQV}		90	ns	*1
F-$\overline{RP}$ High to Output Delay	t_{PHQV}		600	ns	
F-$\overline{OE}$ to Output Delay	t_{GLQV}		55	ns	*1
F-$\overline{BE}$ to Output in Low Z	t_{ELQX}	0		ns	
F-$\overline{BE}$ High to Output in High Z	t_{EHQZ}		55	ns	
F-$\overline{OE}$ to Output in Low Z	t_{GLQX}	0		ns	
F-$\overline{OE}$ High to Output in High Z	t_{GHQZ}		30	ns	
Output Hold from Address, F-$\overline{BE}$ or F-$\overline{OE}$ Change, Whichever Occurs First	t_{OH}	0		ns	

Notes)

*1. F-$\overline{OE}$ may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of F-$\overline{BE}_0$ or F-$\overline{BE}_1$ without impact on t_{ELQV}.

Write Cycle (F-$\overline{WE}$ Controlled) (*2) (T_a= −25℃ to +85℃, V_{CC}=2.7 V to 3.6 V)

Parameter	Sym.	Min.	Max.	Unit	
Write Cycle Time	t_{AVAV}	90		ns	
F-$\overline{RP}$ High Recovery to F-$\overline{WE}$ going to Low	t_{PHWL}	1		μs	
F-$\overline{BE}$ Setup to F-$\overline{WE}$ Going Low	t_{ELWL}	15		ns	
F-$\overline{WE}$ Pulse Width	t_{WLWH}	60		ns	
F-$\overline{WP}$ V_{IH} Setup to F-$\overline{WE}$ Going High	t_{SHWH}	115		ns	
F-V_{CCW} Setup to F-$\overline{WE}$ Going High	t_{VPWH}	115		ns	
Address Setup to F-$\overline{WE}$ Going High	t_{AVWH}	60		ns	*3
Data Setup to F-$\overline{WE}$ Going High	t_{DVWH}	60		ns	*3
Data Hold from F-$\overline{WE}$ High	t_{WHDX}	5		ns	
Address Hold from F-$\overline{WE}$ High	t_{WHAX}	5		ns	
F-$\overline{BE}$ Hold from F-$\overline{WE}$ High	t_{WHEH}	10		ns	
F-$\overline{WE}$ Pulse Width High	t_{WHWL}	20		ns	
Write Recovery before Read	t_{WHGL}	5		ns	
F-V_{CCW} Hold from Valid SRD	t_{QVVL}	0		ns	
F-$\overline{WP}$ V_{IH} Hold from Valid SRD	t_{QVSL}	0		ns	

Write Cycle (F-$\overline{BE}$ Controlled) (*4)

(T_a= −25℃ to +85℃ , V_{CC}= 2.7 V to3.6 V)

Parameter	Sym.	Min.	Max.	Unit	
Write Cycle Time	t_{AVAV}	90		ns	
F-$\overline{RP}$ High Recovery to F-$\overline{BE}$ going to Low	t_{PHEL}	1		μs	
F-$\overline{WE}$ Setup to F-$\overline{BE}$ Going Low	t_{WLEL}	0		ns	
F-$\overline{BE}$ Pulse Width	t_{ELEH}	70		ns	
F-$\overline{WP}$ V_{IH} Setup to F-$\overline{BE}$ Going High	t_{SHEH}	115		ns	
F-V_{CCW} Setup to F-$\overline{BE}$ Going High	t_{VPEH}	115		ns	
Address Setup to F-$\overline{BE}$ Going High	t_{AVEH}	60		ns	*3
Data Setup to F-$\overline{BE}$ Going High	t_{DVEH}	60		ns	*3
Data Hold from F-$\overline{BE}$ High	t_{EHDX}	5		ns	
Address Hold from F-$\overline{BE}$ High	t_{EHAX}	5		ns	
F-$\overline{WE}$ Hold from F-$\overline{BE}$ High	t_{EHWH}	0		ns	
F-$\overline{BE}$ Pulse Width High	t_{EHEL}	25		ns	
Write Recovery before Read	t_{EHGL}	5		ns	
F-V_{CCW} Hold from Valid SRD	t_{QVVL}	0		ns	
F-$\overline{WP}$ V_{IH} Hold from Valid SRD	t_{QVSL}	0		ns	

Notes) *2. Read timing caracteristics during block erase , bank erase , word write and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.

*3. Refer to Section 5. Flash Memory Command Definition for valid AIN and DIN for block erase, bank erase, word write or lock-bit configuration.

*4. In system where F-$\overline{BE}$ defines the pulse width (within a longer F-$\overline{WE}$ timing waveform), all setup, hold, and inactive F-$\overline{WE}$ times should be measured relative to the F-$\overline{BE}$ waveform.

Block Erase, Bank Erase, Word Write and Lock-Bits Configuration Performance

(T_a= −25℃ to +85 ℃ , V_{CC}= 2.7 V to 3.6 V)

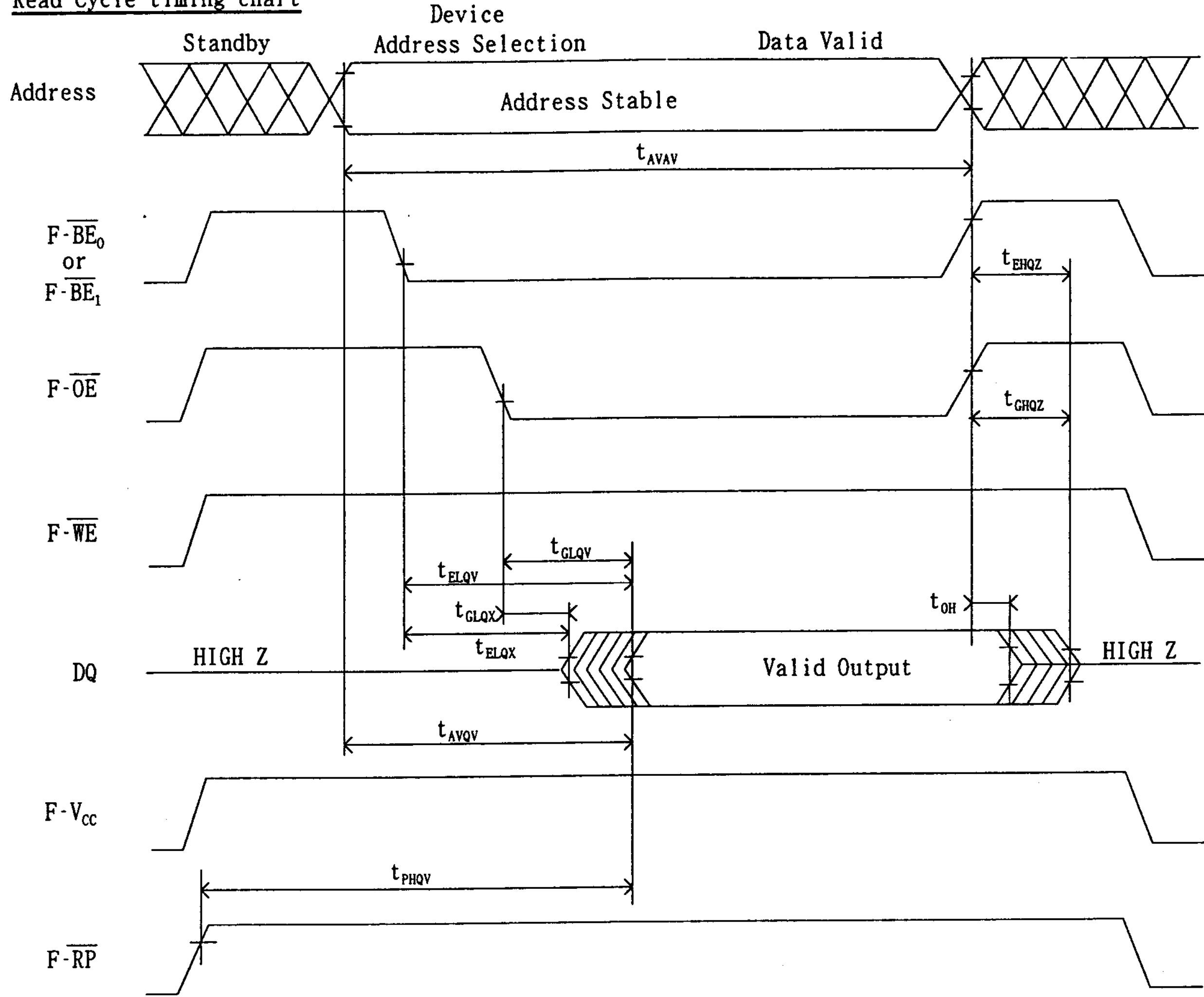
Sym.	Parameter		V_{CCW}= 2.7 V to 3.6 V Typ. (*4)	Max.	Unit	
t_{WHQV1} t_{EHQV1}	Word Write Time	32K-word Block	33	200	μs	*5
		4K-word Block	36	200	μs	*5
	Block Write Time	32K-word Blcok	1.1	4	s	*5
		4K-word Block	0.15	0.5	s	*5
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K-word Block	1.2	6	s	*5
		4K-word Block	0.6	5	s	*5
	Bank Erase Time		42.0	210	s	*5
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time		56	200	μs	*5
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time		1	5	s	*5
t_{WHRZ1} t_{EHRZ1}	Word Write Suspend Latency Time to Read		6.0	15.0	μs	
t_{WHRZ2} t_{EHRZ2}	Erase Suspend Latency Time to Read		16.0	30.0	μs	

Notes) *4. Reference values at T_a= +25℃ and V_{CC}=3.0V, V_{CCW}=3.0V. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.

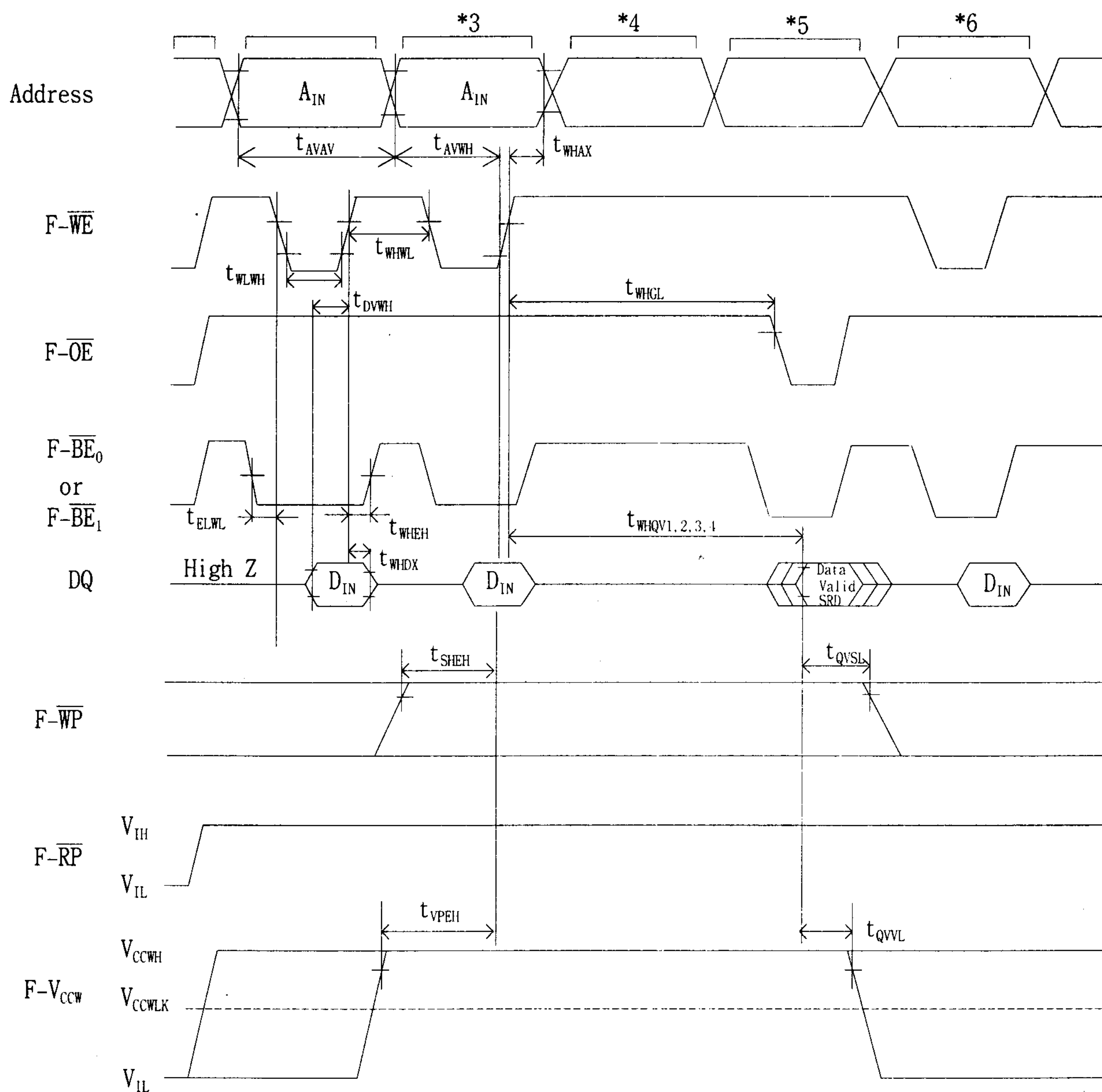
*5. Excludes system-level overhead.

Flash Memory AC Characteristics Timing Chart

Read Cycle timing chart

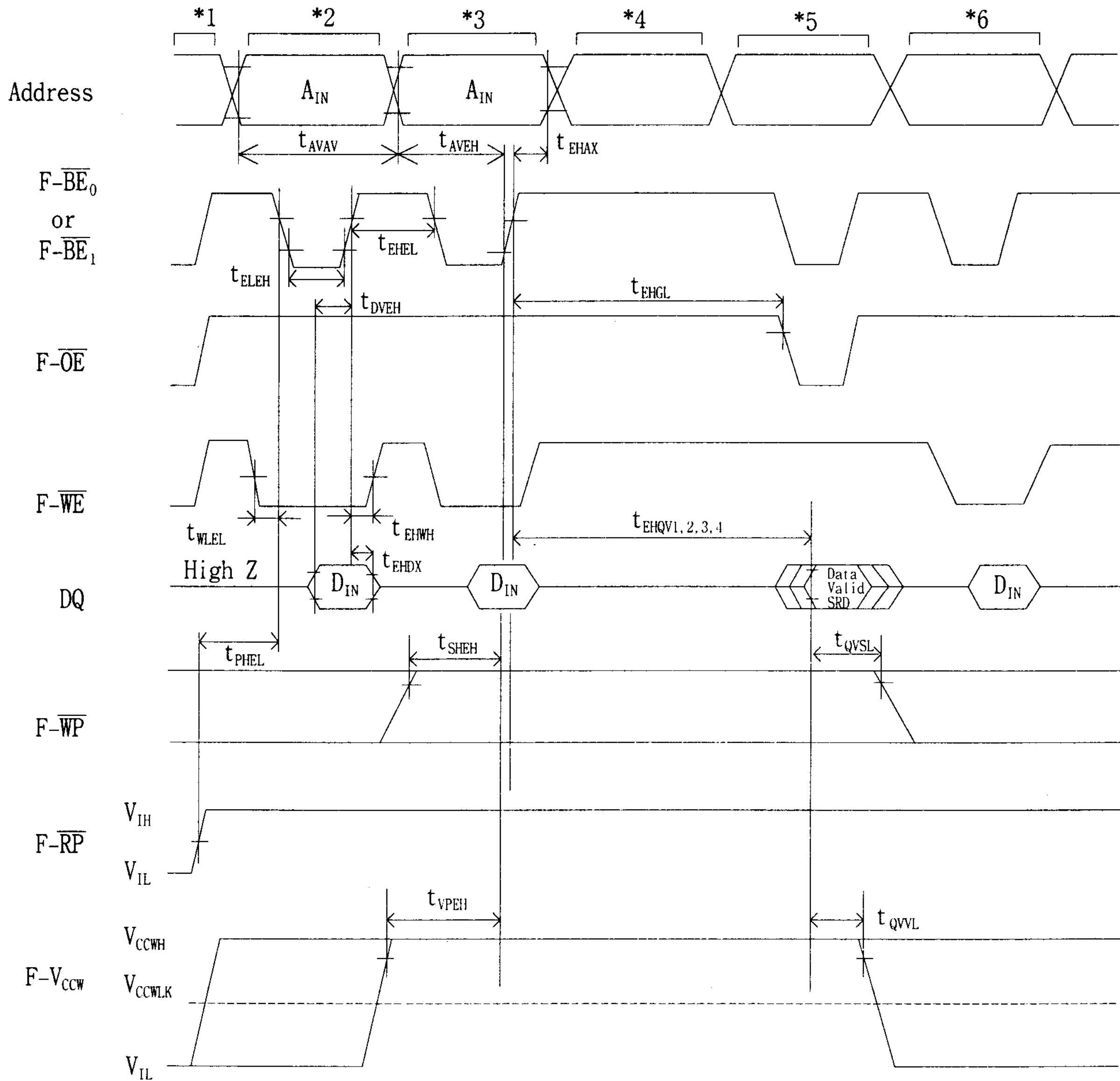


Write cycle timing chart (F-$\overline{WE}$ Controlled)



NOTES:
*1. V_{CC} power-up and standby.
*2. Write each setup command.
*3. Write each comfirm command or valid address and data.
*4. Automated erase or program delay.
*5. Read status register data.
*6. Write Read Array command.

Write cycle timing chart (F-$\overline{BE}$ controlled)



NOTES:
*1. V_{CC} power-up and standby.
*2. Write each setup command.
*3. Write each comfirm command or valid address and data.
*4. Automated erase or program delay.
*5. Read status register data.
*6. Write Read Array command.

Reset Operations (T_a= −25℃ to +85℃ , V_{CC}= 2.7V to 3.6V)

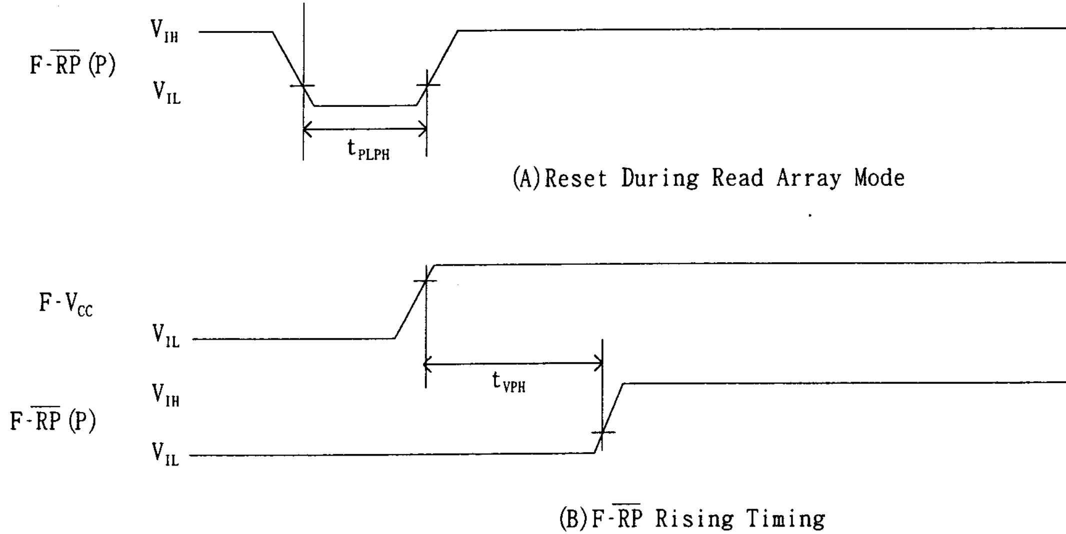
Parameter	Sym.	Min.	Max.	Unit	
F-$\overline{RP}$ Pulse Low Time (If F-$\overline{RP}$ is tied to Vcc, this specification is not applicable.)	t_{PLPH}	100		ns	
F-$\overline{RP}$ Low to Reset during Block Erase, Bank Erase, Word Write or Lock-bit Configuration *1	t_{PLRZ}		30	μs	*2
F-V_{CC} 2.7V to F-$\overline{RP}$ High	t_{VPH}	100		ns	*3

Notes) *1. If F-$\overline{RP}$ is asserted while a block erase, bank erase, word write or lock-bit configuration operation is not executing, the reset will complete with 100ns.

*2. A reset time, t_{PHQV}, is required from the later of F-$\overline{RP}$ going high until outputs are valid.

*3. When the device power-up, holding F-$\overline{RP}$ low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation



(A)Reset During Read Array Mode

(B)F-$\overline{RP}$ Rising Timing

13. SRAM AC Electrical Characteristics

SRAM AC Test Conditions

Input pulse level	0.4 V to 2.2 V
Input rise and fall time	5 ns
Input and Output timing Ref. level	1.5 V
Output load	1TTL+C_L (30pF) (*1)

Note) *1. Including scope and jig capacitance.

Read Cycle

(T_a= −25 ℃ to +85 ℃ , V_{CC}= 2.7 V to 3.6 V)

Parameter	Sym.	Min.	Max.	Unit	
Read Cycle Time	t_{RC}	85		ns	
Address access time	t_{AA}		85	ns	
Chip enable access time (S-$\overline{CE_1}$)	t_{ACE1}		85	ns	
(S-CE_2)	t_{ACE2}		85	ns	
Byte enable access time	t_{BE}		85	ns	
Output enable to output valid	t_{OE}		45	ns	
Output hold from address change	t_{OH}	15		ns	
S-$\overline{CE_1}$, S-CE_2 Low (S-$\overline{CE_1}$)	t_{LZ1}	10		ns	*2
to output active (S-CE_2)	t_{LZ2}	10		ns	*2
S-$\overline{OE}$ Low to output active	t_{OLZ}	5		ns	*2
S-$\overline{UB}$ or $\overline{LB}$ Low to output in High impedance	t_{BLZ}	10		ns	*2
S-$\overline{CE_1}$, S-CE_2 High to (S-$\overline{CE_1}$)	t_{HZ1}	0	25	ns	*2
output in High impedance (S-CE_2)	t_{HZ2}	0	25	ns	*2
S-$\overline{OE}$ High to output in High impedance	t_{OHZ}	0	25	ns	*2
S-$\overline{UB}$ or $\overline{LB}$ High to output active	t_{BHZ}	0	25	ns	*2

Write Cycle

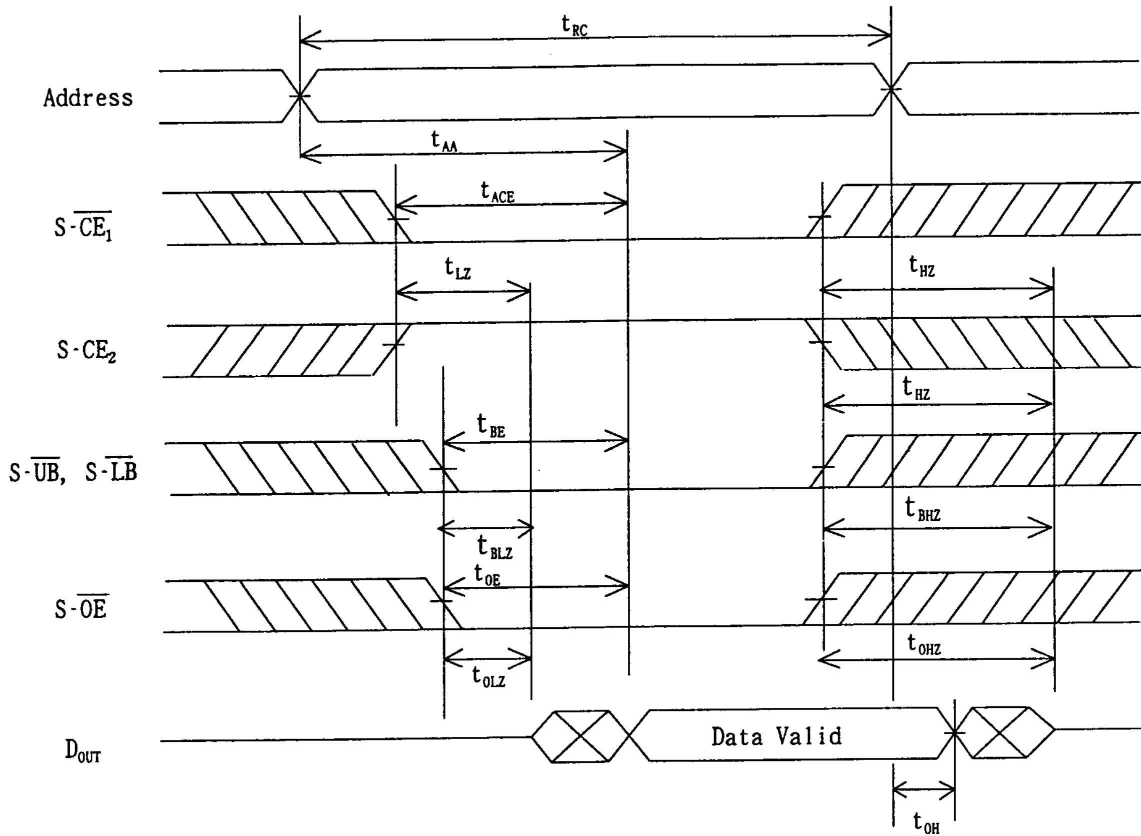
(T_a= −25 ℃ to +85 ℃ , V_{CC}=2.7 V to 3.6 V)

Parameter	Sym.	Min.	Max.	Unit	
Write cycle time	t_{WC}	85		ns	
Chip enable to end of write	t_{CW}	70		ns	
Address valid to end of write	t_{AW}	70		ns	
Byte select time	t_{BW}	70		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	60		ns	
Write recovery time	t_{WR}	0		ns	
Input data setup time	t_{DW}	35		ns	
Input data hold time	t_{DH}	0		ns	*2
S-$\overline{WE}$ High to output active	t_{OW}	5		ns	*2
S-$\overline{WE}$ Low to output in High impedance	t_{WZ}	0	25	ns	

*2. Active output to High impedance and High impedance to output active tests specified for a ±200mV transition from steady state levels into the test load.

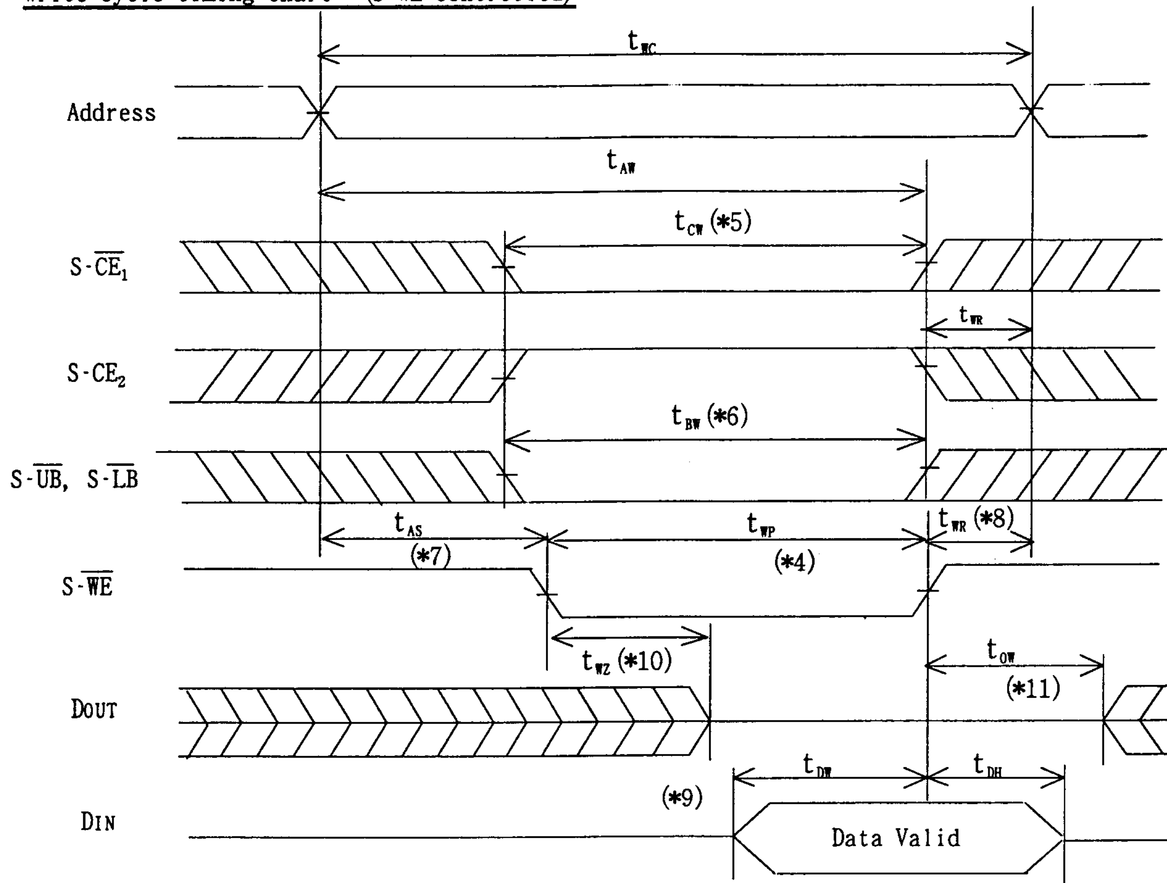
SRAM AC Charaterestics Timing Chart

Read cycle timing chart — (*3)

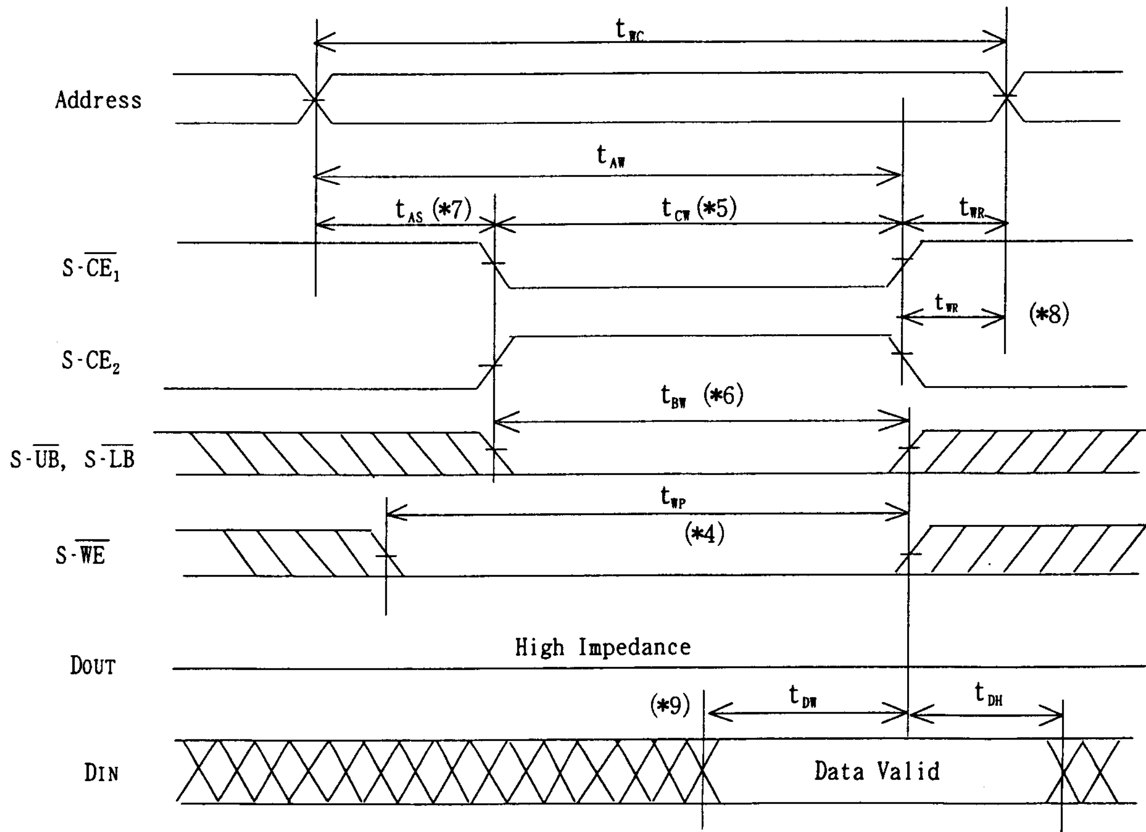


*3 S-WE is high for Read cycle.

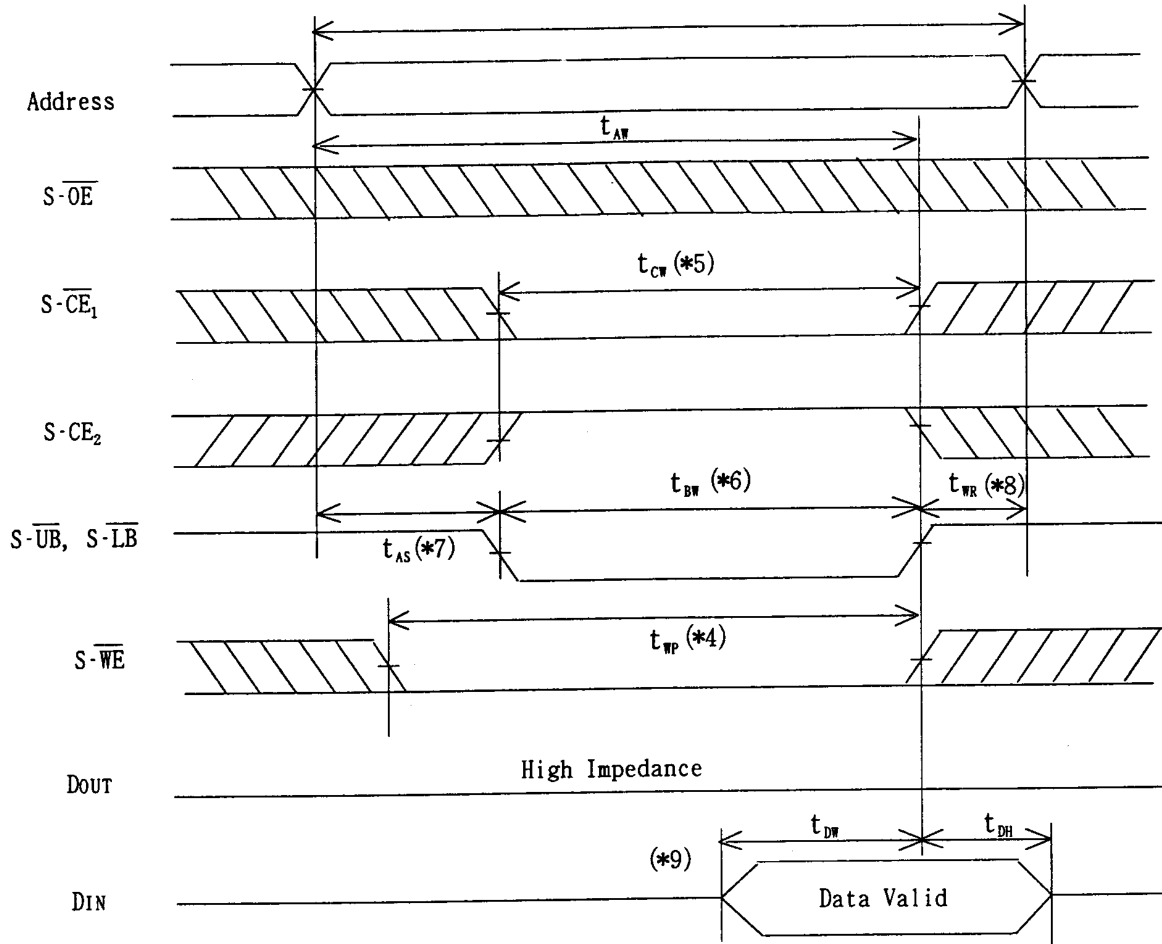
Write cycle timing chart — (S-$\overline{WE}$ Controlled)



Write cycle timing chart — (S-$\overline{CE}$ Controlled)



Write cycle timing chart (S-$\overline{UB}$, S-$\overline{LB}$ control)



Notes:

*4. A write occurs during the overlap of a low S-$\overline{CE_1}$, a high S-CE_2 and a low S-$\overline{WE}$,
A write begins at the latest transition among S-$\overline{CE_1}$ going low, S-CE_2 going high and S-$\overline{WE}$ going low.
A write ends at the earliest transition among S-$\overline{CE_1}$ going high, S-CE_2 going low and S-$\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

*5. t_{CW} is measured from the later of S-$\overline{CE_1}$ going low or S-CE_2 going high to the end of write.

*6. t_{BW} is measured from the time of going low S-$\overline{UB}$ or low S-$\overline{LB}$ to the end of write.

*7. t_{AS} is measured from the address valid to the beginning of write.

*8. t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at S-$\overline{CE_1}$ or S-$\overline{WE}$ going high. t_{WR2} applies in case a write ends at S-CE2 going low.

*9. During this period, DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

*10. If S-$\overline{CE_1}$ goes low or S-CE_2 goes high simultaneously with S-$\overline{WE}$ going low or after S-$\overline{WE}$ going low, the outputs remain in high impedance state.

*11. If S-$\overline{CE_1}$ goes high or S-CE $_2$ goes low simultaneously with S-$\overline{WE}$ going high or S-$\overline{WE}$ going high, the outputs remain in high impedance state.

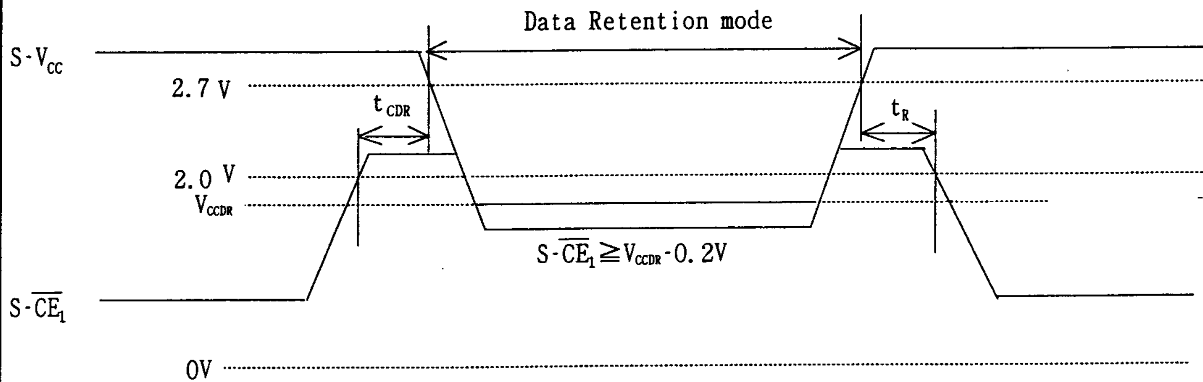
14. SRAM Data Retention Characteristics

(T_a= −25 ℃ to +85 ℃)

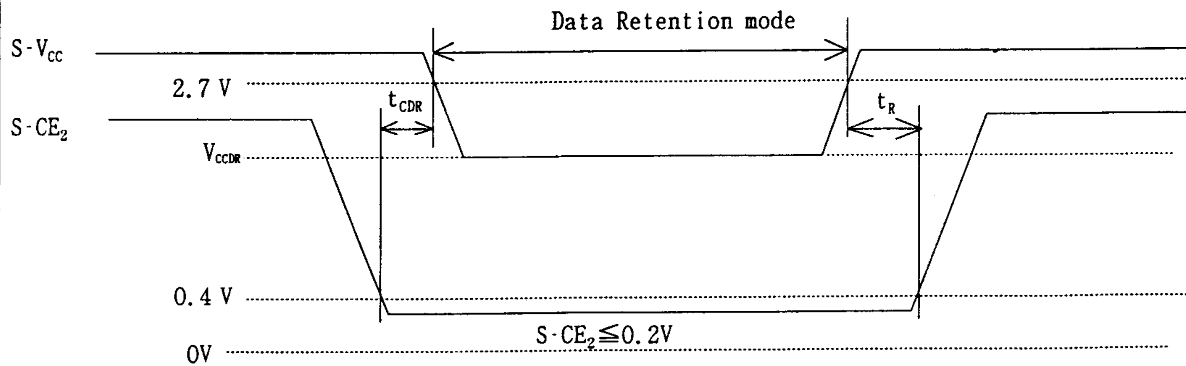
Parameter	Sym.	Conditions	Min.	Typ. (*1)	Max.	Unit
Data Retention Supply volotage	V_{CCDR}	S-CE_2 ≦0.2V or S-$\overline{CE_1}$≧V_{CCDR}-0.2V (*2)	1.5		3.6	V
Data Retention Supply current	I_{CCDR}	V_{CCDR}=3.0V S-CE_2≦0.2V or S-$\overline{CE_1}$ ≧V_{CCDR}-0.2V (*2)		1.0	15	μA
Chip enable setup time	t_{CDR}		0			ns
Chip enable hold time	t_R		t_{RC}			ns

Notes) *1. Reference value at T_a=25℃, S-V_{CC}=3.0V.
*2. S-$\overline{CE_1}$≧V_{CC}-0.2V, S-CE_2≧V_{CC}-0.2V (S-$\overline{CE_1}$ controlled) or S-CE_2≦0.2V (S-CE_2 controlled)

Data Retention timing chart (S-$\overline{CE_1}$ Controlled) (*3)



Data Retention timing chart (S-CE_2 Controlled)



Note) *3. To control the data retention mode at S-$\overline{CE_1}$, fix the input level of S-CE_2 between V_{CCDR} and V_{CCDR}-0.2V or 0V or 0.2V and during the data retetion mode.

15. Notes

This product is a stacked CSP package that a 32M (x16) bit Flash Memory and a 4M (x16) bit SRAM are assembled into.

Supply Power

Maximum difference (between F-V_{CC} and S-V_{CC}) of the voltage is less than 0.3V.

Power Supply and Chip Enable of Flash Memory and SRAM

S-$\overline{CE_1}$ should not be LOW and S-CE_2 should not be HIGH when F-$\overline{BE_0}$ or F-$\overline{BE_1}$ is LOW simultaneously.

If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.

Both F-V_{CC} and S-V_{CC} are needed to be applied by the recommended supply voltage at the same time except SRAM data retention mode.

Power UP Sequence

When turning on Flash memory power supply, keep F-$\overline{RP}$ LOW. After F-V_{CC} reaches over 2.7V, keep F-$\overline{RP}$ LOW for more than 100nsec.

Device Decoupling

The power supply is needed to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals(F-$\overline{BE_0}$, F-$\overline{BE_1}$, S-$\overline{CE_1}$, S-CE_2).

16. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems.
Such noises, when induced onto F-$\overline{WP}$ signal or power supply may be interpreted as false commands, causing undesired memory updating.
To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

1) Protecting data in specific block
By setting a F-$\overline{WP}$ to low, only the boot block can be protected against overwriting.
Parameter and main blocks cannot be locked.
System program, etc., can be locked by storing them in the boot block.
When a high voltage is applied to F-$\overline{RP}$, overwrite operation is enabled for all blocks.
For further information on setting/resetting of block bit, and controlling of F-$\overline{WP}$ and F-$\overline{RP}$, refer to the specification. (See 5. Command Definitions P.5)

2) Data protection through F-V_{CCW}
When the level of F-V_{CCW} is lower than V_{CCWLK} (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected.
For the lockout voltage, refer to the specification. (See Chapter 11. DC Characteristics P.10)

Data protection during voltage transition
1) Data protection thorough F-$\overline{RP}$
When the F-$\overline{RP}$ is kept low during power up and power down sequence, write operation on the flash memory is disabled, write protecting all blocks.
For the details of F-$\overline{RP}$ control, refer to the specification. (See chapter 12. Flash Memory AC Electrical Characteristics)

17. Design Considerations

1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory power switching characteristics, each device should have a 0.1μF ceramic capacitor connected between its F-V_{CC} and GND and between its F-V_{CCW} and GND. Low inductance capacitors should be placed as close as possible to package leads.

2. F-V_{CCW} Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{CCW} Power Supply trace. Use similar trace widths and layout considerations given to the V_{CC} power bus.

3. The Inhibition of Overwrite Operation

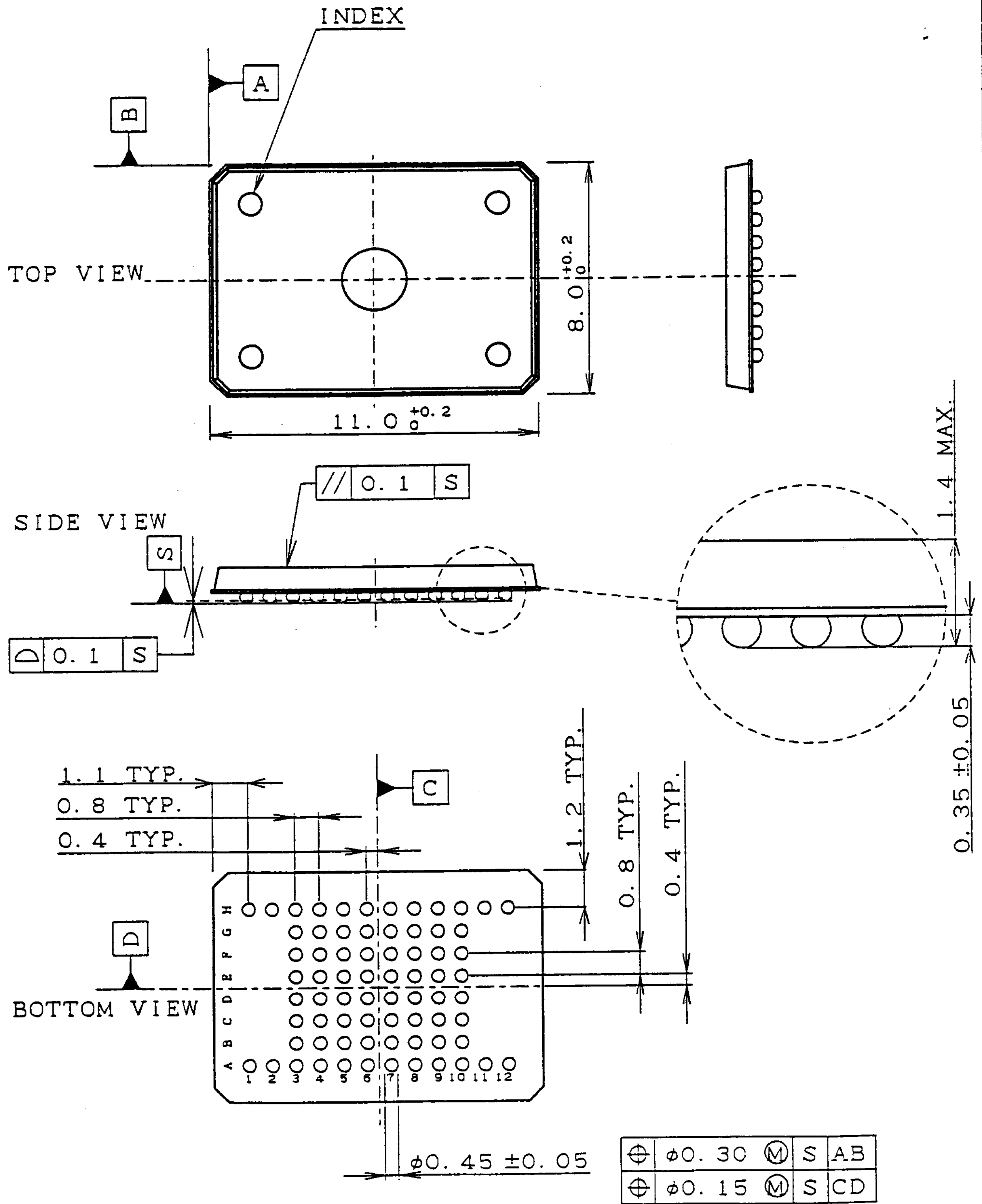
Please do not execute reprogramming "0" for the bit which has already been programed "0". Overwrite operation may generate unerasable bit.
In case of reprogramming "0" to the data which has been programed "1".

- Program "0" for the bit in which you want to change data from "1" to "0".
- Program "1" for the bit which has already been programmed "0".

For example, changing data from "1011110110111101" to "1010110110111100" requires "1110111111111110" programming.

4. Power Supply

Block erase, bank erase, word write and lock-bit configuration with an invalid F-V_{CCW}(See 11. DC Characteristics) produce spurious results and should not be attempted.
Device operations at invalid F-Vcc voltage(see 11.DC Characteristics) produce spurious results and should not be attempted.



改訂日 DATE	改訂記事 REVISE	担当 CHARGE	尺度 SCALE	単位 UNIT	適用機種 APPLICABLE MODEL	16M FLASH MEMORY(X16BB) +2M SRAM (X8)
			5/1	1=1/1mm		
			端子マトリクス MATRIX	12 X 8	名称 NAME	LCSP072-P-0811 (LFBGA072-P-0811)
			端子数 COUNTS	72		
日付 DATE	1998. 2. 10		端子ピッチ PITCH	0.8	コード CODE	LCSP-GR-072-1-0811
設計 DESIGN: SOTA	製図 DRAW: SOTA	写図 TRACE / 検図 CHECK / 承認 APPROVE	シャープ株式会社 SHARP CORPORATION		図番 DRAWING No.	AA2078
			IC天理事業本部 TENRI IC GROUP			
			超LSI開発研究所 VLSI DEVELOPMENT LABORATORIES			
			生産技術開発部 PRODUCTION ENGINEERING DEPT.			

SRAM, Flash Memory, Memory ICs, Stacked Chip Combo Chips Combination Chip Stack Chip