Ordering number : ENN*6698

CMOS IC

LC865632/28/24/20/16/12/08A

8-Bit Single Chip Microcontroller

Preliminary

Overview

The LC865632A/28A/24A/20A/16A/12A/08A microcontrollers are 8-bit single chip microcontrollers with the following on-chip functional blocks :

- CPU : Operable at a minimum bus cycle time of 0.5µs (microsecond)
- On-chip ROM maximum capacity : 32K bytes
- On-chip RAM capacity : 640 bytes (LC865632A/28A/24A)
  : 512 bytes (LC865620A/16A/12A/08A)
- 16-bit timer/counter (or two 8-bit timers)
- 16-bit timer/ PWM (or two 8-bit timers)
- 8-channel × 8-bit AD converter
- Two 8-bit synchronous serial-interface circuits
- 13-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

(1) Read Only Memory (ROM)

: LC865632A	32512 × 8 bits
: LC865628A	28672 × 8 bits
: LC865624A	24576 × 8 bits
: LC865620A	20480 × 8 bits
: LC865616A	16384 × 8 bits
: LC865612A	12288 × 8 bits
: LC865608A	8192 × 8 bits

(2) Random Access Memory (RAM)

: LC865632A/28A/24A	640 × 8 bits
: LC865620A/16A/12A/08A	512 × 8 bits

(3) Bus Cycle Time / Instruction Cycle Time

The LC865632A/28A/24A/20A/16A/12A/08A are constructed to read ROM twice within one instruction cycle. It has 1.7 times more performance capability within the same instruction cycle compared to our 4-bit microcontrollers (LC66000 series).

Bus cycle time indicates the speed to read ROM.

Bus cycle time	cycle time	System clock oscillation	Oscillation Frequency	Voltage
0.5µs	1.0µs	Ceramic resonator oscillation	6MHz	4.5 - 6.0V
2.0µs	4.0µs	Ceramic resonator oscillation	1.5MHz	2.5 - 6.0V
3.75µs	7.5µs	RC resonator oscillation	800MHZ	2.5 - 6.0V
91.5µs	183µs	Crystal oscillation	32.568kHz	2.5 - 6.0V

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

(4) Ports

- Input / output ports	: 6 ports	(42 terminals)
Input/output port programmable in nibble units	: 1 port	(8 terminals)
(When the N-channel open drain output is selected, the data in a bit can be inputted.)		
Input/output port programmable in a bit	: 5 ports	(34 terminals)
Include 15V withstand N-channel open drain output port	: 3 ports	(18 terminals)
- Input ports	: 2 ports	(13 terminals)

(5) AD converter
- 8 channels × 8-bit AD converters

(6) Serial-interface
- Two 8-bit serial-interface circuits
  LSB first / MSB first function available
- Internal 8-bit baud-rate generator in common with two serial-interface circuits

(7) Timers
- Timer0
  16-bit timer / counter
  2-bit prescaler + 8-bit programmable prescaler
  Mode 0 : Two 8-bit timers with programmable prescaler
  Mode 1 : 8-bit timer with a programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with a programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of Timer is 1 tCYC. (tCYC : cycle time)

- Timer 1
  16-bit timer / PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable-bit PWM (9-16 bits)
  In Mode 0 and Mode 1, the resolution of Timer and PWM is tCYC.
  In Mode 2 and Mode 3, the resolution of Timer and PWM selectable ; tCYC or 1/2tCYC by program
- Base timer
  Every 500ms overflow system for a clock application (using 32.568kHz crystal oscillation for Base timer clock)
  Every 976μs, 3.9ms, 15.6ms, 62.5ms overflow system (using 32.568kHz crystal oscillation for Base timer clock)
  The Base timer clock selectable ; 32.568kHz crystal oscillation, System clock, and programmable prescaler output of Timer 0

(8) Buzzer output
- The Buzzer sound frequency selectable ; 4KHz, 2KHz (using 32.568kHz crystal oscillation for Base timer clock)

(9) Remote control receiver circuit (Shares with the P73/INT3/T0IN terminal)
- Noise rejection function
- Switch polarity function

(10) Watchdog timer
- The watchdog timer is taken on RC outside
  - Watchdog timer operation selectable : interrupt system, system reset

(11) Interrupts system
- 13-sources 10-vectored interrupts :
  1. External interrupt INT0 (include watchdog timer)
  2. External interrupt INT1
  3. External interrupt INT2, timer / counter T0L (Lower 8 bits)
  4. External interrupt INT3, base timer
  5. Timer / counter T0H (Upper 8-bit)
  6. Timer T1L, Timer T1H
  7. Serial interface SIO0
  8. Serial interface SIO1
  9. AD converter
  10. Port 0
- Built-in interrupt priority control register

  Microcontroller allows 3 levels of interrupt; low level, high level, and highest level of multiplex interrupt. It can specify a low level or a high level interrupt priority from INT2/T0L through port 0 (i.e. the above interrupt number from three through ten). It can also specify a low level or the highest level interrupt priority to INT0 and INT1.

(12) Real-time service operation

The Real-Time Service (RTS) functions the 4-byte data-transfer between the Special Function Registers at acknowledging the interrupt request.

The RTS starts within 1 instruction cycle-time and completes within 5 instructions cycle-time after occurring the interrupt request.

(13) Sub-routine stack levels
- 128 levels (Max.) : stack area included in RAM area

(14) Multiplication and division
- 16 bits × 8-bit (7 instruction cycle times)
- 16 bits ÷ 8-bit (7 instruction cycle times)

(15) Three oscillation circuits
- On-chip RC oscillation circuit using for the system clock
- On-chip CR oscillation circuit using for the system clock
- On-chip crystal oscillation circuit using for the system clock and for time-base clock

  XT1 terminal can be used as $\overline{P74}$

(16) Standby function
- HALT mode function

  The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This operation mode can be released by the interrupt request signals or the initial system reset request signal.
- HOLD mode function

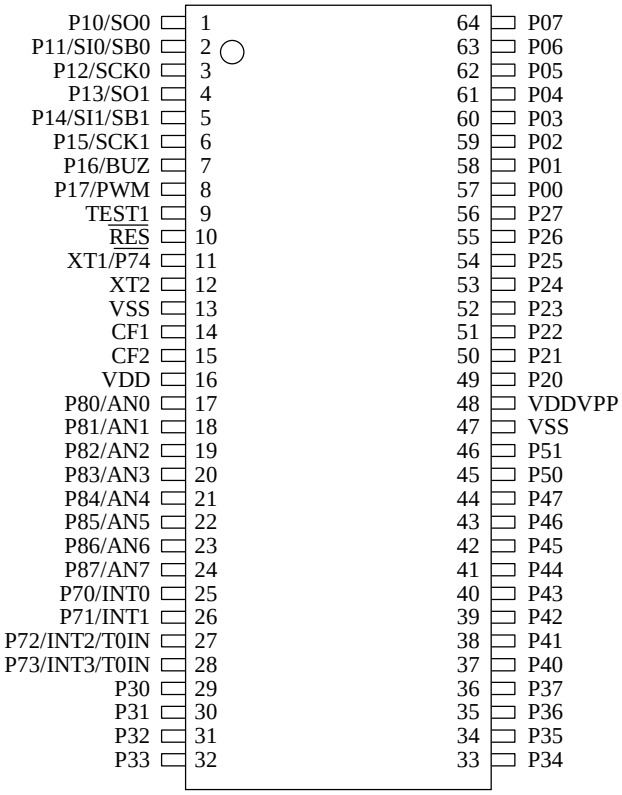
  The HOLD mode is used to freeze all the oscillations ;
  RC (internal), CF and Crystal oscillations. This mode can be released by the following operations.
  - Reset terminal ($\overline{RES}$) set to low level
  - P70/INT0, P71/INT1 terminals set to assigned level (programmable)
  - Input a Port 0 interrupt condition

(17) Factory shipment
- DIP64S, QFP64E delivery form

(18) Development support tools
- Evaluation (EVA) chip : LC866098
- EPROM version : LC86E5632
- One time version : LC86P5632
- Emulator : EVA86000 + ECB866600 (Evaluation chip board)
  + POD865000 (Pod for DIP64S)
  + POD865010 (Pod for QFP64E)

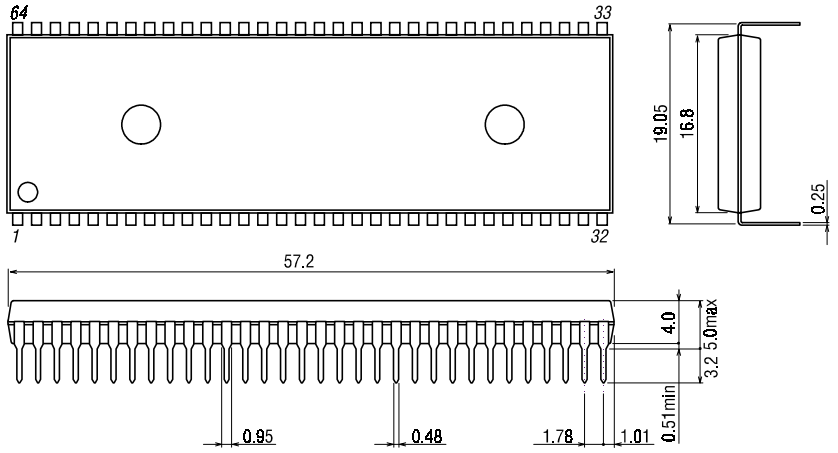
Pin Assignment

•DIP64S



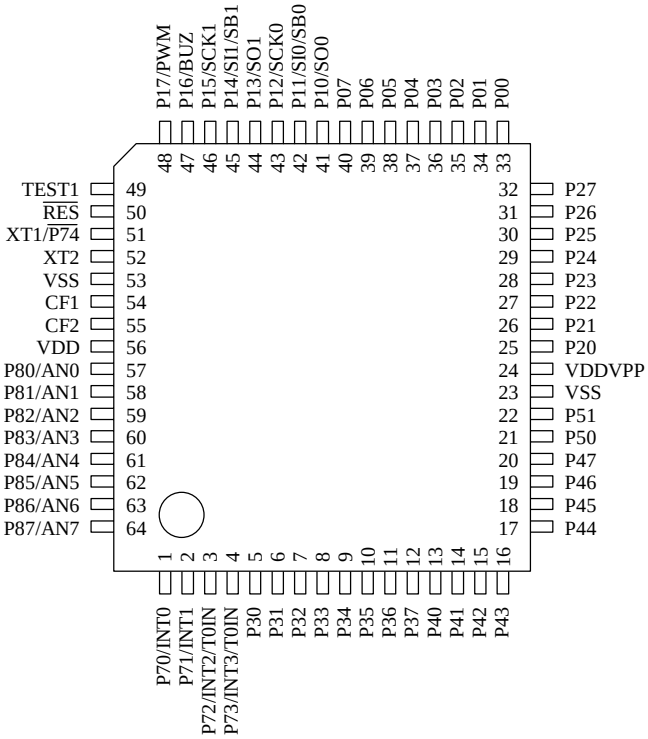
Package Dimension

(unit : mm)
3071



SANYO : DIP-64S(750mil)

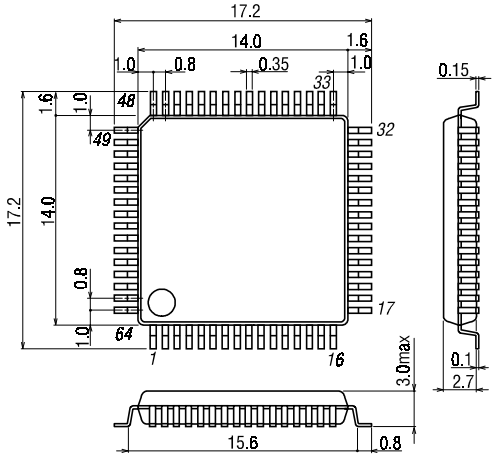
•QIP64E



Package Dimension

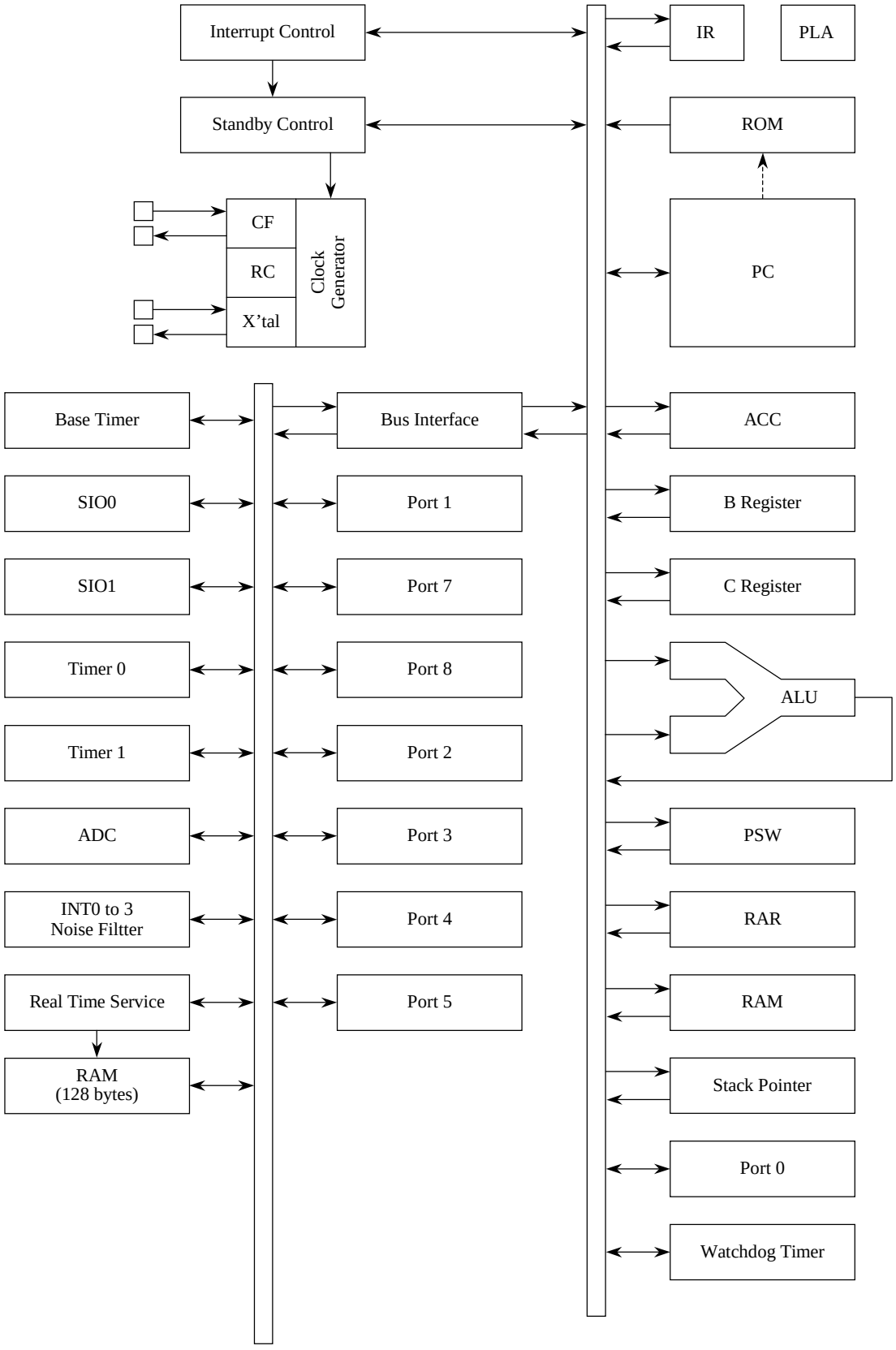
(unit : mm)

3159



SANYO : QIP-64E

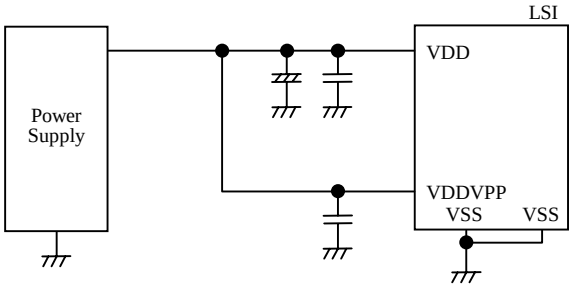
System Block Diagram



Pin Description

Pin name	I/O	Function description	Option
VSS	-	Power pin (–)	-
VDD	-	Power pin (+)	-
VDDVPP*	-	Power pin (+)	-
PORT0 P00 - P07	I/O	• 8-bit input/output port • Input for port 0 interrupt • Input/output in nibble units • Input for HOLD release	• Pull-up resistor : Provided/Not provided • Output form : CMOS/N-channel open drain
PORT1 P10 - P17	I/O	• 8-bit input/output port • Input/output can be specified in bit unit • Other pin functions P10 SIO0 data output P11 SIO0 data input/bus input/output P12 SIO0 clock input/output P13 SIO1 data output P14 SIO1 data input/bus input/output P15 SIO1 clock input/output P16 Buzzer output P17 Timer1 output (PWM output)	• Output form : CMOS/N-channel open drain
PORT2 P20 - P27	I/O	• 8-bit input/output port • Input/output in bit unit	• Output form : CMOS/N-channel open drain
PORT3 P30 - P37	I/O	• 8-bit input/output port • Input/output in bit unit • 15V withstand at N-channel open drain output	• Pull-up resistor : Provided/Not provided • Output form : CMOS/N-channel open drain
PORT4 P40 - P47	I/O	• 8-bit input/output port • Input/output in bit unit • 15V withstand at N-channel open drain output	• Pull-up resistor : Provided/Not provided • Output form : CMOS/N-channel open drain
PORT5 P50, P51	I/O	• 2-bit input/output port • Input/output in bit unit • 15V withstand at N-channel open drain output	• Pull-up resistor : Provided/Not provided • Output form : CMOS/N-channel open drain

* Connect like the following figure to reduce noise into a VDD terminal.
Short-circuit the VDD terminal to the VDDVPP terminal.
Short-circuit the VSS terminal to the VSS terminal.



<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>PORT7

P70

P71 - $\overline{P74}$</td><td>

I/O

I</td><td>• 5-bit input port
• Other pin functions
P70 : INT0 input/HOLD release/N-channel Tr. output for watchdog timer
P71 : INT1 input/HOLD release input
P72 : INT2 input/timer 0 event input
P73 : INT3 input with noise filter/timer 0 event input
$\overline{P74}$: Input pin XT1 for 32.768kHz crystal oscillation
• Interrupt received form, vector address
<table>
<tr><th></th><th>rising</th><th>falling</th><th>rising & falling</th><th>high level</th><th>low level</th><th>vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>• Pull-up resistor :
Provided/Not provided
(P70,71,72,73)
• $\overline{P74}$ does not have Pull-up resistor option</td></tr>
<tr><td>PORT8
P80 - P87</td><td>I</td><td>• 8-bit input port
• Pin description
AD input port (8 port pins)</td><td>-</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset pin</td><td>-</td></tr>
<tr><td>TEST1</td><td>O</td><td>• Test pin
Should be left unconnected
• Output fixed HIGH</td><td></td></tr>
<tr><td>XT1/ $\overline{P74}$</td><td>I</td><td>• Input pin for 32.768kHz crystal oscillation
In case of non use, connect to VDD
• Other function : Input port $\overline{P74}$</td><td>-</td></tr>
<tr><td>XT2</td><td>O</td><td>• Output pin for 32.768kHz crystal oscillation
• In case of non use, should be left unconnected</td><td>-</td></tr>
<tr><td>CF1</td><td>I</td><td>Input pin for ceramic resonator oscillation</td><td>-</td></tr>
<tr><td>CF2</td><td>O</td><td>Output pin for ceramic resonator oscillation</td><td>-</td></tr>
</table>

* All of port options can be specified in bit unit.

* A state of pins at reset

Pin name	Input/output mode	A state of pull-up resistor specified at pull-up option
Port 0 Ports 70,71,72,73	Input	Fixed pull-up resistor exist
Ports 1,2,3,4,5	Input	Programmable pull-up resistor OFF

1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Supply voltage		VDDMAX	VDD,VDDVPP	VDD=VDDVPP		-0.3		+7.0	V
Input voltage		VI(1)	•Ports 71,72,73, $\overline{74}$ •Port 8 • $\overline{RES}$			-0.3		VDD+0.3	
Input/output voltage		VIO(1)	•Ports 0,1,2 •Ports 3,4,5 at CMOS output option			-0.3		VDD+0.3	
		VIO(2)	Ports 3,4,5 at N-ch open drain output option			-0.3		15	
High level output current	Peak output current	IOPH(1)	Ports 0,1,2,3,4,5	•CMOS output •At each pin		-4			mA
	Total output current	ΣIOAH(1)	Ports 0,1	Total all pins		-20			
		ΣIOAH(2)	Ports 2,3,4,5	Total all pins		-20			
Low level output current	Peak output current	IOPL(1)	Ports 0,1,2,3,4,5	At each pin				20	
		IOPL(2)	Port 70	At each pin				15	
	Total output current	ΣIOAL(1)	Ports 0,1 Port 70	Total all pins				40	
		ΣIOAL(2)	Port 2	Total all pins				40	
		ΣIOAL(3)	Ports 3,4,5	Total all pins				80	
Maximum power dissipation		Pdmax(1)	DIP64S	Ta=-30 to +70°C				670	mW
		Pdmax(2)	QFP64E	Ta=-30 to +70°C				420	
Operating temperature range		Topr				-30		+70	°C
Storage temperature range		Tstg				-65		+150	

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Operating supply voltage range	VDD(1)	VDD	0.98μs ≤ tCYC ≤ 400μs		4.5		6.0	V
	VDD(2)		3.9μs ≤ tCYC ≤ 400μs		2.5		6.0	
Hold voltage	VHD	VDD	RAMs and the registers hold voltage at HOLD mode.		2.0		6.0	
Input high voltage	VIH(1)	Port 0 (Schmitt)	Output disable	2.5-6.0	0.4VDD +0.9		VDD	
	VIH(2)	•Ports 1,2 •Ports 72,73 (Schmitt)	Output disable	2.5-6.0	0.75VDD		VDD	
	VIH(3)	•Port 70 (Port input/interrupt) •Port 71 • $\overline{\text{RES}}$ (Schmitt)	Output N-channel Tr. OFF	2.5-6.0	0.75VDD		VDD	
	VIH(4)	Port 70 (Watchdog timer)	Output N-channel Tr. OFF	2.5-6.0	0.9VDD		VDD	
	VIH(5)	•Port $\overline{74}$ •Port 8	Output N-channel Tr. OFF	2.7-6.0	0.75VDD		VDD	
	VIH(6)	Ports 3,4,5 of CMOS output	Output disable	4.0-6.0	0.75VDD		VDD	
				2.5-4.0	0.8VDD		VDD	
	VIH(7)	Ports 3,4,5 of open drain output	Output disable	4.0-6.0	0.75VDD		13.5	
				2.5-4.0	0.8VDD		13.5	
Input low voltage	VIL(1)	Port 0 (Schmitt)	Output disable	2.5-6.0	VSS		0.2VDD	
	VIL(2)	•Ports 1,2,3,4,5 •Ports 72,73 (Schmitt)	Output disable	2.5-6.0	VSS		0.25VDD	
	VIL(3)	•Port 70 (Port input/interrupt) •Port 71 • $\overline{\text{RES}}$ (Schmitt)	N-channel Tr. OFF	2.5-6.0	VSS		0.25VDD	
	VIL(4)	Port 70 (Watchdog timer)	N-channel Tr. OFF	2.5-6.0	VSS		0.8VDD -1.0	
	VIL(5)	•Port $\overline{74}$ •Port 8	Output N-channel Tr. OFF	2.5-6.0	VSS		0.25VDD	
Operation cycle time	tCYC			4.5-6.0	0.98		400	μs
				2.5-6.0	3.9		400	

Continue.

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5-6.0		6		MHz
	FmCF(2)	CF1, CF2	•1.5MHz (ceramic resonator oscillation) •Refer to figure 1	2.5-6.0		1.5		
	FmRC		RC oscillation	2.5-6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	2.5-6.0		32.768		kHz
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5-6.0				ms
	tmsCF(2)	CF1, CF2	•1.5MHz (ceramic resonator oscillation) •Refer to figure 3	4.5-6.0				
				2.5-6.0				
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5-6.0				s
				2.5-6.0				

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Input high current	IIH(1)	Ports 3,4,5 of open drain output	•Output disable •VIN=13.5V (including the off-leak current of the output Tr.)	2.5-6.0			5	μA
	IIH(2)	•Port 0 without pull-up MOS Tr. •Ports 1,2,3,4,5	•Output disable •Pull-up MOS Tr. OFF. VIN=VDD (including the off-leak current of the output Tr.)	2.5-6.0			1	
	IIH(3)	•Ports 70,71,72,73 without pull-up MOS Tr. •Port 8	•VIN=VDD	2.5-6.0			1	
	IIH(4)	$\overline{RES}$	VIN=VDD	2.5-6.0			1	
Input low current	IIL(1)	•Ports 1,2,3,4,5 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. VIN=VSS (including the off-leak current of the output Tr.)	2.5-6.0	-1			
	IIL(2)	•Ports 70,71,72,73 without pull-up MOS Tr. •Port 8	•VIN=VSS	2.5-6.0	-1			
	IIL(3)	$\overline{RES}$	VIN=VSS	2.5-6.0	-1			
Output high voltage	VOH(1)	Ports 0,1,2,3,4,5 of CMOS output	IOH=-1.0mA	4.5-6.0	VDD-1			V
	VOH(2)		IOH=-0.1mA	2.5-6.0	VDD-0.5			
Output low voltage	VOL(1)	Ports 0,1,2,3,4,5	IOL=10mA	4.5-6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5-6.0			0.4	
	VOL(3)		•IOL=1.0mA •The current of any unmeasurement pin is not over 1 mA.	2.5-6.0			0.4	
	VOL(4)	Port 70	IOL=1mA	4.5-6.0			0.4	
	VOL(5)		IOL=0.5mA	2.5-6.0			0.4	
Pull-up MOS Tr. resistor	Rpu	•Ports 0,1,2,3,4,5 •Ports 70,71,72,73	VOH=0.9VDD	4.5-6.0	15	40	70	kΩ
				2.5-4.5	25	70	150	
Hysteresis voltage	VHIS	•Ports 0,1,2,3,4,5 •Ports 70,71,72,73 • $\overline{RES}$	Output disable	2.5-6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •Unmeasurement terminals for the input are set to VSS level. •Ta=25°C	2.5-6.0		10		pF

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5.	2.7-6.0	2			tCYC
		Low Level pulse width	tCKL(1)			2.7-6.0	1			
		High Level pulse width	tCKH(1)			2.7-6.0	1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	•Use pull-up resistor (1kΩ) when open drain output. •Refer to figure 5.	2.7-6.0	2			
		Low Level pulse width	tCKL(2)			2.7-6.0		1/2 tCKCY		
		High Level pulse width	tCKH(2)			2.7-6.0		1/2 tCKCY		
Serial input	Data set up time		tICK	•SI0,SI1 •SB0,SB1	•Data set-up to SCK0,1 •Data hold from SCK0,1 •Refer to figure 5.	4.5-6.0	0.1			μs
						2.7-6.0	0.4			
	Data hold time		tCKI			4.5-6.0	0.1			
						2.7-6.0	0.4			
Serial output	Output delay time (Serial clock is external clock)		tCKO(1)	•SO0,SO1 •SB0,SB1	•Use pull-up resistor (1kΩ) when open drain output. •Data hold from SCK0,1 •Refer to figure 5.	4.5-6.0			7/12 tCYC +0.2	
						2.7-6.0			7/12 tCYC +1	
	Output delay time (Serial clock is internal clock)		tCKO(2)			4.5-6.0			1/3 tCYC +0.2	
						2.7-6.0			1/3 tCYC +1	

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings				unit
				VDD[V]	min.	typ.	max.	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN •INT3	•Interrupt acceptable •Timer0-countable	2.7-6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is selected to 1/1.)	Interrupt acceptable	2.7-6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is selected to 1/16.)	Interrupt acceptable	2.7-6.0	32			
	tPIL(4)	$\overline{\text{RES}}$	Reset acceptable	4.5-6.0	200			μs

6. AD Converter Characteristics at Ta=-30°C to + 70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings				unit
				VDD[V]	min.	typ.	max.	
Resolution	N			4.5-6.0		8		bit
Absolute precision (Note 2)	ET			4.5-6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)	4.5-6.0	15.68 (tCYC= 0.98μs)		65.28 (tCYC= 4.08μs)	μs
			AD conversion time = 32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98μs)		130.56 (tCYC= 4.08μs)	
Analog input voltage range	VAIN	AN0 - AN7		4.5-6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5-6.0			1	μA
	IAINL		VAIN=VSS	4.5-6.0	-1			

(Note 2) Absolute precision excepts quantizing error (±1/2 LSB).

(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD	•FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops	4.5-6.0		10	20	mA
	IDDOP(2)		•FmCF=1.5MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops	4.5-6.0		3	7	
	IDDOP(3)			2.7-4.5		1.5	5	
	IDDOP(4)		•FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation	4.5-6.0		1.0	3.5	
	IDDOP(5)			2.7-4.5		0.6	3.0	
	IDDOP(6)		•FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops	4.5-6.0		50	150	μA
	IDDOP(7)			2.7-4.5		25	75	

Continue.

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Current dissipation in HALT mode (Note 4)	IDDHALT(1)	VDD	•HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops	4.5-6.0		5	10	mA
	IDDHALT(2)		•HALT mode •FmCF=1.5MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops	4.5-6.0		2.2	4.6	
	IDDHALT(3)			2.7-4.5		0.8	2.5	
	IDDHALT(4)		•HALT mode FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation	4.5-6.0		800	2000	μA
	IDDHALT(5)			2.7-4.5		400	1500	
	IDDHALT(6)		•HALT mode FmCF=0Hz (when oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops	4.5-6.0		35	140	
	IDDHALT(7)			2.7-4.5		11	56	
Current dissipation in HOLD mode (Note 4)	IDDHOLD(1)	VDD	HOLD mode	4.5-6.0		0.05	30	
	IDDHOLD(2)			2.7-4.5		0.02	20	

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation recommended constant (main clock)

Oscillation type	Maker	Oscillator	C1	C2	Rf	Rd
12MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33pF	33pF	OPEN	560Ω
		CSA12.0MTZ	39pF	30pF	OPEN	0Ω
		CST12.0MTW	on chip		OPEN	560Ω
3MHz ceramic resonator oscillation	Murata	CSA3.00MG040	100pF	100pF	OPEN	1.5Ω
		CST3.00MGW040	on chip		OPEN	1.5Ω

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation recommended constant (sub clock)

Oscillation type	Maker	Oscillator	C3	C4
32.768kHz crystal oscillation	Kyocera	KF-38G-13P0200	18pF	18pF
	Seiko Epson	MC-306,C-002RX,32.768kHz	4pF	4pF

* Both C3 and C4 must use J rank (±5%) and CH characteristics.
(It is about the application which is not in need of high precision. Use K rank (±10%) and SL characteristics.)

(Notes) •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.

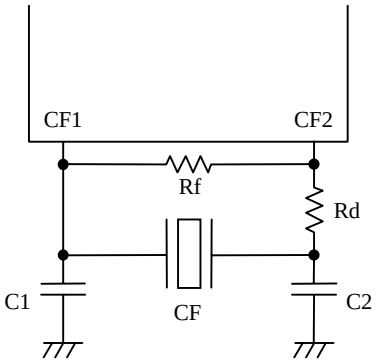


Figure 1 Main-clock circuit
Ceramic oscillation circuit

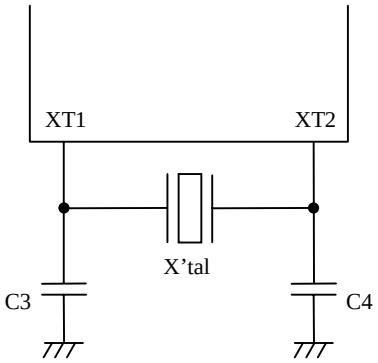


Figure 2 Sub-clock circuit
Crystal oscillation

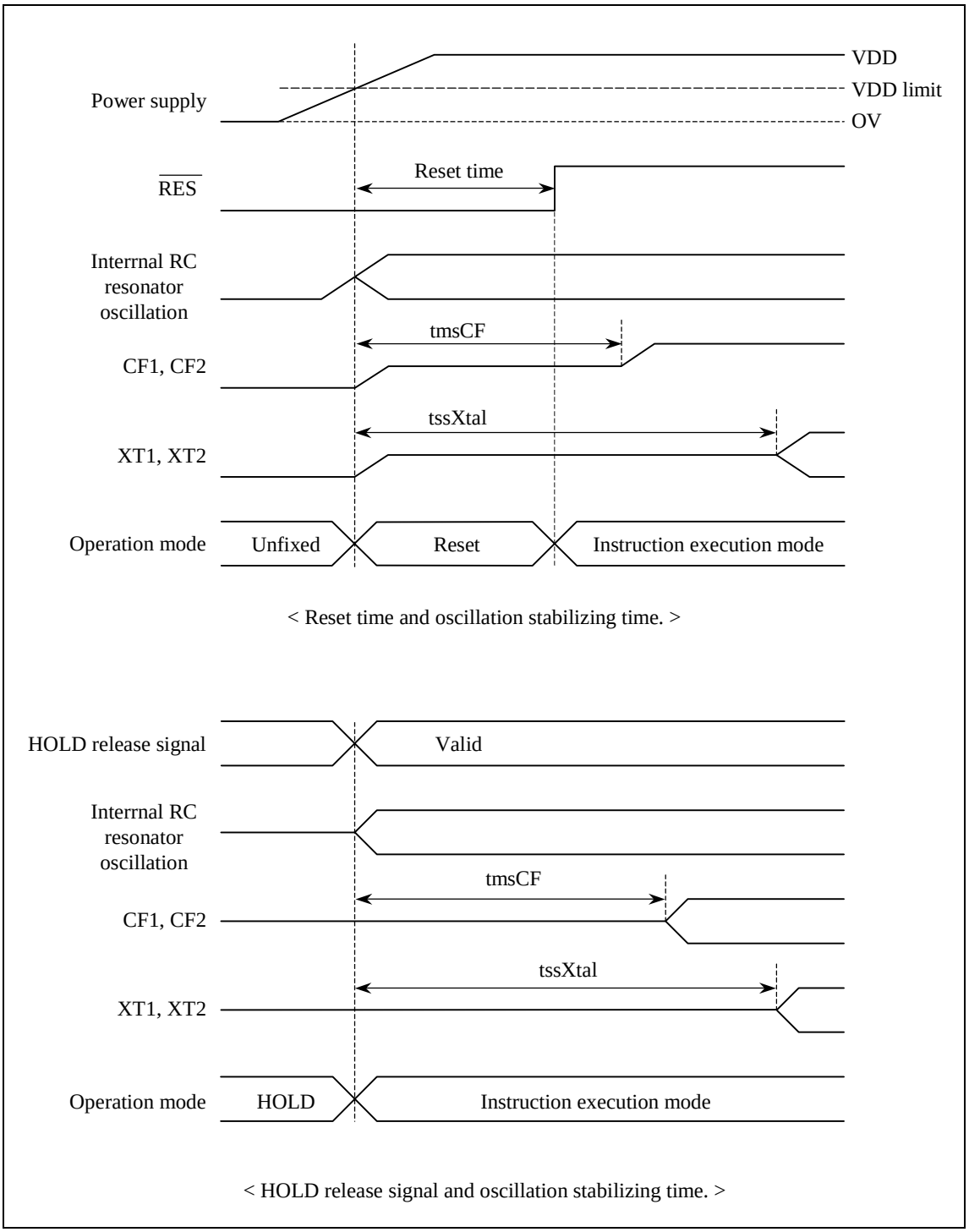
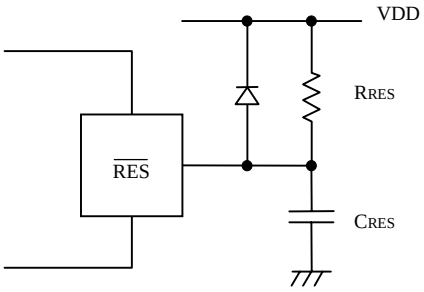


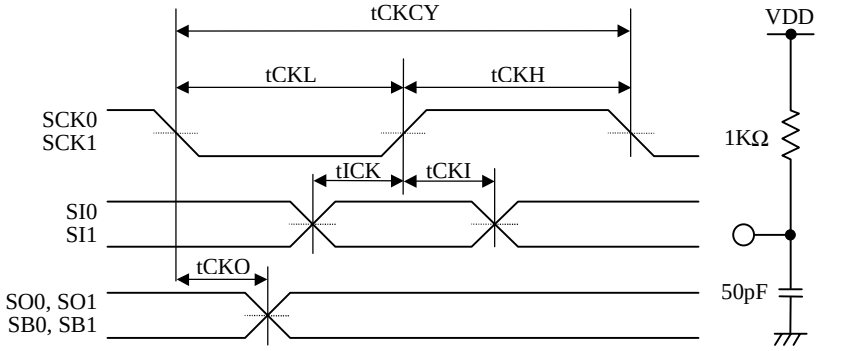
Figure 3 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

<AC timing point>



<Timing> <Test load>

Figure 5 Serial input / output test condition

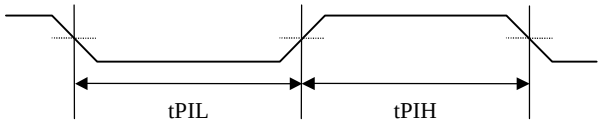


Figure 6 Pulse input timing condition

memo: