CDP68HC68A2

July 1998

CMOS Serial 10-Bit A/D Converter

Features

- **10-Bit Resolution**
- **8-Bit Mode for Single Data Byte Transfers**
- **SPI (Serial Peripheral Interface) Compatible**
- **Operates Ratiometrically Referencing V_{DD} or an External Source**
- **14µs 10-Bit Conversion Time**
- **8 Multiplexed Analog Input Channels**
- **Independent Channel Select**
- **Three Modes of Operation**
- **On Chip Oscillator**
- **Low Power CMOS Circuitry**
- **Intrinsic Sample and Hold**
- **16 Lead Dual-In-Line Plastic Package**
- **20 Lead Dual-In-Line Small Outline Plastic Package**
- **Evaluation Board available - CDP68HC05C16BEVAL**

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CDP68HC68A2E	-40 to 85	16 Ld PDIP	E16.3
CDP68HC68A2M	-40 to 85	20 Ld SOIC	M20.3

Description

The CDP68HC68A2 is a CMOS 8-bit or 10-bit successive approximation analog to digital converter (A/D) with a standard Serial Peripheral Interface (SPI) bus and eight multiplexed analog inputs. Voltage referencing is user selectable to be relative to either V_{DD} or analog channel 0 (AI0). The analog inputs can range between V_{SS} and V_{DD}.

The CDP68HC68A2 employs a switched capacitor, successive approximation A/D conversion technique which provides an inherent sample-and-hold function. An onchip Schmitt oscillator provides the internal timing for the A/D converter. The Schmitt input can be externally clocked or connected to a single, external capacitor to form an RC oscillator with a period of approximately 10-30ns per picofarad.

Conversion times are proportional to the oscillator period. At the maximum specified frequency of 1MHz, 10-bit conversions take 14µs per channel. At the same frequency, 8-bit conversions consume 12µs per channel.

The versatile modes of the CDP68HC68A2 allow any combination of the eight input channels to be enabled and any one of the selected channels to be specified as the “starting” channel. Conversions proceed sequentially beginning with the starting channel. Nonselected channels are skipped. Modes can be selected to: sequence from channel to channel on command; sequence through channels automatically, converting each channel one time; or sequence repeatedly through all channels.

The results of 10-bit conversions are stored in 8-bit register pairs (one pair per channel). The two most significant bits are stored in the first register of each pair and the eight least significant bits are stored in the second register of the pair. To allow faster access, in the 8-bit mode, the results of conversions are stored in a single register per channel.

A read-only STATUS register facilitates monitoring the status of conversions. The STATUS register can simply be polled or the $\overline{INT}$ pin can be enabled for interrupt driven communications.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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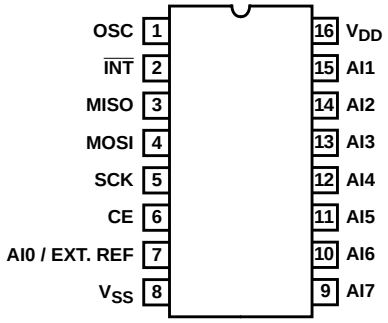
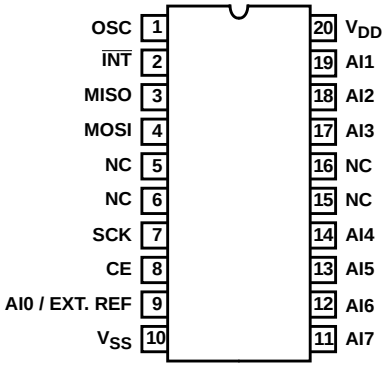
File Number **1963.3**

Pinouts

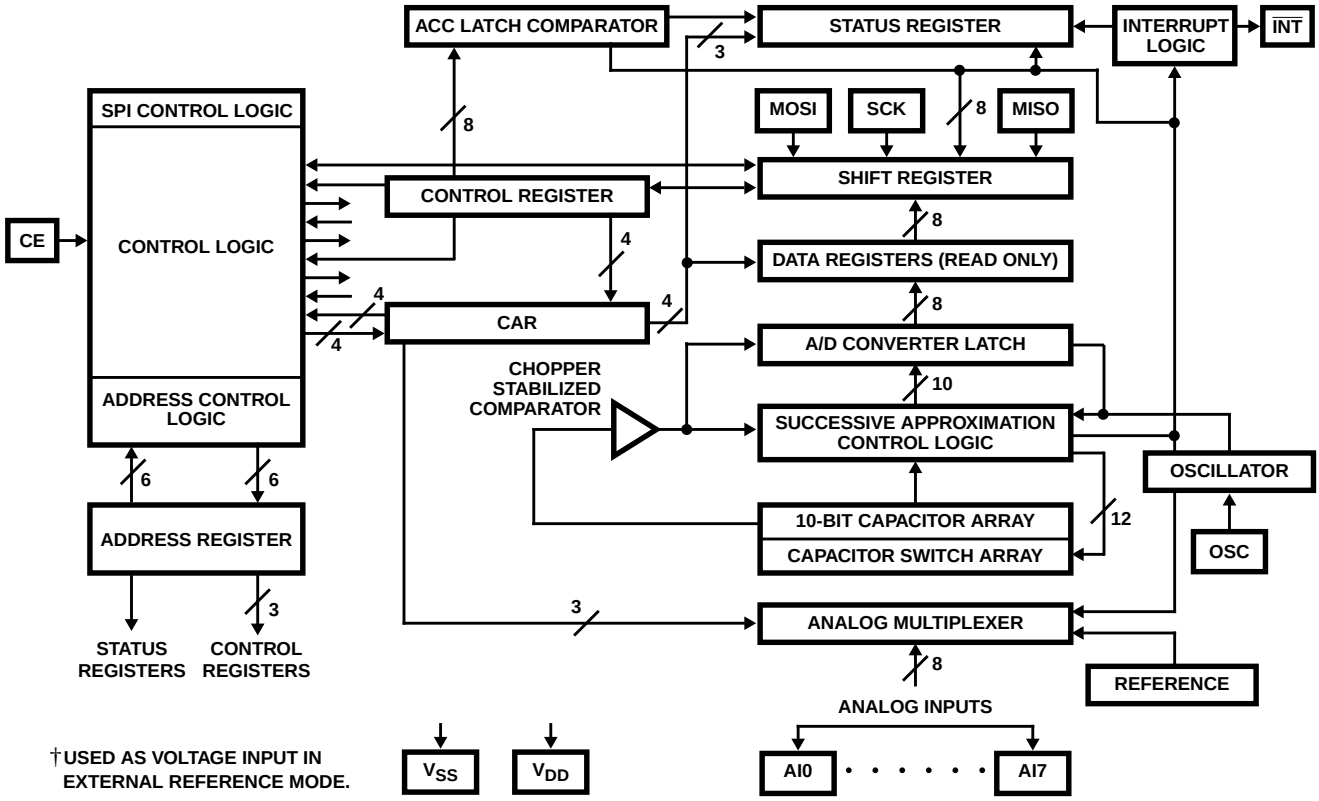
CDP68HC58A2E
(PDIP)
TOP VIEW



CDP68HC68A2M
(SOIC)
TOP VIEW



Block Diagram



Absolute Maximum Ratings

DC Supply Voltage Range, (V_{DD}) . . . . . -0.5V to +7V
(Voltage Referenced to V_{SS} Terminal)
Input Voltage Range, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. . . . . ±10mA

Operating Conditions (Note 1)

Temperature Ambient, T_A . . . . . -40°C to 85°C
DC Voltage Range . . . . . 3V Min, 6V Max

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
PDIP Package 90
SOIC Package 104
Maximum Power Dissipation Per Package (P_D)
T_A = -40°C to 60°C (Package Type E) 500mW
T_A = 60°C to 85°C (Package Type E)
Derate Linearly at . . . . . 12mW/°C to 200mW
T_A = -40°C to 70°C (Package Type M) (Note 3) 400mW
T_A = -70°C to 85°C (Package Type M) (Note 3)
Derate Linearly at . . . . . 6.0mW/°C to 310mW
Device Dissipation Per Output Transistor 40mW
T_A = Full Package Temperate Range (All Package Types)
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range (T_{STG}) . . . . . -65°C to 150°C
Maximum Lead Temperature (During Soldering) . . . . . 265°C
At Distance 1/16 ±1/32 In. (1.59 ± 0.79mm)
From Case for 10s Max (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the ranges specified.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. Printed circuit board mount: 58mm x 57mm minimum area x 1.6mm thick G10 epoxy glass, or equivalent.

Electrical Specification T_A = 25°C, V_{DD} = 5V, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Differential Linearity Error	10-Bit Mode	-	±1.25	±2	LSB
Integral Linear Error	10-Bit Mode	-	±1.25	±2	LSB
Offset Error	10-Bit Mode	-1	3	4	LSB
Gain Error	10-Bit Mode	-1	1	2	LSB
ANALOG INPUTS: AI0 THRU AI7					
Input Resistance	In Series with Sample Caps	-	85	-	Ω
Sample Capacitance	During Sample State	-	400	-	pF
Input Capacitance	During Hold State	-	20	-	pF
Input Current	At V_{IN} = V_{REF} + During Sample During Hold or Standby State	-	+30	-	µA
		-	-	±1	µA
Input + Full Scale Range	From Input RC Time Constant VR = 1	V_{SS}	-	V_{DD} +0.3	V
Input Bandwidth (3dB)		-	4.68	-	MHz
Input Voltage Range: AI0		3.0	-	V_{DD}	V
DIGITAL INPUTS: MOSI, SCK, CE, T_A = -40°C to 85°C					
High Input Voltage V_{IH}	V_{DD} = 3 to 6V	70	-	-	% of V_{DD}
Low Input Voltage V_{IL}	V_{DD} = 3 to 6V	-	-	30	% of V_{DD}
Input Leakage		-	-	±1	µA
Input Capacitance	T_A = 25°C	-	-	10	pF

Electrical Specification $T_A = 25^oC$, $V_{DD} = 5V$, Unless Otherwise Specified. **(Continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS: MISO, INT, $T_A = -40^oC$ to 85^oC						
High Level Output	V_{OH}, MISO	I_{SOURCE} 6mA	4.25	-	-	V
Low Level Output	V_{OL}, MISO, INT	I_{SINK} = 6mA	-	-	0.4	V
Three-State Output Leakage	I_{OUT}, MISO, INT		-	-	±10	µA
TIMING PARAMETERS $T_A = -40^oC$ to 85^oC						
Oscillator Frequency	f_{SAMPLE}	10-Bit Mode	-	-	-1	MHz
Conversion Time (Including Sample Time)		10-Bit Mode	14 Oscillator Cycles			
		8-Bit Mode	12 Oscillator Cycles			
Sample Time (Pre-Encode)		8 Time Constants (8τ) Required	First 1.5 Oscillator ≥ 8τ			
Serial Clock (SCK) Frequency			-	-	1.5	MHz
SCK Pulse Width	T_P	Either SCK_A or SCK_B	150	-	-	ns
MOSI Setup Time	T_{DSU}	Prior to Leading Edge of T_P	60	-	-	ns
MOSI Hold Time	T_{DH}	After Leading Edge of T_P	60	-	-	ns
MISO Rise and Fall Time		200pF Load	-	-	100	ns
MISO Propagation Delay	T_{DOD}	From Trailing SCK Edge	-	-	100	ns
I_{DD}		V_{DD} = 5V, Continuous Operation	-	1.4	2	mA
I_{DD}		V_{DD} = 3V, Continuous Operation	-	0.7	1.2	mA

Through this specification the CDP68HC68A2 is referred to simply as the A2.

Functional Pin Description

OSC - Oscillator (Input/Output)

This pin is user programmable. In the “external” mode, the clock input for the successive approximation logic is applied to OSC from an external clock source. The input is a Schmitt trigger input which provides excellent noise immunity. In the “internal” mode, a capacitor is connected between this pin and a power supply to form a “one pin oscillator”. The frequency of the oscillator is inversely dependent on the capacitor value. Differences in period, from one device to another, should be anticipated. Systems utilizing the internal oscillator must be tolerant of uncertainties in conversion times or provide trimming capability on the OSC capacitor. See Table 2 for typical frequencies versus capacitance.

$\overline{\text{INT}}$ - Interrupt (Open Drain Output)

$\overline{\text{INT}}$ is used to signal the completion of an A/D conversion. This output is generally connected, in parallel with a pullup resistor, to the interrupt input of the controlling microprocessor. The open drain feature allows wire-NOR’ing with other interrupt inputs. The inactive state of $\overline{\text{INT}}$ is high impedance. When active, $\overline{\text{INT}}$ is driven to a low level output voltage. The state of $\overline{\text{INT}}$ is controlled and monitored by bits in the Mode Select and Status Registers.

MISO - Master-In-Slave-Out (Output)

Serial data is shifted out on this pin. Data is provided most significant bit first.

MOSI - Master-Out-Slave-In (Input)

Serial data is shifted in on this pin. Data must be supplied most significant bit first. This is a CMOS input and must be held high or low at all times to minimize device current.

SCK - Serial Clock (Input)

Serial data is shifted out on MISO, synchronously, with each leading edge of SCK. Input data from the MOSI pin is latched, synchronously, with each trailing edge of SCK.

CE - Chip Enable (Input)

An active HIGH device enable. CE is used to synchronize communications on the SPI lines (MOSI, MISO, and SCK). When CE is held in a low state, the SPI logic is placed in a reset mode with MISO held in a high impedance state. Following a transition from low to high on CE, the CDP68HC68A2 interprets the first byte transferred on the SPI lines as an address. If CE is maintained high, subsequent transfers are interpreted as data reads or writes.

AIO/$\overline{\text{EXT}}$ REF - Analog Input 0/External Reference (Input)

This input is one of eight analog input channels. Its function is selectable through the Mode Select Register (MSR). If VR is set high in the MSR, AI0/$\overline{\text{EXT}}$ REF provides an external voltage reference against which all other inputs are measured. AI0/$\overline{\text{EXT}}$ REF must fall within the V_{SS} and V_{DD} supply rails. If VR is set low in the MSR, V_{DD} is used as the reference voltage and AI0/$\overline{\text{EXT}}$ REF is treated as any other analog input (see AI1-AI7).

AI1-AI7 - Analog Inputs 1-7 (Inputs)

Together with AI0/$\overline{\text{EXT}}$ REF, these pins provide the eight analog inputs (channels) which are multiplexed within the CDP68HC68A2 to a single, high-speed, successive approximation, A/D converter. AI1-AI7 must fall within the V_{SS} and V_{DD} supply rails.

V_{SS} - Negative Power Supply

This pin provides the negative analog reference and the negative power supply for the CDP68HC68A2.

V_{DD} - Positive Power Supply

This pin provides the positive power supply and, depending on the value of the VR bit in the MSR, the positive analog reference for the CDP68HC68A2.

Overview

From the programmer’s perspective, the A2 is comprised of three control registers (Mode Select Register - MSR, Channel Select Register - CSR, and Starting Address Register - SAR), a status register (SR), an array of eight pairs of Data Registers, and one non-addressable, internal register (Channel Address Register). See Figure 1.

The A2 contains a high speed, 10-bit, successive approximation, analog to digital converter (A/D). The input to the A/D can be any one of the A2’s eight analog inputs (AI0 through AI7). The contents of the CAR determine which analog input is connected to the A/D. The result of each analog to digital conversion is written to the Data Register array. The Data Register array is also addressed by the contents of the CAR, providing a one to one correspondence between each analog input and each Data Register pair.

The contents of the CAR are also used during Data Register reads to address the Data Register array. The CAR is automatically jammed with the correct address when an Address/Control Byte is sent to the A2. A second means, to initialize the CAR, is by writing to the SAR.

Normal procedure for programming the A2 is to first select the desired hardware mode by writing to the MSR. The “active” analog channels are then specified by writing to the CSR (channels not selected in the CSR are skipped during conversions and burst mode reads). Finally, a write to the SAR initializes the CAR (designating the first channel to convert) and initiates the A/D conversions.

Polling of the SR or hardware interrupts can be used to determine the completion of conversions.

The converted data is read from the data registers. In eight bit mode, a single register is read for each channel of interest. In ten bit mode, two registers are read per channel.

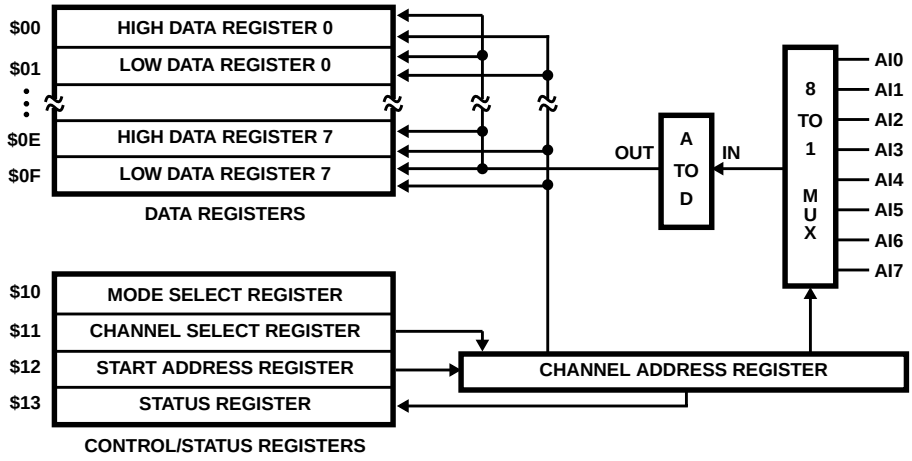


FIGURE 1. A PROGRAMMER'S MODEL OF THE CDP68HC68A2

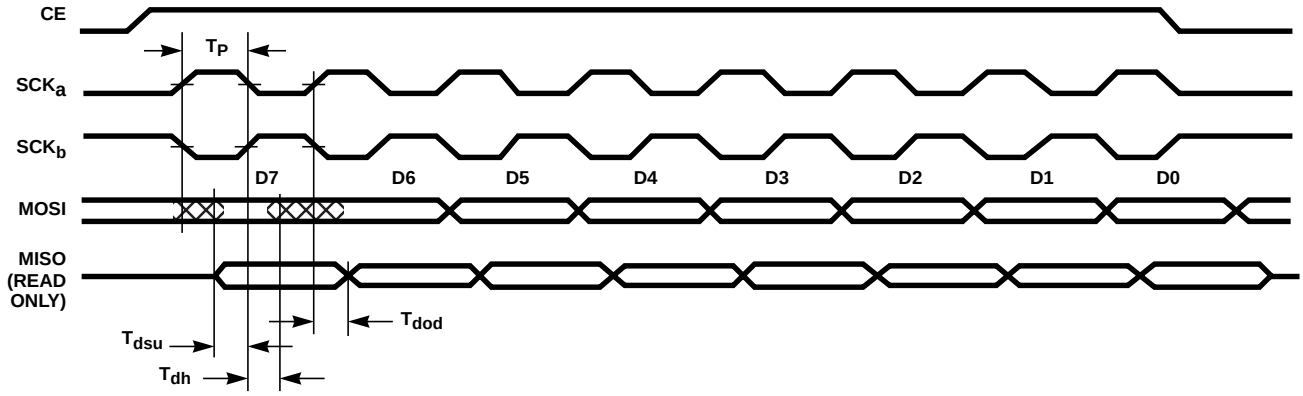


FIGURE 2. TIMING DIAGRAM FOR SERIAL PERIPHERAL INTERFACE

Serial Communications

Hardware Interface

All communications between the A2 and the controlling processor are carried out over the Serial Peripheral Interface (SPI) bus lines (MOSI, MISO, SCK, and CE). The SPI bus is directly compatible with the SPI facilities of Intersil' CDP68HC05 microcontrollers. Data is transmitted over the MISO and MOSI lines synchronous with SCK. Transfers are done most significant bit first.

The A2 acts as a "slave" device. The controlling "master" signals the A2 that a SPI transfer is to take place by raising CE and clocking SCK. A single shift register is used for transferring data in and out of the A2. Whenever CE and SCK are activated, data is shifted from the master to the A2 over the Master-Out-Slave-In (MOSI) line and, simultaneously, during read operations, data is shifted to the master from the A2 over the Master-In-Slave-Out (MISO) line. Note that SCK must be provided by the master for both reads and writes.

To accommodate various hardware systems, the A2 can shift data on either the rising or falling edge of SCK. The "active" edge is automatically determined by the A2. At the moment that CE is first brought to a high level, the state of SCK is latched. This latched state determines the interpretation of SCK. If SCK is low when CE is activated, data is shifted out on MISO on each rising edge of SCK and data is latched from MOSI on each falling edge of SCK (see SCK_a in Figure 2). If SCK is high when CE is activated, data is shifted out on MISO on each falling edge of SCK and data is latched from MOSI on each rising edge of SCK (see SCK_b in Figure 2).

Hardware Interfacing to CDP68HC05 Controllers

When interfacing the A2 to CDP68HC05 controllers, set CPHA = 1 and CPOL = (0 or 1) in the SPI control register. Note that SCK pulses are generated only when data is written to the SPI Data Register in a CDP68HC05. Reading data from or writing data to the A2 requires writing data to the SPI Data Register. The data will be ignored by the A2 for read operations. The read data is available to the CDP68HC05 in the SPI Data Register when SPIF is true in the SPI Status Register.

Hardware Interfacing to Non-CDP68HC05 Controllers

Most popular microcontrollers have a synchronous communications facility which can be adapted to work with the A2. Those that don't can be easily interfaced using port lines to synthesize a SPI bus.

Software Interface

Reading and writing to the A2 can be performed in either single byte or multiple byte (burst) modes. Both modes begin the same way: a positive transition is applied to CE (if CE is high, it must first be brought low, then returned high); an address/control byte is transferred (requires 8 clocks on SCK and 8 bits of data on MOSI); and the first byte of data is transferred (requires 8 clocks of SCK). In the case of single byte mode, the transfer is complete. For multiple byte transfers, each series of 8 pulses on SCK produces another 8-bit transfer (see Figure 3).

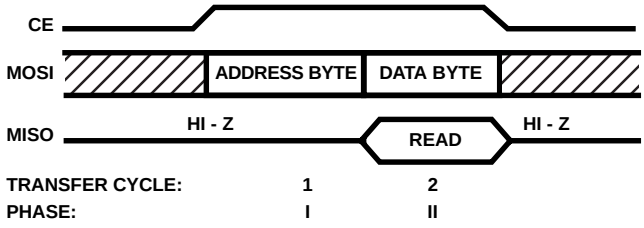


FIGURE 3A. SINGLE BYTE TRANSFER (REQUIRES 2 SPI TRANSFERS)

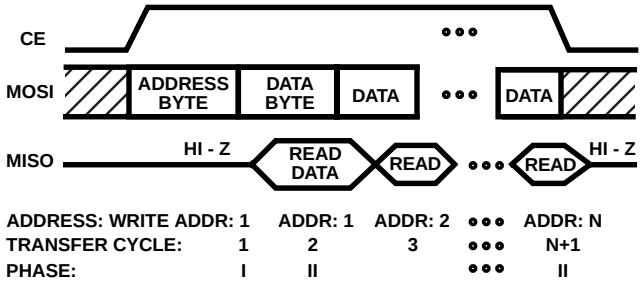


FIGURE 3B. MULTIPLE (N) BYTE TRANSFER (EFFICIENT DEVICE COMMUNICATION REQUIRING N+1 SPI TRANSFERS)

The format of the address/control byte is shown in Figure 4. The most significant bit is the $\overline{R}$/W bit. When $\overline{R}$/W is 0, read operations are to be performed. If $\overline{R}$/W is 1, write operations are to be performed. A0 through A4 specify the register to access. Data registers are mapped to address $00 through $0F. The Control and Status Registers are at locations $10 through $13 (See Figure 1).

When transferring multiple bytes of data, the type of transfer - read or write - is fixed by bit seven of the initial address/control byte. After the initial data transfer, the address will automatically be adjusted for each subsequent transfer.

When reading Data Registers in the 8-bit mode, each read will advance the address by two, to the next (as specified in the CSR) active channel's Low Data Register. In the 10-bit mode, following a read of a High Data Register, the address is advanced to the Low Data Register of the same channel. Reading the Low Data Register then increments the read address to the next (as specified in the CSR) active channel's High Data Register. Following a read of the last (closest to 7) active channel's Data Register(s), the address recycles to the first (closest to 0) active channel's Data Register(s).

When reading or writing control registers, the address will increment to the next register after each transfer. Once address $13 has been reached no more increments are performed. This facilitates polling of the Status Register (SR) which is located at address $13. If the A2 remains selected following a read of SR, each successive 8 bit transfer will read the SR again without; the need for an address /control byte.

Programming the CDP68HC68A2 Registers

Initializing the A2

The A2 is equipped with a power on reset circuit which clears the MSR to all 0's. This ensures that $\overline{INT}$ is in a high impedance state and conversions are inhibited. The contents of all other registers are unknown until explicitly initialized. No other provisions are made for resetting the A2.

Systems which can be reset after power up must reset the A2 by explicitly writing 0's to the MSR. Designs which utilize the $\overline{INT}$ line must be certain that the MSR is cleared, or the A2 is initialized to a known state, before enabling interrupts.

NOTE: It is good practice to include code which initializes the A2, to a known state, at the earliest practical point. In systems which utilize $\overline{INT}$, if a system reset occurs after power-up, A2 initialization code must be executed before processor interrupts are enabled.

Address/Control Byte

The Address/Control Byte is a dual purpose word which performs register addressing and read/write control. The Address/Control Byte is the first byte transferred to the A2 following activation of CE. If CE is active, it must first be brought low, then reactivated prior to transferring an Address/Control Byte.

$\overline{R}$/W	-	-	A4	A3	A2	A1	A0
7	6	5	4	3	2	1	0

FIGURE 4. ADDRESS/CONTROL BYTE

The most significant bit (MSB) of the Address/Control byte is $\overline{R}$/W. This bit is used to control the flow of data during the subsequent SPI data transfers. If $\overline{R}$/W is a 0, reads take place. If $\overline{R}$/W is a 1, writes take place. During read transfers, data is shifted out on MISO. During writes, data is shifted in on MOSI and MISO is held in a high impedance state.

The least significant five bits (A0 through A4) provide the read address. Bits 5 and 6 are not required and can be sent as either 0 or 1 (0's are assembled throughout this specification). When addressing Data Registers in 8-bit mode, A0 is internally forced to a 1. Attempting to read a High Data Register in 8-bit mode will result in a read of the Low Data Register of the next active channel).

NOTE: CAUTION! When addressing Data Registers, the user must ensure that the contents of the CAR match the address portion of the Address/Control Byte. Failure to do so may result in corrupted data. This condition is generally met in Modes 1 and 2. When running in Mode 3 special care must be taken to meet this requirement. See further explanation under SAR, SR, Modes, and Applications Information.

Mode Select Register (MSR)

Address/Control: (R/W)0010000 - $10

Read/Write: Yes

7	6	5	4	3	2	1	0	
0	0	$\overline{EXT}$	VR	M8	IE	M1	M0	$10

The read/write register is used to select the various modes of operation of the A2. Bits 6 and 7 are “don’t cares” and can be set as either 1 or 0. The functions of bits 0 through 5 are as follows:

B5, $\overline{EXT}$ The External Oscillator bit ($\overline{EXT}$) is used to select between an external or an internal (single pin oscillator) clock source at pin 1 (OSC) of the A2. If $\overline{EXT}$ is low, an external clock is selected and the OSC pin functions as an input. If $\overline{EXT}$ is high, an internal clock is selected and the OSC pin functions as a one pin oscillator. See Table 2 for typical frequencies of the internal oscillator.

B4, VR The Voltage Reference (VR) bit is used to select the source of the voltage reference. When VR is 0, V_{DD} is used as the full scale reference for the A/D converter. When VR is 1, the voltage at AI0 serves as the full scale reference for the A/D converter. When VR = 1, the digital reading of any active channel which exceeds the AI0 reference voltage will be “clipped” to the full scale value of $3FF ($FF for 8-bit mode).

B3, M8 The Eight Bit Mode (M8) bit selects either 10-bit or 8-bit as the mode of operation. A low (0) in this bit enables the 10-bit mode, while a high (1) enables the 8-bit mode.

B2, IE The Interrupt Enable (IE) bit is used to enable the $\overline{INT}$ output function on pin 2. A low (0) disables the interrupt function and maintains $\overline{INT}$ in a high impedance state. A high enables the interrupt function, allowing $\overline{INT}$ to be driven low at the appropriate times in Modes 1 and 2.

B1, M1 Mode Select, bit 1. This bit is used along with M0 to select the conversion mode, shown in Table 1, of the A/D converter.

B0, M0 Mode Select, bit 0. This bit is used along with M1 to select the conversion mode, shown in Table 1, of the A/D converter.

TABLE 1. CONVERSION MODES

M1	M2	MODE	DESCRIPTION
0	0	0	Idle
0	1	1	Single Conversion
1	0	2	Single Scan
1	1	3	Continuous Scan

Channel Address Register (CAR)

Address/Control: Not Addressable

The CAR contains the address of the next channel to convert during Modes 1, 2, and 3. During multiple byte reads of the Data Registers, the CAR contains the address of the channel to read and is advanced, to the next higher active channel, following each read. When advancing, the CAR skips any channel not selected in the CSR. After incrementing to the highest active channel, the CAR will return to the lowest active channel.

The CAR is not directly accessible. It can be jammed via a write to the SAR or by transmitting an Address/Control Byte which addresses any Data Register. Note: addressing a Data Register to set the CAR is valid only under certain circumstances - see the following boxed caution. When jamming the CAR via the SAR, the specified channel does not need to be selected in the CSR. The CAR’s contents are read as part of the SR. See the descriptions of the SAR and the SR for details.

NOTE: CAUTION! When addressing Data Registers, the user must ensure that the contents of the CAR match the address portion of the Address/Control Byte. Failure to do so may result in corrupted data. This condition is generally met in Modes 1 and 2. When running in Mode 3 special care must be taken to meet this requirement. See further explanation under SAR, SR, Modes, and Applications Information.

Channel Select Register (CSR)

Address/Control: (R/W)0010001 - $11

Read/Write: Yes

7	6	5	4	3	2	1	0	
C7	C6	C5	C4	C3	C2	C1	C0	$11

This read/write register is used to designate the active analog input channels. Channels which are not active will be skipped during conversions and multiple byte reads, unless specifically selected by writing to the SAR. Setting a bit high in CSR selects the associated channel, while setting a bit low deselects the channel. Each Cn bit in the CSR corresponds to an AIn pin on the A2 device. Example: setting C7 = C4 = 1 and setting all other bits to 0 will select AI7 and AI4 as inputs to the A/D multiplexer.

Starting Address Register (SAR)

Address/Control: (R/W)0010010 - $12

Read/Write: Yes

7	6	5	4	3	2	1	0	
ENC	0	0	SAE	CA2	CA1	CA0	$\overline{H}$/L	$12

This register is used to enable conversions in all modes and to set the address of the current channel in the CAR. Prior to, or simultaneously with, enabling conversions, the CAR must be set to a known state via the SAR. Once set, the contents of the CAR determine the first channel to be converted when conversions are enabled - hence the name “Starting Address Register”. The CAR may be jammed with

the number of a channel which is not selected in the CSR. After the specified channel is converted, subsequent conversions proceed in ascending order, skipping channels not selected in the CSR. Therefore, jamming the CAR with a non-selected channel number will cause a conversion to be performed on that channel once and only once.

After stopping a Mode 2 or 3 conversion (by setting ENC low), the CAR must be jammed to match the channel address prior to initiating Data Register reads. If an Address/Control Byte is sent to begin reads from a Data Register other than the one currently addressed by the CAR, the contents of the Data Register may be corrupted. If the CAR contents are known, single or multiple byte reads can be properly made, by sending a matching Address/Control Byte.

Bits 5 and 6 in the SAR are “don’t cares” and can be set to either 0’s or 1’s. The functions of the remaining bits are as follows:

B7, ENC — The Enable Conversions (ENC) bit is used to synchronously switch on and off the successive approximation A/D converter. When this bit is set high, the appropriate conversion operation (as defined in the MSR) is initiated. Setting the ENC bit low stops the conversion operation. If a channel is being converted when ENC is cleared, the conversion of that channel will complete and further conversions will be inhibited.

B4, SAE — Starting Address Enable (SAE). If the SAR is written to, with the SAE bit high, the CAR is jammed with the value defined by CA2, CA1, and CA0. If SAE is low, the CA2, CA1, and CA0 bits are ignored.

B3, CA2 — Channel Address, bit 2. When writing to the SAR with SAE high, CA2, CA1, and CA0 form a 3-bit channel address which is used to set the CAR and select the first channel to be converted or read. Reading the SAR returns the previously written values for these three bits. To determine the contents of the CAR a read of the Status Register (SR) must be performed.

B2, CA1 — Channel Address, bit 1. See discussion under CA2.

B1, CA0 — Channel Address, bit 0. See discussion under CA2.

B0, $\overline{H}$/L — $\overline{High}$/Low. For most applications, the SAR should be written with $\overline{H}$/L as a 0. In combination with CA2, CA21, and CA0, this bit is used to select a specific High or Low Data Register. $\overline{H}$/L only has significance in 10-bit mode. The 10-bit read sequence is High Data Register followed by Low Data Register for each channel read. When jamming the CAR prior to reads, $\overline{H}$/L should be set low, unless the user specifically wants to skip the first High Data Register. When read, this bit, indicates whether the next Data Register read will access the High or Low Data Register. In 8-bit mode, $\overline{H}$/L is ignored by the A2.

Status Register (SR)

Address/Control: 00010011 - $13

Read/Write: Read Only

7	6	5	4	3	2	1	0	
INT	ACC	CIP	0	CA2	CA1	CA0	0	$13

This is a read only register used to monitor the status of the A/D converter. If an Address/Control Byte of $13 is sent to the A2, the Status Register will be addressed and will remain addressed until the CE pin is brought low. This provides efficient polling of the SR by allowing multiple reads of the SR with only one Address/Control Byte transmission.

Bits 0 and 4 of the SR are always read as lows. The significance of each of the other bits is:

B7, INT — Interrupt. In Modes 1 and 2, this bit is set high under the same conditions that the $\overline{INT}$ pin would be activated (see Conversion Modes). Once set, the INT bit can be cleared by reading the SR, reading any Data Register, or writing to the MSR or CSR. The INT bit is not affected by the state of the IE bit in the MSR.

B6, ACC — All Conversions Complete bit. When high, this status bit indicates that conversions have been completed on all channels selected in the CSR. It is cleared by reading any of the Data Registers or by writing to the MSR or CSR. In 10-bit mode, ACC = 1 implies that the DV bits of all active channels are true (see Data Registers). This bit is often used in Modes 2 and 3. In Mode 1, ACC will only be set if conversions are explicitly invoked (via writes to the SAR) for each channel selected in the CSR.

B5, CIP — Conversion In Progress bit. This bit is logically high when a conversion is initiated and goes low when a conversion completes. In the scanning modes, Modes 2 and 3, CIP will go low momentarily between successive channels and cannot be used in lieu of ACC in Mode 2.

NOTE: Following a write of $00 to the SAR, to terminate Mode 3 conversions, CIP may remain high until cleared with a write to the MSR or the CSR or with the read of a Data Register or with a write to the SAR with ENC or SAE = 1. CIP = 1 is not a true indication of an ongoing conversion. See “Mode 3 - Continuous Scan”

B3, CA2 — Channel Address Register, bit 2. CA2, CA1, and CA0 form a three bit binary number that indicates the current contents of the CAR. The CAR is originally set by the user via the SAR (see SAR). The CAR is automatically incremented following reads of Data Registers and following conversions in the scanning modes (Modes 2 and 3). The Status Register can be read at any time. Reading CA2 - CA0 during Modes 2 and 3 will produce changing channel addresses as the conversions proceed.

B2, CA1 Channel Address, bit 1. See discussion under CA2.

B1, CA0 Channel Address, bit 0. See discussion under CA2.

Data Registers

Address/Control: 0000000 to 0000111 - $00 to $0F

Read/Write: Read Only

High $\overline{H}$/L = 0	DV	DOV	0	0	0	0	D9	D8
	7	6	5	4	3	2	1	0
Low $\overline{H}$/L = 1	D7	D6	D5	D4	D3	D2	D1	D0
	7	6	5	4	3	2	1	0

The Data Registers are used to store the results of A/D conversions. There are two registers, a High Data Register and a Low Data Register, associated with each channel.

In 8-bit mode, the High Data Registers are inaccessible, and each Low Data Register holds the 8-bit result of the most recent conversion of its associated channel. The values range from $00 (AIn = V_{SS}) to a full scale reading of $FF. During multiple byte Data Register reads, the address (held in the CAR) is advanced to the Low Data Register of the next active channel (as specified in the CSR) following each read.

In 10-bit mode, bits 0 and 1 of the High Data Register together with the contents of the Low Data Register hold the result of the most recent conversion to the associated channel. The values range from $000 (AIn = V_{SS}) to a full scale reading of $3FF. During multiple byte Data Register reads, the address (held in the CAR) is automatically advanced from the High Data Register to the Low Data Register. Following a read of the Low Data Register, the address advances to the High Data Register of the next active channel (as specified in the CSR).

Two status flags are maintained for each channel. In 10-bit mode these status flags are provided in the High Data Register. In 8-bit mode they are not available to the user. Their functions are:

B7, DV The Data Valid bit indicates whether the corresponding channel has been converted since it was last read. DV is set upon completion of a conversion on the corresponding channel. DV is cleared by reading the Data Register or by a write to the MSR or the CSR.

NOTE: A write to the SAR does not clear the DV flag for each channel. This implies that if: conversion are completed on all registers selected in CSR; conversions stopped; an incomplete read of the Data Registers is performed; and conversions reinitiated with a write to the SAR - some DVs will still be set. In Mode 2, which terminates when all DVs are true (ACC goes true), unread channels may not be converted, unless CSR is written to, before setting ENC.

B6, DOV The Data Overrun (DOV) bit indicates that more than one conversion has been performed on a channel since it was last read. This bit is only valid in Modes 1 and 3. DOV is cleared by reading the Data Register or by performing a write to the CSR or the MSR.

Conversion Modes of the CDP68HC68A2

Mode 0 - Idle

On power_up, the MSR is reset to all 0's placing the A2 into Mode 0. After power_up, the user can effectively reset the A2 by selecting Mode 0 via the MSR. Setting the A2 to Mode 0, at any time, will abort any current conversions and force the $\overline{INT}$ pin to a high impedance state. In mode 0, if $\overline{EXT}$ is high in the MSR, the one pin, internal oscillator is placed in a low power, shutdown mode and internal clocking of the A/D converter is inhibited. If $\overline{EXT}$ is low in the MSR, internal clocking of the A/D converter is inhibited.

Mode 1 - Single Conversion

In Mode 1, conversions are performed on command. After setting Mode 1 in the MSR, a write to the SAR with ENC high will initiate a conversion on the channel currently selected by the CAR. Note: this channel does not have to be active in the CSR. When using the internal oscillator, the oscillator is enabled. The CIP flag in the SR will be set when the conversion begins.

Upon completion of the conversion, the INT bit in the SR will be set, the CIP flag will cleared, and, if IE is true in the MSR, the $\overline{INT}$ pin will be driven low (if all channels specified in the CSR have been converted since the last Data Register read the ACC bit in the SR will also be set). Finally, if it's active, the internal oscillator will be stopped.

Another conversion can be initiated with a write to the SAR. However, the normal procedure is to read the results of the first conversion. This does two things: first it clears the INT flag (the $\overline{INT}$ pin is returned to a high impedance state); second a conversion is automatically started on the next channel selected in the CSR. This read-convert pattern can be continued indefinitely.

When reading Data Registers in Mode 1, the user can be certain that the contents of the CAR equal the channel number which was just converted. Thus the Address/Control Byte sent prior to the read will automatically match the CAR. If a read from a Data Register, other than the one just converted, is performed, the CAR must be set to the desired register prior to sending the Address/Control Byte. Setting CAR is done by writing the SAR with ENC = 0, SAE = 1, and the CA2 - CA0 bits equal to the desired channel.

Mode 2 - Single Scan

In mode 2, when ENC is set in the SAR, conversions are performed on all channels selected in the CSR. Conversions begin on the channel specified by the CAR (this channel does not have to be active in the CSR) and proceed in ascending order until all channels selected in the CSR have been converted. If the starting channel is not the lowest active channel, when the highest active channel is done converting, the CAR advances to the lowest active channel and continues from that point until all channels have been converted once.

When ENC is set i n the SAR, the internal clock is activated (if selected), the CIP flag is set in the SR, and conversions begin. The CIP flag doesn't remain high, as it momentarily goes low between each channel conversion.

When all channels have been converted the INT and ACC flags in the SR are set, the $\overline{INT}$ pin is driven low (if IE is true in the MSR), the CIP flag is cleared, and, if active, the internal oscillator is disabled.

Data Registers can safely be read after all channels have been converted. If the starting channel was a channel active in the CSR then the CAR will one again be pointing to that channel (providing all channels had been read or CSR or MSR written since the last set of conversions - see Note below). IF a read from a Data Register, other than the one first converted, is performed, the CAR must be set to the desired register prior to sending the Address/Control Byte. Setting CAR is done by writing the SAR with ENC = 0, SAE = 1, and the CA2 - CA0 bits equal to the desired channel.

NOTE: A write to the SAR does not clear the DV flag for each channel. This implies that if: conversions are completed on all registers selected in CSR; conversions stopped; an incomplete read of the Data Registers is performed; and conversions reinitiated with a write to the SAR - some DVs will still be set. In Mode 2, which terminates when all DVs are true (ACC goes true), unread channels may not be converted unless CSR is written to before setting ENC.

There are two ways to prematurely stop conversions in Mode 2. The first is to perform any “abort” action (see Abort Modes). Performing an abort, may produce spurious conversion values. The second, and preferred means to stop a Mode 2 conversion, is to clear the ENC bit by writing a $00 to the SAR. Clearing ENC will synchronously stop conversions at the end of the current conversion. When prematurely stopping conversions, CIP is not valid. The CIP flag cannot be used to determine when the current conversion is complete. Instead, a time delay equal to one conversion time must be built into the software. The appropriate delay will ensure the last conversion is complete before Data Register reads begin.

Prematurely stopping the conversions leaves the CAR in an unknown state. One remaining task, before Data Registers are read, is to be certain the contents of the CAR match the address sent in the Address/Control Byte. This is done by jamming the CAR with a write to the SAR with ENC = 0, SAE = 1, CA3 - C A2 - CA0 equal to the desired channel address.

Mode 3 - Continuous Scan

In Mode 3, when ENC is set in the SAR, conversions are performed on all channels selected in the CSR. COnversion begin on the channel specified by the CAR (this channel does not have to be active in the CSR) and proceed in ascending order for all channels selected in the CSR. Each time the highest active channel is done converting, the CAR advances to the lowest active channel and continues from that point.

When ENC is set in the SAR, the internal clock is activated (if selected) and conversions begin.

When all channels have been converted one time the ACC flag in the SR is set. This is the only valid status flag in Mode 3. The CIP flag is not valid in Mode 3. The INT flag and the $\overline{INT}$ pin are both held in a disabled state during Mode 3.

Data Registers cannot be read until Mode 3 conversions have been terminated. There are two ways to stop conversions in Mode 3. The first is to perform any “abort” action (see Abort Modes). Performing an abort, may produce spurious conversion values. The second, and preferred means to stop a Mode 3 conversion, is to clear the ENC bit by writing a $00 to the SAR. Clearing ENC will synchronously stop conversions at the end of the current conversion. CIP is not valid following the clearing of ENC. The CIP flag cannot be used to determine when the current conversion is complete. Instead, a time delay equal to one conversion time must be built into the software. The appropriate delay will ensure the last conversion is complete before Data Register reads begin.

The Data Registers can safely be read after ENC is cleared and one conversion time has elapsed. One remaining task is to be certain the contents of the CAR match the address sent in the Address/Control Byte. This is done by jamming the CAR with a write to the SAR with ENC = 0, SAE = 1, and CA2 - CA0 equal to the desired channel address.

Abort Modes

Any active mode can be aborted by any one of the following means:

1. A write to the MSR
2. A write to the CSR
3. A write to the SAR with ENC and/or SAE = 1
4. A read of any Data Register

The contents of Data Registers are not guaranteed following an abort. Writing a $00 to the MSR is equivalent to a reset.

To synchronously stop conversions in Modes 2 or 3 set the SAR to $00 (See Mode 2 and Mode 3).

Analog Inputs

Shown in Figure 5 is a simplified equivalent circuit representing the input to the Analog to Digital Converter through the multiplexer as seen from each AIn pin.

Due to the nature of the switched capacitor array used by the successive approximation A/D, two important points are noted here:

1. A property of capacitive input is the intrinsic sample and hold function. This provides all that is necessary to accurately sample a point on an input waveform within the input bandwidth shown in the specifications (under 1.5 conversion oscillator cycles).
2. The input to the capacitor network appears as an RC network with a time constant and therefore places constraints on the source impedance. The charging time and therefore the accuracy of the conversion will be adversely affected by increasing the source impedance.

It is recommended to set the conversion oscillator frequency in accordance with the input impedance in order to allow sufficient time (the 1.5 T_{OSC} cycles) to sample a changing waveform through the modeled input low pass filter network which includes the input source in a series circuit with the internal impedance.

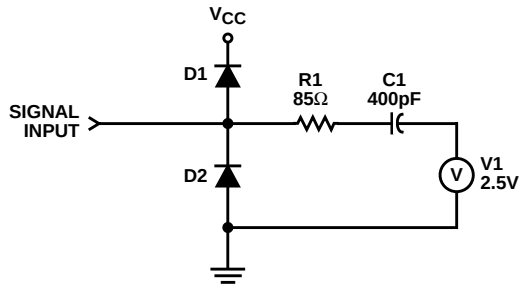


FIGURE 5A. ANALOG INPUT DURING SAMPLE TIME

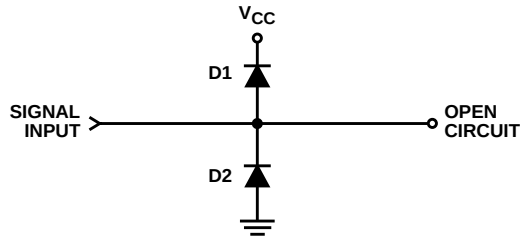


FIGURE 5B. ANALOG INPUT DURING HOLD AND IDLE TIME

The time constant (τ) for the input network is $R_{EFF}C_{NET}$.

$R_{EFF} = R_S + R_{NET}$, $C_{NET} = 400pF$, and $R_{NET} = 50\Omega$.
$\tau = R_{EFF}C_{NET} = (R_S + 50\Omega)\ 400pF$.

8τ is required during the first 1.5 sample clock cycles to sufficiently encode 10-bit conversion. Therefore, $1.5\ T_S \geq 8\tau$ and $T_S \geq 5.33\ R_{EFF}C$.

$T_S = 1/f_{SAMPLE}$,
then $f_{SAMPLE} \leq [5.33\ (R_S + 85\Omega)\ 400pF] - 1$,
$f_{SAMPLE} \leq (4.688 \times 10^8)/(R_S + 85\Omega)$.

For example, if R_S = 1000, f_{SAMPLE} must be less than 432kHz, and T_S = 2.3µs. This yields a 10-bit conversion time of 32µs. An internal $C_{OSC} \geq 68pF$, see chart.

The maximum frequency is limited by the device specification (see characteristics) and by the (R_S) Series input resistance:

$R_S \leq [(4.688 \times 10^8)/f_{SAMPLE}] - 85\Omega$.

For example, for a 1MHz sample clock R_S max = 385Ω.

The Internal Schmitt Oscillator

Figure 6 shows a simplified model of the Schmitt oscillator used to help familiarize the user with its operation. Table 2 shows typical internal oscillator frequency versus capacitance at 5V and 25°C.

TABLE 2. TYPICAL OSCILLATOR FREQUENCY vs CAPACITANCE AT V_{DD} = 5V, T_A = 25°C

C(pF)	f(MHz)	C(pF)	f(MHz)
18	1.0 - 3.0	218	0.148 - 0.40
38	0.65 - 2.0	318	0.111 - 0.25
48	0.54 - 1.6	409	0.107 - 0.23
68	0.38 - 1.1	528	0.072 - 0.17
118	0.26 - 0.75	1018	0.040 - 0.10

When measuring the oscillator, probe capacitance will affect frequency. An alternative to direct frequency measurement of the oscillator input is to measure the interval between successive interrupts in modes 1 and 2.

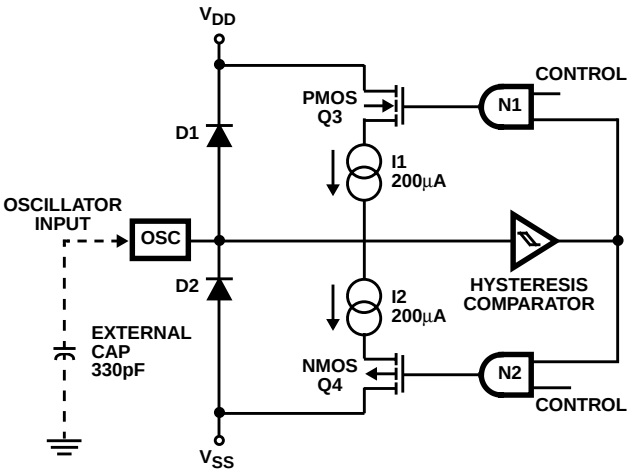
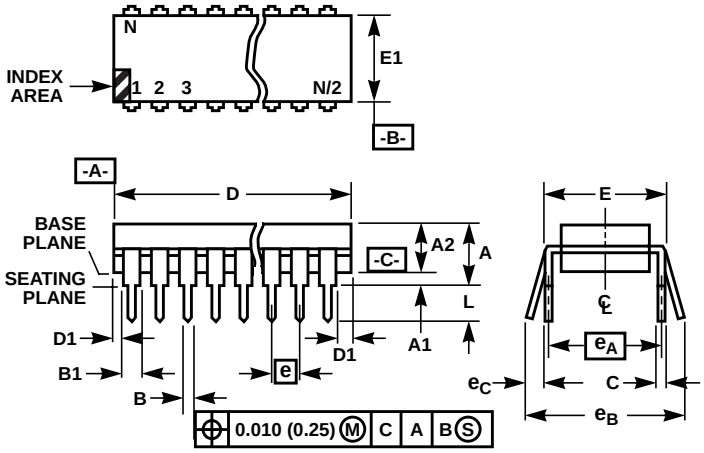


FIGURE 6. EQUIVALENT CIRCUIT FOR OSCILLATOR INPUT

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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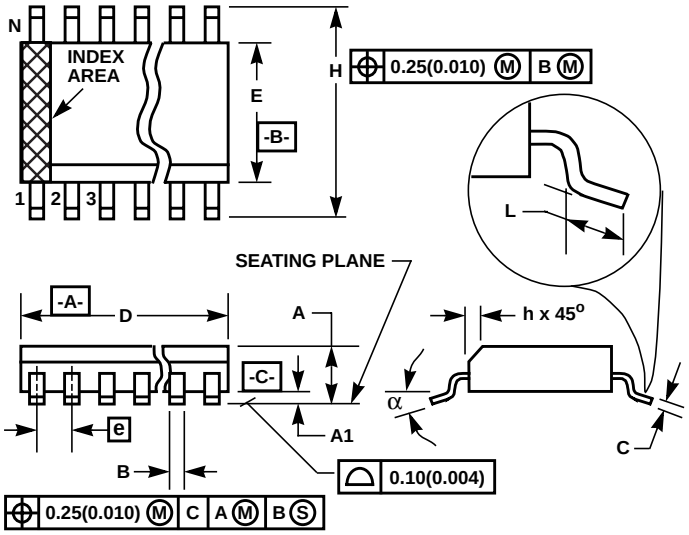
Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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