

Features

- High-Voltage Type (20V Rating)
- Medium Speed Operation: 8MHz (Typ.) at CL = 50pF and VDD - VSS = 10V
- Multi-Package Parallel Clocking for Synchronous High Speed Output Response or Ripple Clocking for Slow Clock Input Rise and Fall Times
- "Preset Enable" and Individual "Jam" Inputs Provided
- Binary or Decade Up/Down Counting
- BCD Outputs in Decade Mode
- 100% Tested for Maximum Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics
- Maximum Input Current of 1 μ A at 18V Over Full Package-Temperature Range; 100nA at 18V and +25 $^{\circ}$ C
- Noise Margin (Over Full Package Temperature Range):
 - 1V at VDD = 5V
 - 2V at VDD = 10V
 - 2.5V at VDD = 15V
- Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Device's

Applications

- Programmable Binary and Decade Counting/Frequency Synthesizers-BCD Output
- Analog to Digital and Digital to Analog Conversion
- Up/Down Binary Counting
- Difference Counting
- Magnitude and Sign Generation
- Up/Down Decade Counting

Description

CD4029BMS consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, $\overline{\text{CARRY-IN}}$ ($\overline{\text{CLOCK ENABLE}}$), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals. Q1, Q2, Q3, Q4 and a CARRY OUT signal are provided as outputs.

A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the $\overline{\text{CARRY-IN}}$ and PRE-SET ENABLE signals are low. Advancement is inhibited when the $\overline{\text{CARRY-IN}}$ or PRESET ENABLE signals are high. The $\overline{\text{CARRY-OUT}}$ signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the $\overline{\text{CARRY-IN}}$ signal is low. The $\overline{\text{CARRY-IN}}$ signal in the low state can thus be considered a $\overline{\text{CLOCK ENABLE}}$. The $\overline{\text{CARRY-IN}}$ terminal must be connected to VSS when not in use.

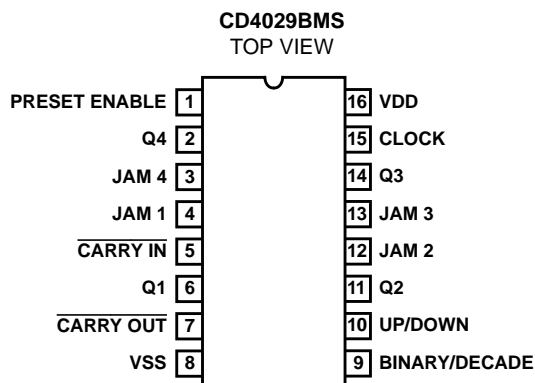
Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts up when the UP/DOWN input is high, and down when the UP/DOWN input is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in Figure 17.

Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

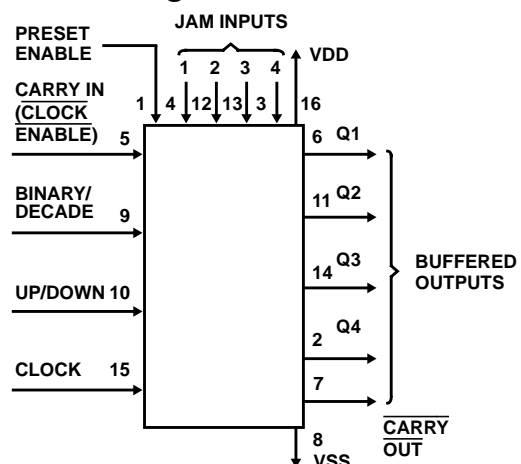
The CD4029BMS is supplied in these 16-lead outline packages:

- Braze Seal DIP H4X
- Frit Seal DIP H1F
- Ceramic Flatpack H6W

Pinout



Functional Diagram



Specifications CD4029BMS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) -0.5V to +20V
 (Voltage Referenced to VSS Terminals)
 Input Voltage Range, All Inputs -0.5V to VDD +0.5V
 DC Input Current, Any One Input ±10mA
 Operating Temperature Range -55°C to +125°C
 Package Types D, F, K, H
 Storage Temperature Range (TSTG) -65°C to +150°C
 Lead Temperature (During Soldering) +265°C
 At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for
 10s Maximum

Reliability Information

Thermal Resistance θ_{ja} θ_{jc}
 Ceramic DIP and FRIT Package 80°C/W 20°C/W
 Flatpack Package 70°C/W 20°C/W
 Maximum Package Power Dissipation (PD) at +125°C
 For TA = -55°C to +100°C (Package Type D, F, K) 500mW
 For TA = +100°C to +125°C (Package Type D, F, K) Derate
 Linearity at 12mW/°C to 200mW
 Device Dissipation per Output Transistor 100mW
 For TA = Full Package Temperature Range (All Package Types)
 Junction Temperature +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS (NOTE 1) | | GROUP A SUBGROUPS | TEMPERATURE | LIMITS | | UNITS |
|-----------------------------|--------|------------------------------------|-----------|----------------------|----------------------|----------------|----------------|-------|
| | | | | | | MIN | MAX | |
| Supply Current | IDD | VDD = 20V, VIN = VDD or GND | | 1 | +25°C | - | 10 | μA |
| | | | | 2 | +125°C | - | 1000 | μA |
| | | VDD = 18V, VIN = VDD or GND | | 3 | -55°C | - | 10 | μA |
| Input Leakage Current | IIL | VIN = VDD or GND | VDD = 20 | 1 | +25°C | -100 | - | nA |
| | | | VDD = 18V | 2 | +125°C | -1000 | - | nA |
| | | | | 3 | -55°C | -100 | - | nA |
| Input Leakage Current | IIH | VIN = VDD or GND | VDD = 20 | 1 | +25°C | - | 100 | nA |
| | | | VDD = 18V | 2 | +125°C | - | 1000 | nA |
| | | | | 3 | -55°C | - | 100 | nA |
| Output Voltage | VOL15 | VDD = 15V, No Load | | 1, 2, 3 | +25°C, +125°C, -55°C | - | 50 | mV |
| Output Voltage | VOH15 | VDD = 15V, No Load (Note 3) | | 1, 2, 3 | +25°C, +125°C, -55°C | 14.95 | - | V |
| Output Current (Sink) | IOL5 | VDD = 5V, VOUT = 0.4V | | 1 | +25°C | 0.53 | - | mA |
| Output Current (Sink) | IOL10 | VDD = 10V, VOUT = 0.5V | | 1 | +25°C | 1.4 | - | mA |
| Output Current (Sink) | IOL15 | VDD = 15V, VOUT = 1.5V | | 1 | +25°C | 3.5 | - | mA |
| Output Current (Source) | IOH5A | VDD = 5V, VOUT = 4.6V | | 1 | +25°C | - | -0.53 | mA |
| Output Current (Source) | IOH5B | VDD = 5V, VOUT = 2.5V | | 1 | +25°C | - | -1.8 | mA |
| Output Current (Source) | IOH10 | VDD = 10V, VOUT = 9.5V | | 1 | +25°C | - | -1.4 | mA |
| Output Current (Source) | IOH15 | VDD = 15V, VOUT = 13.5V | | 1 | +25°C | - | -3.5 | mA |
| N Threshold Voltage | VNTH | VDD = 10V, ISS = -10μA | | 1 | +25°C | -2.8 | -0.7 | V |
| P Threshold Voltage | VPTH | VSS = 0V, IDD = 10μA | | 1 | +25°C | 0.7 | 2.8 | V |
| Functional | F | VDD = 2.8V, VIN = VDD or GND | | 7 | +25°C | VOH > VDD/2 | VOL < VDD/2 | V |
| | | VDD = 20V, VIN = VDD or GND | | 7 | +25°C | | | |
| | | VDD = 18V, VIN = VDD or GND | | 8A | +125°C | | | |
| | | VDD = 3V, VIN = VDD or GND | | 8B | -55°C | | | |
| Input Voltage Low (Note 2) | VIL | VDD = 5V, VOH > 4.5V, VOL < 0.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | - | 1.5 | V |
| Input Voltage High (Note 2) | VIH | VDD = 5V, VOH > 4.5V, VOL < 0.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | 3.5 | - | V |
| Input Voltage Low (Note 2) | VIL | VDD = 15V, VOH > 13.5V, VOL < 1.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | - | 4 | V |
| Input Voltage High (Note 2) | VIH | VDD = 15V, VOH > 13.5V, VOL < 1.5V | | 1, 2, 3 | +25°C, +125°C, -55°C | 11 | - | V |

NOTES: 1. All voltages referenced to device GND, 100% testing being implemented. 3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.
 2. Go/No Go test with limits applied to inputs.

Specifications CD4029BMS

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS (NOTE 1, 2) | GROUP A SUBGROUPS | TEMPERATURE | LIMITS | | UNITS |
|---|----------------|----------------------------|----------------------|---------------|--------|-----|-------|
| | | | | | MIN | MAX | |
| Propagation Delay Clock To Q Output | TPHL1 TPLH1 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 500 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 675 | ns |
| Propagation Delay Clock To Carry Out | TPHL2 TPLH2 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 560 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 756 | ns |
| Propagation Delay Preset Enable To Q | TPHL3 TPLH3 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 470 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 635 | ns |
| Propagation Delay Preset Enable To Carry- Out | TPHL4 TPLH4 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 640 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 864 | ns |
| Propagation Delay Carry-In To Carry-Out | TPHL5 TPLH5 | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 340 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 459 | ns |
| Transition Time Q Output | TTHL TTLH | VDD = 5V, VIN = VDD or GND | 9 | +25°C | - | 200 | ns |
| | | | 10, 11 | +125°C, -55°C | - | 270 | ns |
| Maximum Clock Input Frequency | FCL | VDD = 5V, VIN = VDD or GND | 9 | +25°C | 2 | - | MHz |
| | | | 10, 11 | +125°C, -55°C | 1.48 | - | MHz |

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|-------------------------|--------|-----------------------------|-------|-------------------------|--------|-------|-------|
| | | | | | MIN | MAX | |
| Supply Current | IDD | VDD = 5V, VIN = VDD or GND | 1, 2 | -55°C, +25°C | - | 5 | μA |
| | | | | +125°C | - | 150 | μA |
| | | VDD = 10V, VIN = VDD or GND | 1, 2 | -55°C, +25°C | - | 10 | μA |
| | | | | +125°C | - | 300 | μA |
| | | | | -55°C, +25°C | - | 10 | μA |
| +125°C | - | 600 | μA | | | | |
| Output Voltage | VOL | VDD = 5V, No Load | 1, 2 | +25°C, +125°C, -55°C | - | 50 | mV |
| Output Voltage | VOL | VDD = 10V, No Load | 1, 2 | +25°C, +125°C, -55°C | - | 50 | mV |
| Output Voltage | VOH | VDD = 5V, No Load | 1, 2 | +25°C, +125°C, -55°C | 4.95 | - | V |
| Output Voltage | VOH | VDD = 10V, No Load | 1, 2 | +25°C, +125°C, -55°C | 9.95 | - | V |
| Output Current (Sink) | IOL5 | VDD = 5V, VOUT = 0.4V | 1, 2 | +125°C | 0.36 | - | mA |
| | | | | -55°C | 0.64 | - | mA |
| Output Current (Sink) | IOL10 | VDD = 10V, VOUT = 0.5V | 1, 2 | +125°C | 0.9 | - | mA |
| | | | | -55°C | 1.6 | - | mA |
| Output Current (Sink) | IOL15 | VDD = 15V, VOUT = 1.5V | 1, 2 | +125°C | 2.4 | - | mA |
| | | | | -55°C | 4.2 | - | mA |
| Output Current (Source) | IOH5A | VDD = 5V, VOUT = 4.6V | 1, 2 | +125°C | - | -0.36 | mA |
| | | | | -55°C | - | -0.64 | mA |

Specifications CD4029BMS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|---|----------------|-------------------------------|---------|----------------------|--------|-------|-------|
| | | | | | MIN | MAX | |
| Output Current (Source) | IOH5B | VDD = 5V, VOUT = 2.5V | 1, 2 | +125°C | - | -1.15 | mA |
| | | | | -55°C | - | -2.0 | mA |
| Output Current (Source) | IOH10 | VDD = 10V, VOUT = 9.5V | 1, 2 | +125°C | - | -0.9 | mA |
| | | | | -55°C | - | -2.6 | mA |
| Output Current (Source) | IOH15 | VDD = 15V, VOUT = 13.5V | 1, 2 | +125°C | - | -2.4 | mA |
| | | | | -55°C | - | -4.2 | mA |
| Input Voltage Low | VIL | VDD = 10V, VOH > 9V, VOL < 1V | 1, 2 | +25°C, +125°C, -55°C | - | 3 | V |
| Input Voltage High | VIH | VDD = 10V, VOH > 9V, VOL < 1V | 1, 2 | +25°C, +125°C, -55°C | 7 | - | V |
| Propagation Delay Q Output | TPHL1 TPLH1 | VDD = 10V | 1, 2, 3 | +25°C | - | 240 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 180 | ns |
| Propagation Delay Carry Output | TPHL2 TPLH2 | VDD = 10V | 1, 2, 3 | +25°C | - | 260 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 190 | ns |
| Propagation Delay Preset Enable To Q | TPHL3 TPLH3 | VDD = 10V | 1, 2, 3 | +25°C | - | 200 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 160 | ns |
| Propagation Delay Preset Enable To Carry- Out | TPHL4 TPLH4 | VDD = 10V | 1, 2, 3 | +25°C | - | 290 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 210 | ns |
| Propagation Delay Carry In To Carry Out | TPHL5 TPLH5 | VDD = 10V | 1, 2, 3 | +25°C | - | 140 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 100 | ns |
| Transition Time | TTHL TTLH | VDD = 10V | 1, 2, 3 | +25°C | - | 100 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 80 | ns |
| Maximum Clock Input Frequency | FCL | VDD = 10V | 1, 2, 3 | +25°C | 4 | - | MHz |
| | | VDD = 15V | 1, 2, 3 | +25°C | 5.5 | - | MHz |
| Minimum Data Setup Time Note 4 | TS | VDD = 5V | 1, 2, 3 | +25°C | - | 340 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 140 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 100 | ns |
| Clock Rise And Fall Time Note 5 | TRCL TFCL | VDD = 5V | 1, 2, 3 | +25°C | - | 15 | μs |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 15 | μs |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 15 | μs |
| Minimum Clock Pulse Width | TW | VDD = 5V | 1, 2, 3 | +25°C | - | 180 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 90 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 60 | ns |
| Minimum Carry In Setup Time Note 6 | TS | VDD = 5V | 1, 2, 3 | +25°C | - | 200 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 70 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 60 | ns |
| Minimum Carry Input Hold Time Note 6 | TH | VDD = 5V | 1, 2, 3 | +25°C | - | 50 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 30 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 25 | ns |
| Minimum Preset Enable Removal Time Note 4 | TREM | VDD = 5V | 1, 2, 3 | +25°C | - | 200 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 110 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 80 | ns |

Specifications CD4029BMS

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|-----------------------------------|--------|------------|---------|-------------|--------|-----|-------|
| | | | | | MIN | MAX | |
| Minimum Preset Enable Pulse Width | TW | VDD = 5V | 1, 2, 3 | +25°C | - | 130 | ns |
| | | VDD = 10V | 1, 2, 3 | +25°C | - | 70 | ns |
| | | VDD = 15V | 1, 2, 3 | +25°C | - | 50 | ns |
| Input Capacitance | CIN | Any Input | 1, 2 | +25°C | - | 7.5 | pF |

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. From Up/Down, Binary/Decode, Carry In, or Preset Enable Control Inputs to Clock Edge.
5. If more than one unit is cascaded in the parallel clocked application, tr CL should be made ≤ the sum of the fixed propagation delay at 15pF and the transition time of the carry output driving stage for the estimated capacitive load. This measurement was made with a decoupling capacitor (>1μF) between VDD and VSS.
6. From Carry In to Clock Edge.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|---------------------------|--------------|-----------------------------|------------|-------------|-------------|--------------------|-------|
| | | | | | MIN | MAX | |
| Supply Current | IDD | VDD = 20V, VIN = VDD or GND | 1, 4 | +25°C | - | 25 | μA |
| N Threshold Voltage | VNTH | VDD = 10V, ISS = -10μA | 1, 4 | +25°C | -2.8 | -0.2 | V |
| N Threshold Voltage Delta | ΔVTN | VDD = 10V, ISS = -10μA | 1, 4 | +25°C | - | ±1 | V |
| P Threshold Voltage | VTP | VSS = 0V, IDD = 10μA | 1, 4 | +25°C | 0.2 | 2.8 | V |
| P Threshold Voltage Delta | ΔVTP | VSS = 0V, IDD = 10μA | 1, 4 | +25°C | - | ±1 | V |
| Functional | F | VDD = 18V, VIN = VDD or GND | 1 | +25°C | VOH > VDD/2 | VOL < VDD/2 | V |
| | | VDD = 3V, VIN = VDD or GND | | | | | |
| Propagation Delay Time | TPHL TPLH | VDD = 5V | 1, 2, 3, 4 | +25°C | - | 1.35 x +25°C Limit | ns |

- NOTES:**
1. All voltages referenced to device GND.
 2. CL = 50pF, RL = 200K, Input TR, TF < 20ns
 3. See Table 2 for +25°C limit.
 4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

| PARAMETER | SYMBOL | DELTA LIMIT |
|-------------------------|--------|--------------------------|
| Supply Current - MSI-2 | IDD | ± 1.0μA |
| Output Current (Sink) | IOL5 | ± 20% x Pre-Test Reading |
| Output Current (Source) | IOH5A | ± 20% x Pre-Test Reading |

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TABLE 6. APPLICABLE SUBGROUPS

| CONFORMANCE GROUP | | MIL-STD-883 METHOD | GROUP A SUBGROUPS | READ AND RECORD |
|-------------------------------|--------------|--------------------|---------------------------------------|------------------------------|
| Initial Test (Pre Burn-In) | | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| Interim Test 1 (Post Burn-In) | | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| Interim Test 2 (Post Burn-In) | | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| PDA (Note 1) | | 100% 5004 | 1, 7, 9, Deltas | |
| Interim Test 3 (Post Burn-In) | | 100% 5004 | 1, 7, 9 | IDD, IOL5, IOH5A |
| PDA (Note 1) | | 100% 5004 | 1, 7, 9, Deltas | |
| Final Test | | 100% 5004 | 2, 3, 8A, 8B, 10, 11 | |
| Group A | | Sample 5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 | |
| Group B | Subgroup B-5 | Sample 5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas | Subgroups 1, 2, 3, 9, 10, 11 |
| | Subgroup B-6 | Sample 5005 | 1, 7, 9 | |
| Group D | | Sample 5005 | 1, 2, 3, 8A, 8B, 9 | Subgroups 1, 2 3 |

NOTE: 1. 5% Parametric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

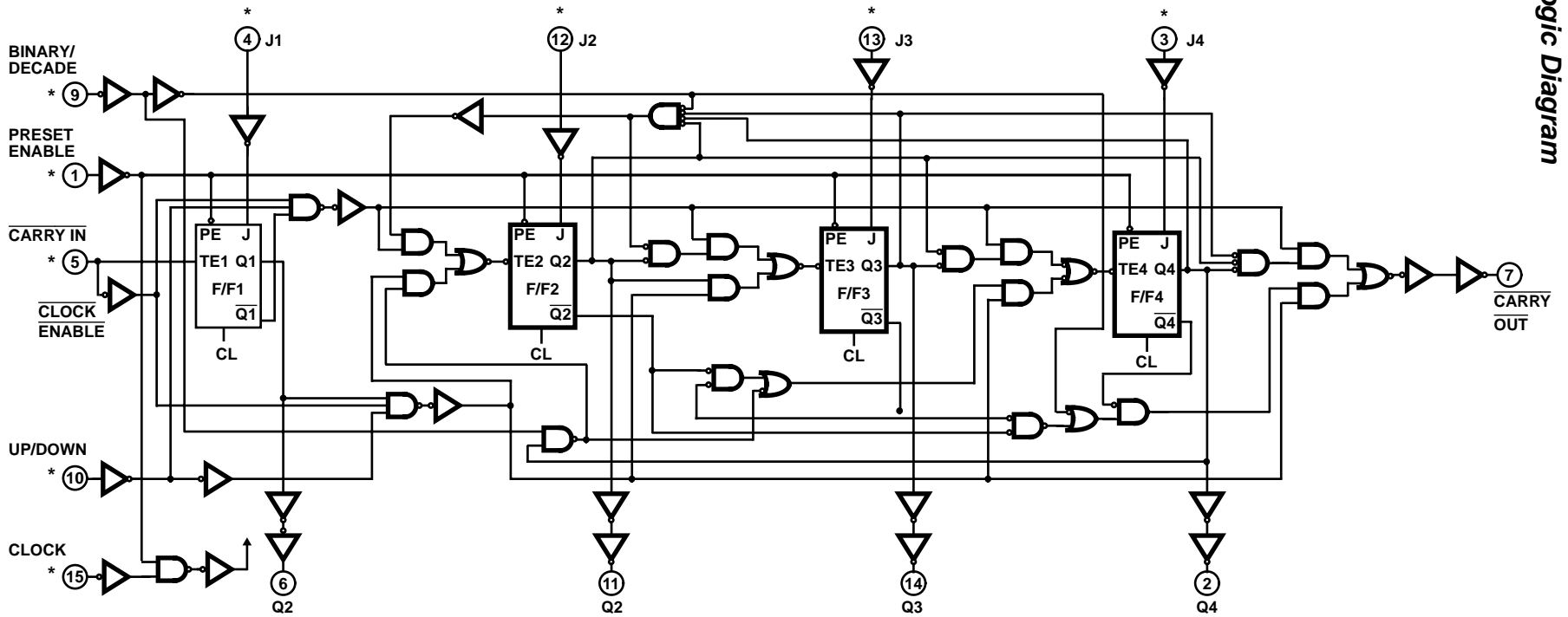
| CONFORMANCE GROUPS | MIL-STD-883 METHOD | TEST | | READ AND RECORD | |
|--------------------|--------------------|-----------|------------|-----------------|------------|
| | | PRE-IRRAD | POST-IRRAD | PRE-IRRAD | POST-IRRAD |
| Group E Subgroup 2 | 5005 | 1, 7, 9 | Table 4 | 1, 9 | Table 4 |

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

| FUNCTION | OPEN | GROUND | VDD | 9V ± -0.5V | OSCILLATOR | |
|----------------------------|-----------------|---------------------------------|------------------------------------|-----------------|------------|-------|
| | | | | | 50kHz | 25kHz |
| Static Burn-In 1 Note 1 | 2, 6, 7, 11, 14 | 1, 3 - 5, 8 - 10, 12, 13, 15 | 16 | | | |
| Static Burn-In 2 Note 1 | 2, 6, 7, 11, 14 | 8 | 1, 3 - 5, 9, 10, 12, 13, 15, 16 | | | |
| Dynamic Burn-In Note 1 | - | 1, 3 - 5, 8, 12, 13 | 9, 10, 16 | 2, 6, 7, 11, 14 | 15 | - |
| Irradiation Note 2 | 2, 6, 7, 11, 14 | 8 | 1, 3 - 5, 9, 10, 12, 13, 15, 16 | | | |

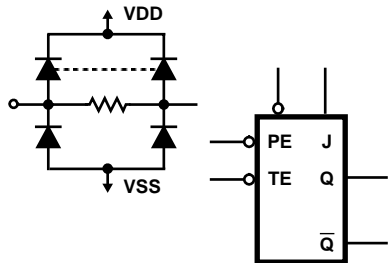
NOTE:

- Each pin except VDD and GND will have a series resistor of $10K \pm 5\%$, $VDD = 18V \pm 0.5V$
- Each pin except VDD and GND will have a series resistor of $47K \pm 5\%$; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, $VDD = 10V \pm 0.5V$



7-804

*ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK



TRUTH TABLE

| CLOCK | TE | PE | J | Q | \bar{Q} | |
|-------|----|----|---|-----------|-----------|----|
| X | X | 0 | 0 | 0 | 1 | |
| | 0 | 1 | X | \bar{Q} | Q | |
| X | X | 0 | 1 | 1 | 0 | |
| | 1 | 1 | X | Q | \bar{Q} | NC |
| | X | 1 | X | Q | Q | NC |

X = Don't Care

FUNCTION TABLE

| CONTROL INPUT | LOGIC LEVEL | ACTION |
|---|-------------|--|
| BIN/DEC (B/D) | 1 | Binary Count |
| BIN/DEC (B/D) | 0 | Decade Count |
| UP/DOWN (U/D) | 1 | Up Count |
| UP/DOWN (U/D) | 0 | Down Count |
| Preset Enable (PE) | 1 | Jam In |
| Preset Enable (PE) | 0 | No Jam |
| $\overline{\text{CARRY IN}} (\bar{C}_i)$ (CLOCK ENABLE) | 1 | No Counter Advance at POS Clock Transition |
| $\overline{\text{CARRY IN}} (\bar{C}_i)$ (CLOCK ENABLE) | 0 | Advance Counter at POS Clock Transition |

FIGURE 1.

Typical Performance Characteristics

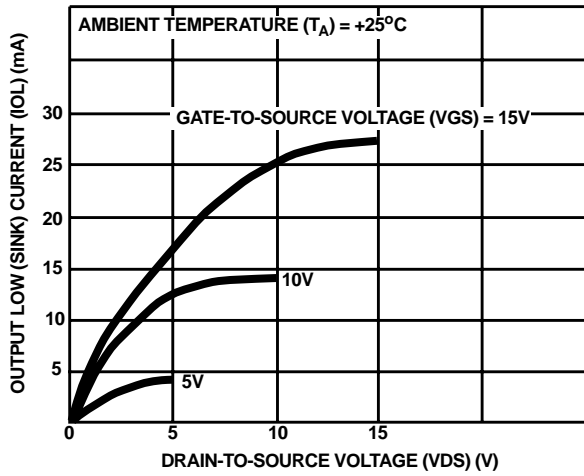


FIGURE 2. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

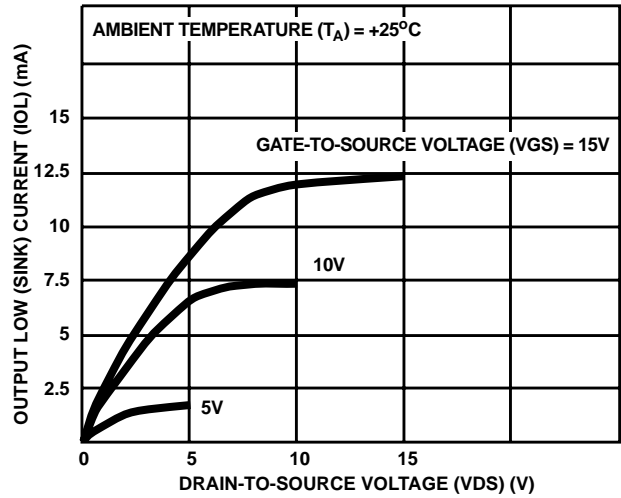


FIGURE 3. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

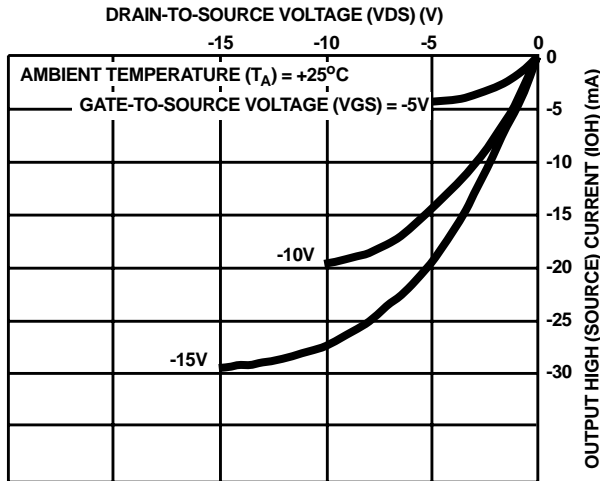


FIGURE 4. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

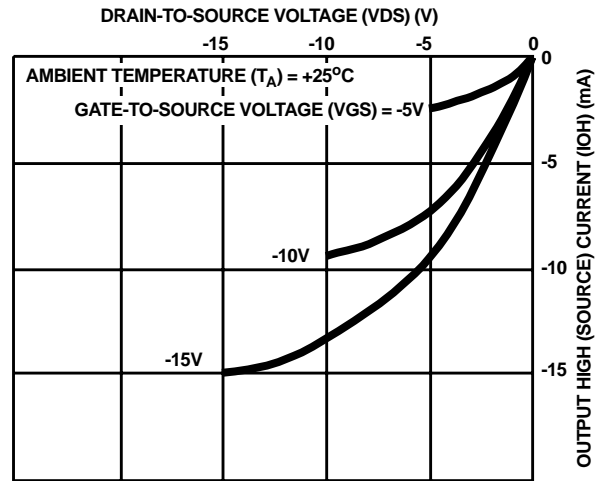


FIGURE 5. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

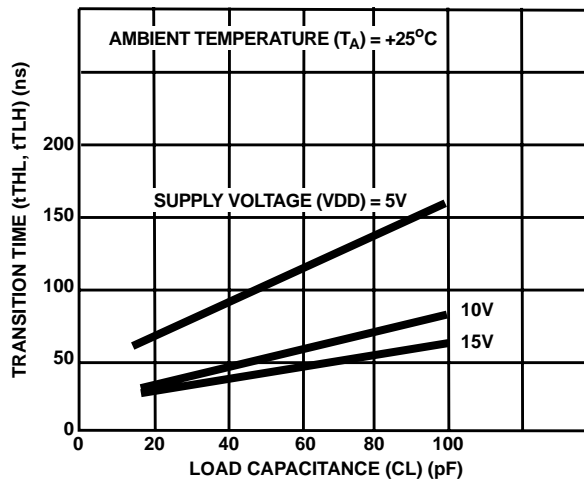


FIGURE 6. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

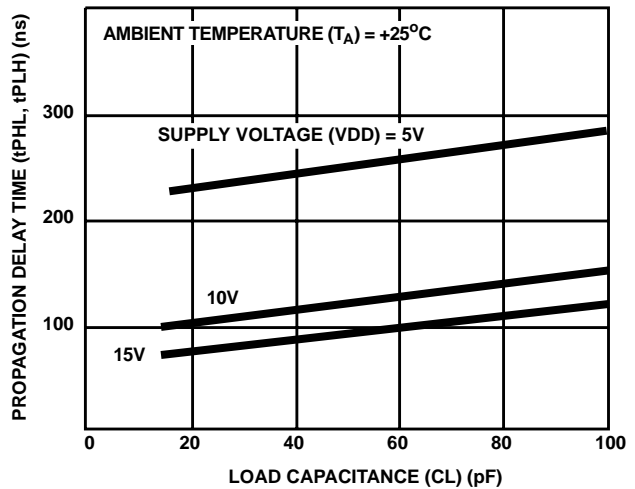


FIGURE 7. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (Q OUTPUT)

Typical Performance Characteristics (Continued)

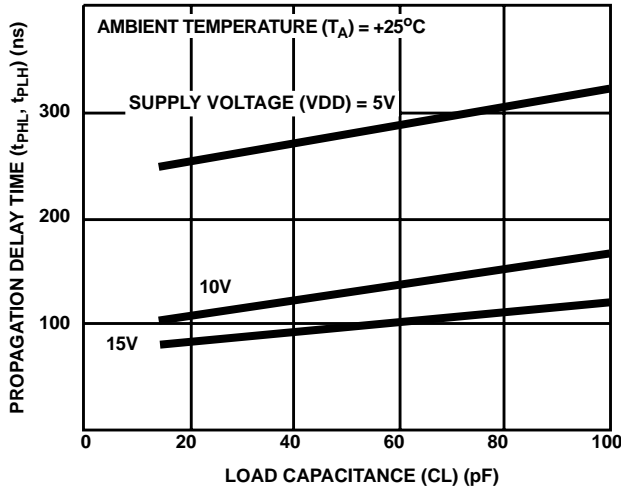


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (CARRY OUTPUT)

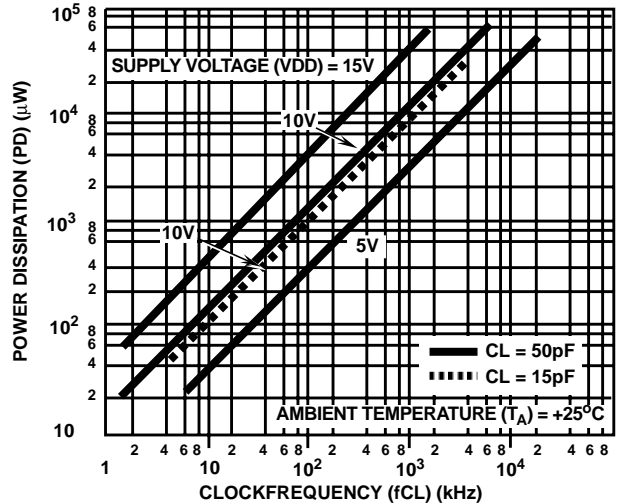
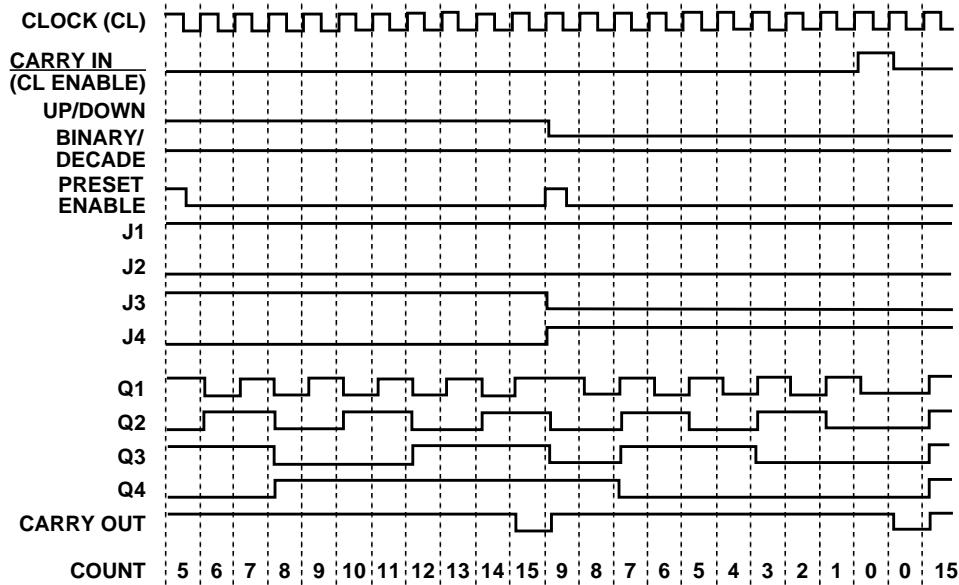


FIGURE 9. TYPICAL POWER DISSIPATION AS A FUNCTION OF FREQUENCY

Timing Diagrams



The CD4029BMS CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the CD4029BMS CLOCK and UP/DOWN inputs can easily be realized by use of the circuit in Figure 11.

CD4029BMS changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration in Figure 12, when counting up the CLOCK DOWN input must be maintained high and conversely when counting down the CLOCK UP input must be maintained high.

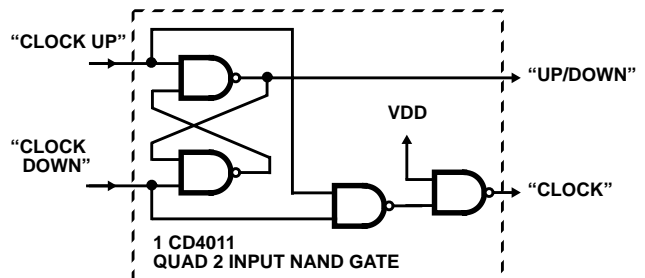


FIGURE 11. CONVERSION OF CLOCK UP, CLOCK DOWN INPUT SIGNALS TO CLOCK AND UP/DOWN INPUT SIGNALS

CD4029BMS

Timing Diagrams (Continued)

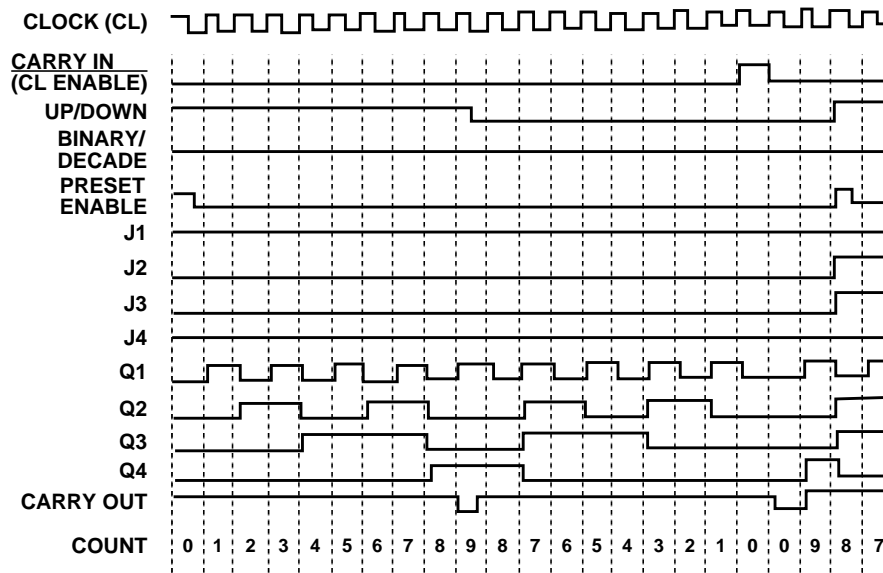
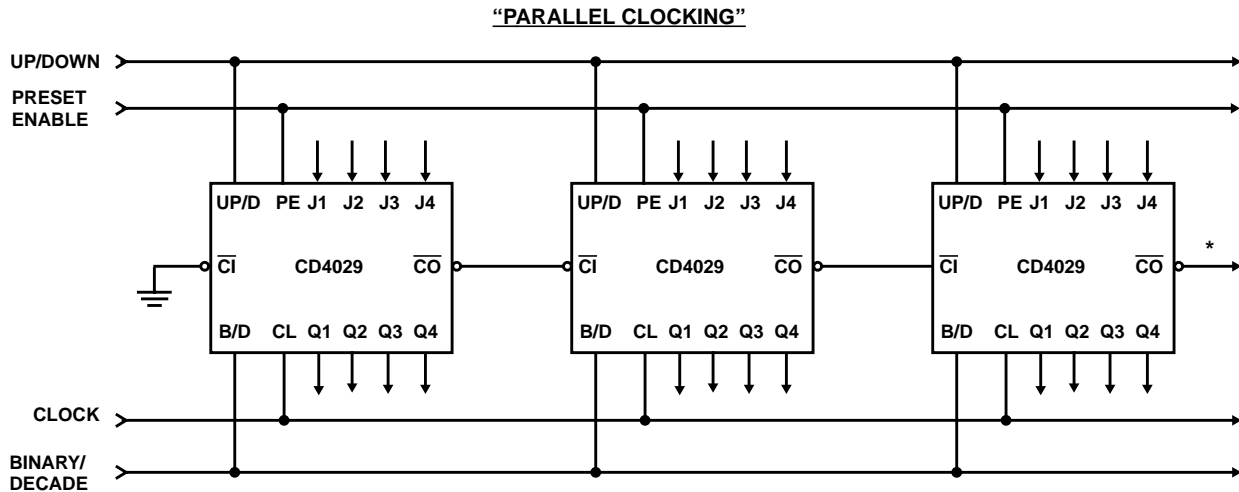


FIGURE 12. TIMING DIAGRAM-DECADE MODE



*CARRY OUT LINES AT THE 2ND, 3RD, ETC, STAGES MAY HAVE A NEGATIVE-GOING GLITCH PULSE RESULTING FROM DIFFERENTIAL DELAYS OF DIFFERENT CD4029BMS IC'S. THESE NEGATIVE GOING GLITCHES DO NOT AFFECT PROPER CD4029BMS OPERATION. HOWEVER, IF THE CARRY OUT SIGNALS ARE USED TO TRIGGER OTHER EDGE-SENSITIVE LOGIC DEVICES, SUCH AS FF'S OR COUNTERS, THE CARRY OUT SIGNALS SHOULD BE GATED WITH THE CLOCK SIGNAL USING A 2-INPUT OR GATE SUCH AS CD4071BMS.

FIGURE 13. CASCADING COUNTER PACKAGES

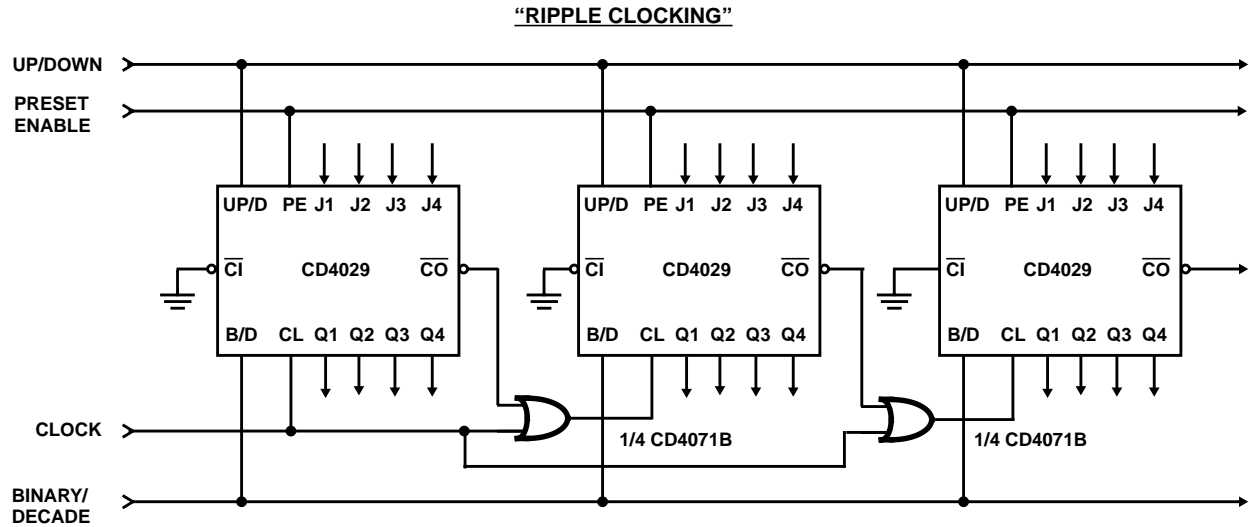
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CD4029BMS

Timing Diagrams (Continued)

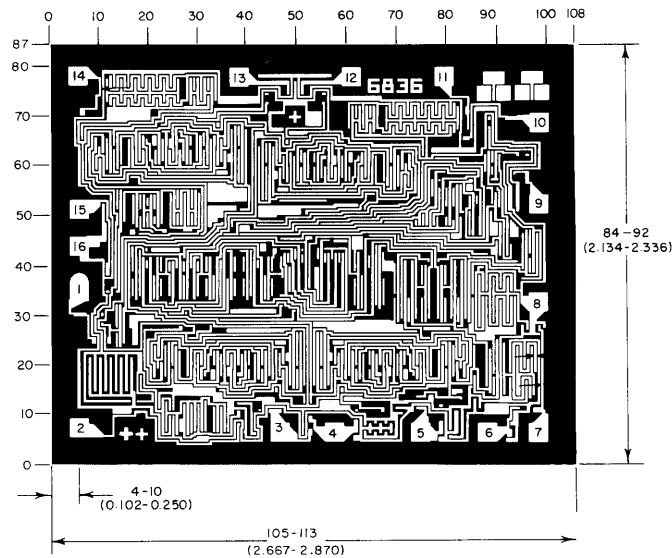


RIPPLE CLOCKING MODE:

THE UP/DOWN CONTROL CAN BE CHANGED AT ANY COUNT. THE ONLY RESTRICTION ON CHANGING THE UP/DOWN CONTROL IS THAT THE CLOCK INPUT TO THE FIRST COUNTING STAGE MUST BE HIGH. FOR CASCADING COUNTERS OPERATING IN A FIXED UP-COUNT OR DOWN-COUNT MODE, THE OR GATES ARE NOT REQUIRED BETWEEN STAGES, AND \overline{CO} IS CONNECTED DIRECTLY TO THE CL INPUT OF THE NEXT STAGE WITH \overline{CI} GROUNDED.

FIGURE 13. CASCADING COUNTER PACKAGES (Continued)

Chip Dimensions and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: $11\text{k}\text{\AA} - 14\text{k}\text{\AA}$, AL.

PASSIVATION: $10.4\text{k}\text{\AA} - 15.6\text{k}\text{\AA}$, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches