

# DATA SHEET

**74F151A**

8-input multiplexer

Product specification  
Supercedes data of 1989 Mar 03  
IC15 Data Handbook

1995 Jul 17

8-input multiplexer

74F151A

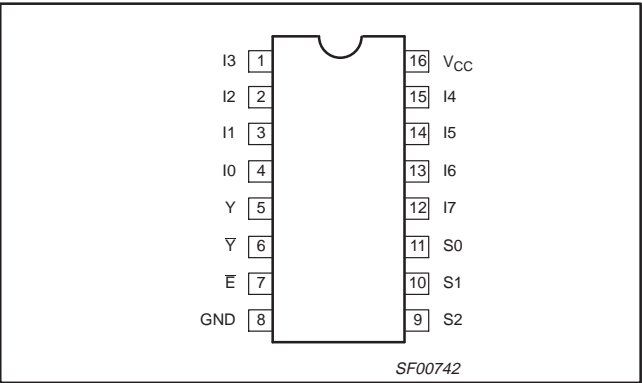
FEATURES

- High speed 8-to-1 multiplexing
- On chip decoding
- Multifunction capability
- Complementary outputs

DESCRIPTION

The 74F151A is a logic implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select (S0, S1, S2) inputs. True (Y) and complementary ( $\bar{Y}$ ) outputs are both provided. The Enable input ( $\bar{E}$ ) is active Low. When  $\bar{E}$  is High, the  $\bar{Y}$  output is High and the Y output is Low, regardless of all other inputs. In one package the 74F151A provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and the negation with correct manipulation.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F151A	4.5ns	17mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$	
16-pin plastic DIP	N74F151AN	SOT38-4
16-pin plastic SO	N74F151AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0–I7	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
S0–S2	Select inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\bar{E}$	Enable input (active High)	1.0/1.0	20 $\mu$ A/0.6mA
Y, $\bar{Y}$	Data outputs	150/33	3mA/20mA

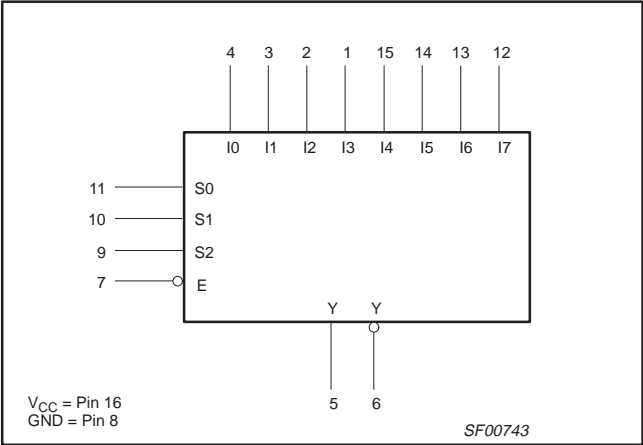
NOTE:

One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

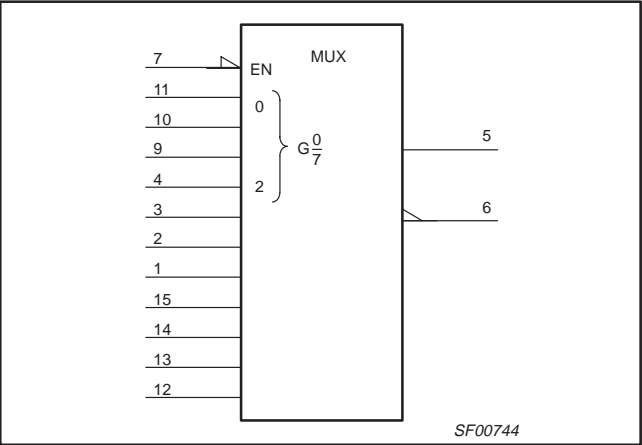
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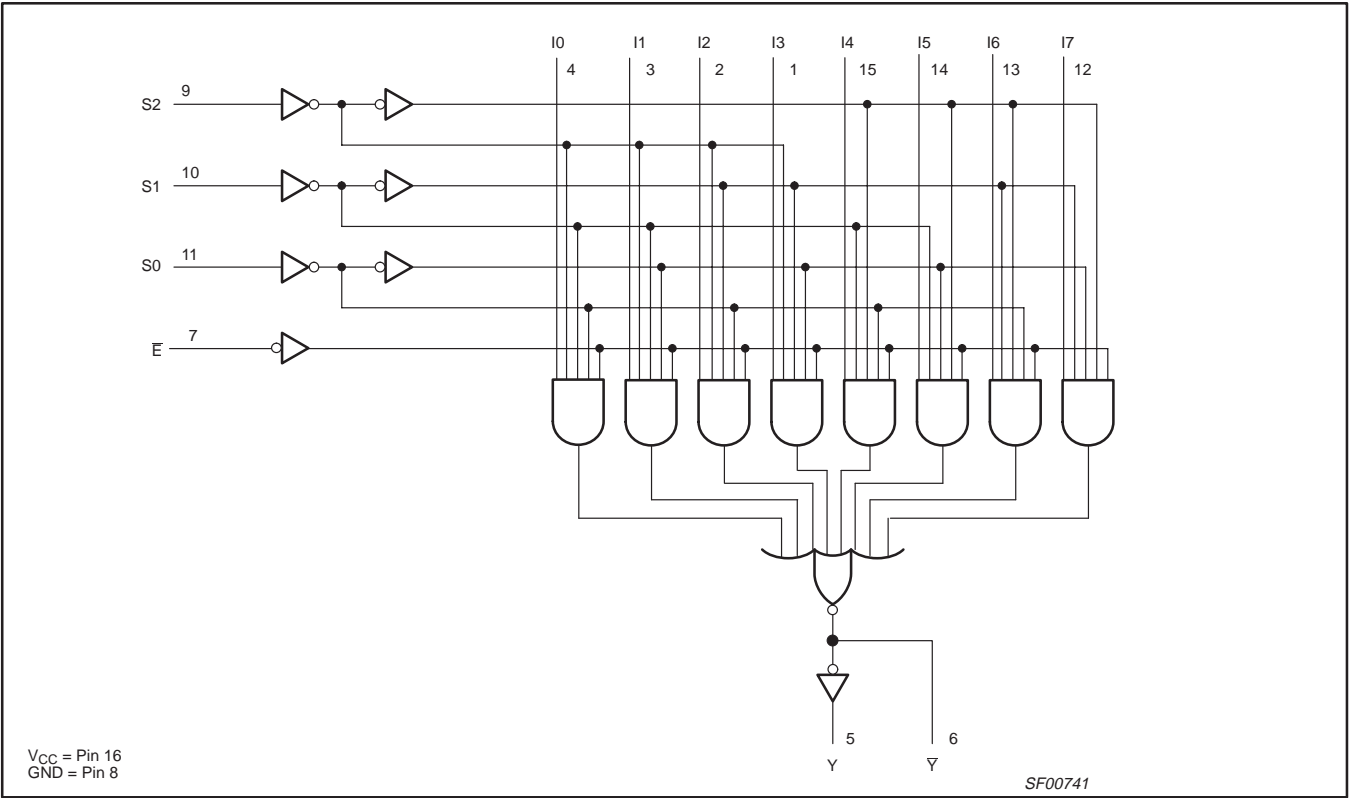
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



## 8-input multiplexer

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## FUNCTION TABLE

INPUTS				OUTPUTS	
S2	S1	S0	$\bar{E}$	Y	$\bar{Y}$
X	X	X	H	L	H
L	L	L	L	I0	$\bar{I}0$
L	L	H	L	I1	$\bar{I}1$
L	H	L	L	I2	$\bar{I}2$
L	H	H	L	I3	$\bar{I}3$
H	L	L	L	I4	$\bar{I}4$
H	L	H	L	I5	$\bar{I}5$
H	H	L	L	I6	$\bar{I}6$
H	H	H	L	I7	$\bar{I}7$

## NOTES:

H = High voltage level

L = Low voltage level

X = Don't care

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	−0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	−0.5 to +7.0	V
I <sub>IN</sub>	Input current	−30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	−0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature	−65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			−18	mA
I <sub>OH</sub>	High-level output current			−1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	0		+70	°C

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER\	TEST CONDITIONS <sup>NO TAG</sup>		LIMITS			UNIT
				MIN	TYP NO TAG	MAX	
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>	2.5			V
			±5%V <sub>CC</sub>	2.7	3.4		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.30	0.50	V
			±5%V <sub>CC</sub>		0.30	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			−0.73	−1.2	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				100	μA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				20	μA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V				−0.6	mA
I <sub>OS</sub>	Short-circuit output current <sup>NO TAG</sup>		V <sub>CC</sub> = MAX	−60		−150	mA
I <sub>CC</sub>	Supply current (total)	I <sub>CC</sub> H	V <sub>CC</sub> = MAX		18	25	mA
		I <sub>CC</sub> L			17	25	mA

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## AC ELECTRICAL CHARACTERISTICS

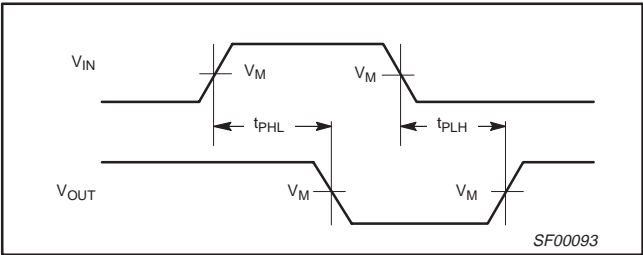
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5.0V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5.0V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay In to Y	Waveform NO TAG	2.5 2.5	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay In to $\bar{Y}$	Waveform NO TAG	2.0 1.0	4.0 2.0	7.0 4.5	2.0 1.0	7.5 5.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S <sub>n</sub> to Y	Waveform 1, 2	4.5 4.0	6.5 6.0	10.0 8.5	4.0 3.5	11.0 9.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S <sub>n</sub> to $\bar{Y}$	Waveform NO TAG, NO TAG	3.5 2.5	5.5 4.5	8.5 7.0	3.0 2.0	9.5 7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $\bar{E}$ to Y	Waveform 1	4.0 3.0	6.5 5.0	9.0 7.0	3.5 3.0	9.5 7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $\bar{E}$ to $\bar{Y}$	Waveform NO TAG	2.5 2.0	4.5 3.5	6.5 5.5	2.5 1.5	7.0 6.0	ns

## AC WAVEFORMS

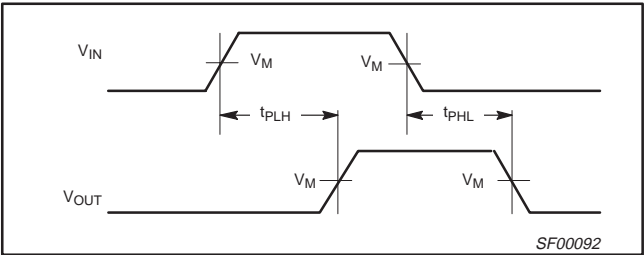
For all waveforms, V<sub>M</sub> = 1.5V

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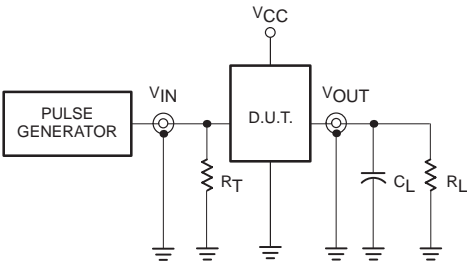


Waveform 1. For Inverting Outputs

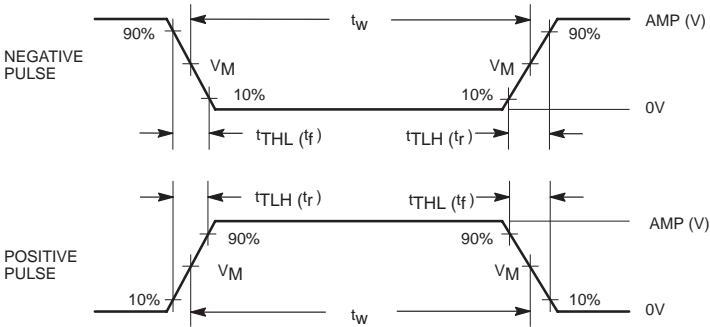


Waveform 2. For Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

- $R_L$  = Load resistor;  
see AC ELECTRICAL CHARACTERISTICS for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance;  
see AC ELECTRICAL CHARACTERISTICS for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of  
pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

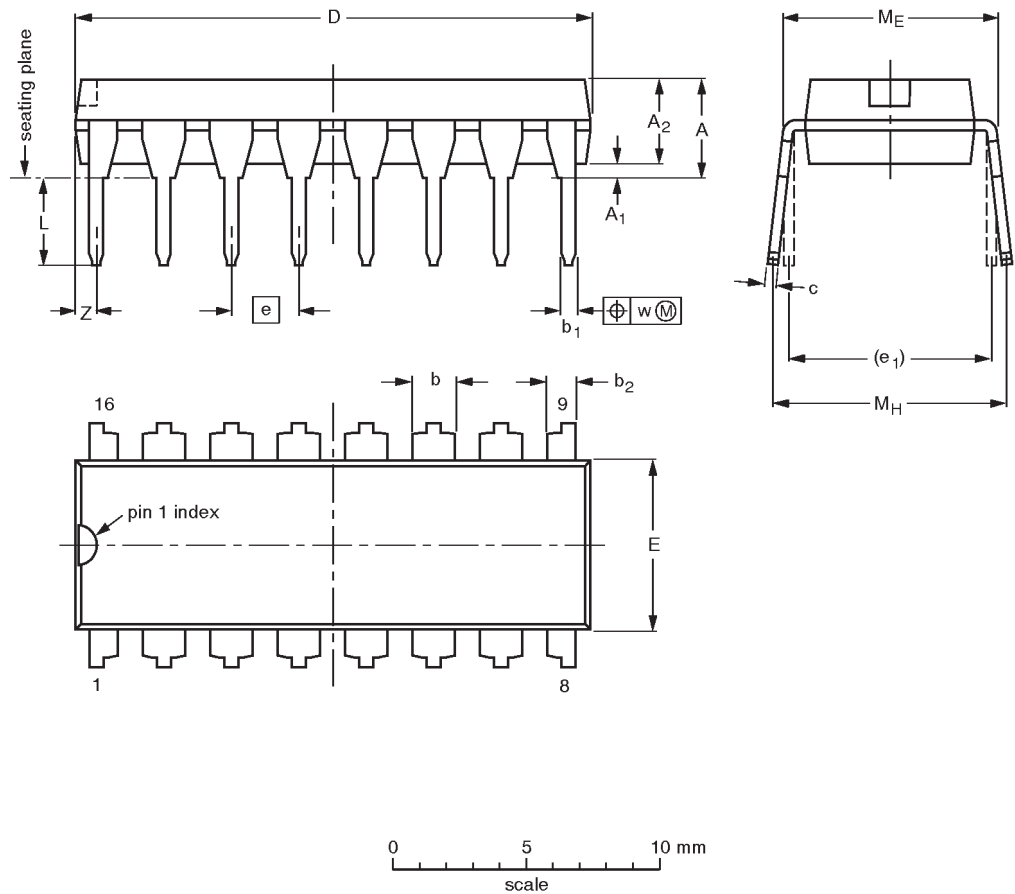
SF00006

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4




DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

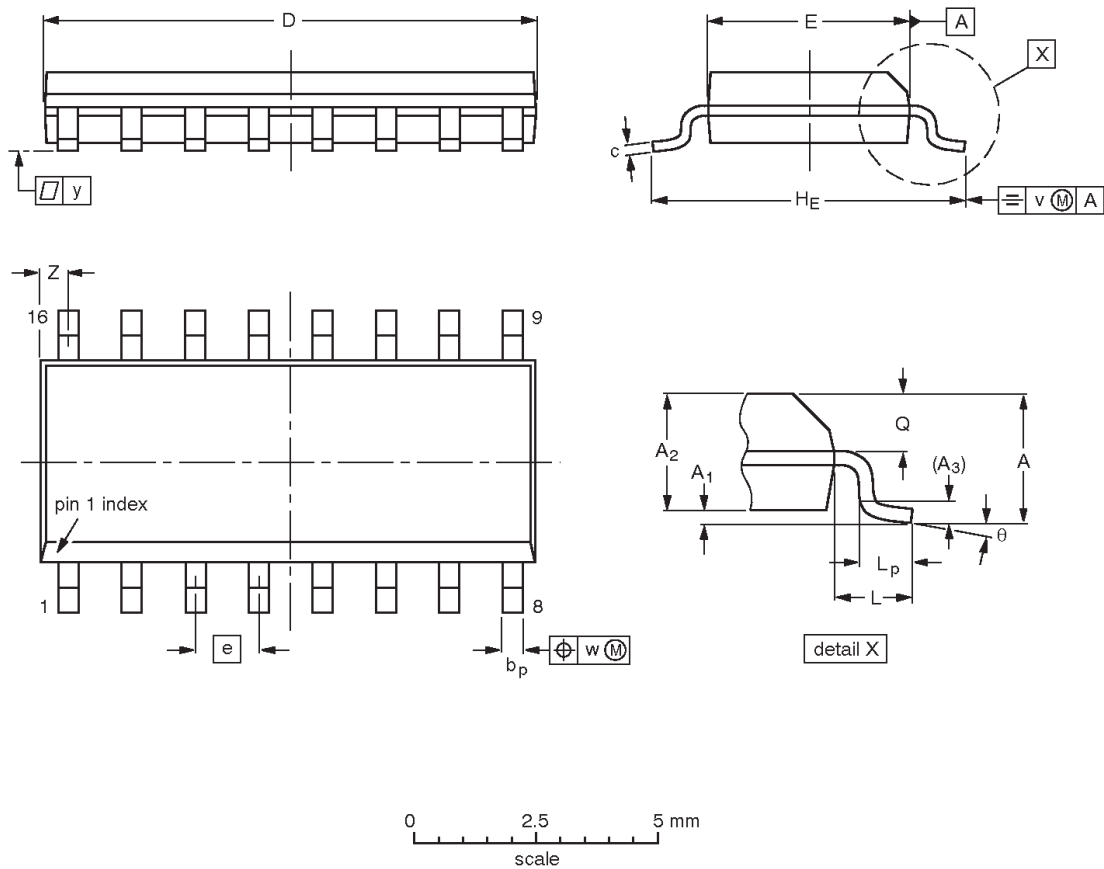
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22



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NOTES

## 8-input multiplexer

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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print code

Date of release: 10-98

Document order number:

9397-750-05079

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