NEC

MOS INTEGRATED CIRCUIT

μPD178004A, 178006A, 178016A, 178018A

8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD178004A, 178006A, 178016A and 178018A are 8-bit single-chip CMOS microcontrollers that incorporate hardware for digital tuning systems.

The CPU uses the 78K/0 architecture, which makes it easy to implement high-speed access to internal memory and control of peripheral hardware. Also, the instructions used are the high-speed 78K/0 instructions, suitable for system control.

The rich assortment of peripheral hardware includes an input/output port, 8-bit timer, A/D converter, serial interface, power-ON clear circuits, as well as a pre-scaler for digital tuning, a PLL frequency synthesizer and a frequency counter.

The μPD178P018A, one-time PROM or EPROM versions which can be operated in the same supply voltage range as for the mask ROM versions, and various development tools, are also available.

For more information on functions, refer to the following User's Manuals. Be sure to read them when designing.

μPD178018A Subseries User's Manual: to be prepared
78K/0 Series User's Manual Instruction: U12326E

FEATURES

- Internal high-capacity ROM and RAM

Items / Product Name	Program Memory	Data Memory		
	ROM	Internal High-Speed RAM	Buffer RAM	Internal Expanded RAM
μPD178004A	32 Kbytes	1 024 bytes	32 bytes	Not provided
μPD178006A	48 Kbytes			
μPD178016A				2 048 bytes
μPD178018A	60 Kbytes			

- Instruction Cycle: 0.44 μs (4.5-MHz crystal oscillator used)
- Large array of on-chip peripheral hardware
  General-purpose input/output port, A/D converter, serial interface, timer, frequency counter, power-ON clear circuits.
- On-chip hardware for a PLL frequency synthesizer.
  Dual modulus pre-scaler, programmable divider, phase comparator, charge pump.
- Vector interrupt sources: 17
- Supply Voltage: V_{DD} = 4.5 to 5.5 V (during PLL operation)
  V_{DD} = 3.5 to 5.5 V (during CPU operation, when the system clock is f_X/2 or lower)
  V_{DD} = 4.5 to 5.5 V (during CPU operation, when the system clock is f_X)

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APPLICATIONS

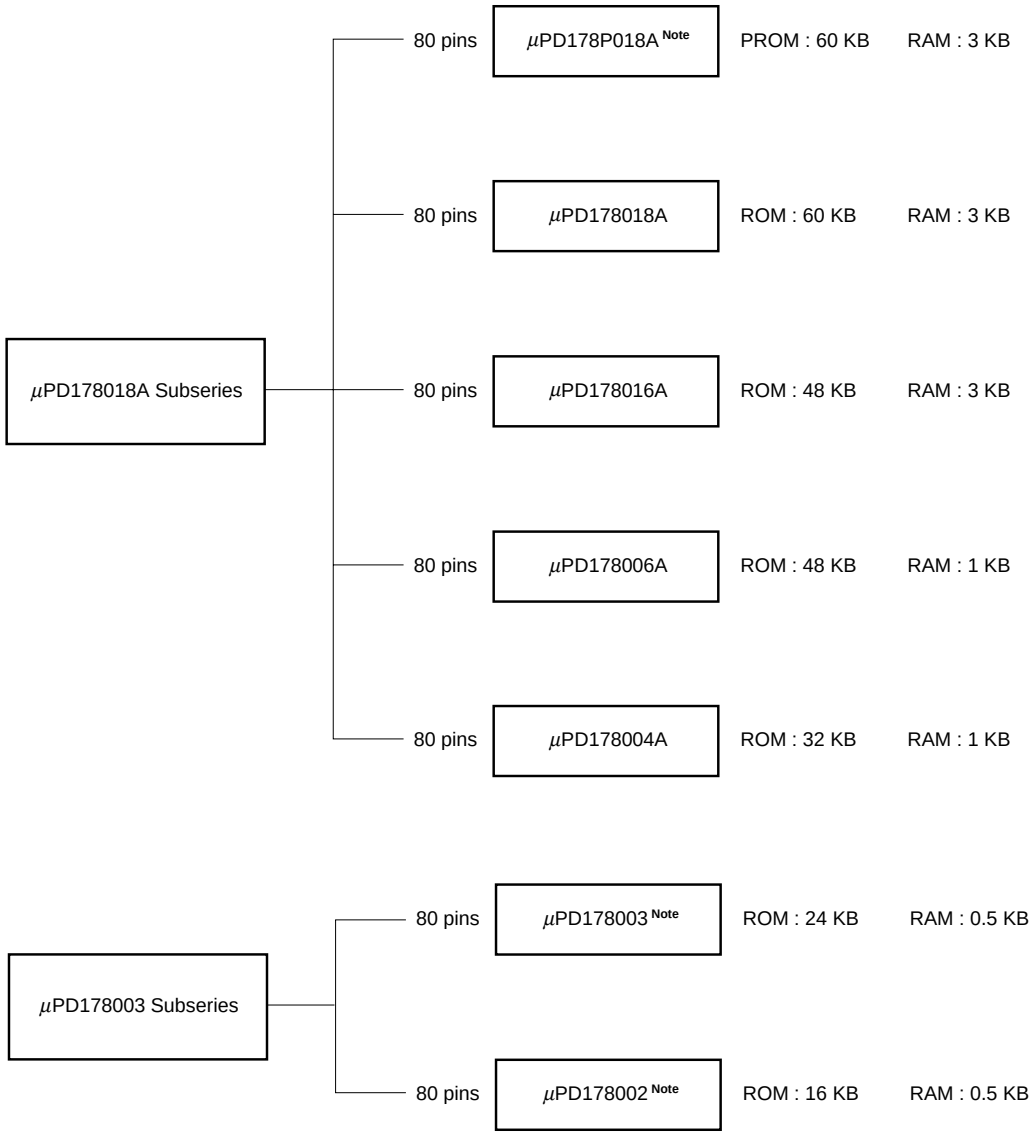
Car stereo, home stereo systems.

ORDERING INFORMATION

Part Number	Package
μPD178004AGC-×××-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)
μPD178006AGC-×××-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)
μPD178016AGC-×××-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)
μPD178018AGC-×××-3B9	80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)

Remark ××× denotes the ROM code number. Also, the ROM code number becomes E×× when the I^2C bus is used.

μPD178018A SUBSERIES AND μPD178003 SUBSERIES EXPANSION



Note Under development

OUTLINE OF FUNCTION

(1/2)

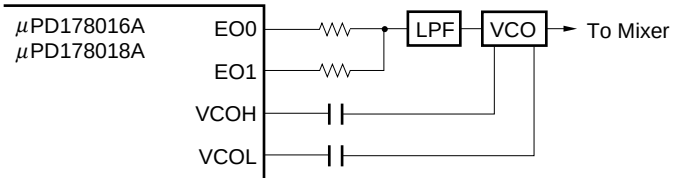
Item \ Product name		μPD178004A	μPD178006A	μPD178016A	μPD178018A
Internal memory	ROM (ROM configuration)	32 Kbytes (mask ROM)	48 Kbytes (mask ROM)		60 Kbytes (mask ROM)
	High-speed RAM	1 024 bytes			
	Buffer RAM	32 bytes			
	Expansion RAM	Not provided		2 048 bytes	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Instruction cycle		With variable instruction execution time function 0.44 μs/0.88 μs/1.78 μs/3.56 μs/7.11 μs/14.22 μs (with 4.5-MHz crystal resonator)			
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjustment, etc.			
I/O port		Total : 62 pins CMOS input : 1 pin CMOS I/O : 54 pins N-ch open-drain I/O : 4 pins N-ch open-drain output : 3 pins			
A/D converter		8-bit resolution × 6 channels			
Serial interface		• 3-wire/SBI/2-wire/I²C bus Note mode selectable : 1 channel • 3-wire serial I/O mode (with automatic transfer/receive function of up to 32 byte) : 1 channel			
Timer		• Basic timer (timer carry FF (10 Hz)) : 1 channel • 8-bit timer/event counter : 2 channels • 8-bit timer (D/A converter: PWM output) : 1 channel • Watchdog timer : 1 channel			
Buzzer (BEEP) output		1.5 kHz, 3 kHz, 6 kHz			
Vectored interrupt Source	Maskable	Internal: 8, external: 7			
	Non-maskable	Internal: 1			
	Software	Internal: 1			
Test input		Internal: 1			

Note When using the I²C bus mode (including when this mode is implemented by program without using the peripheral hardware), consult your local NEC sales representative when you place an order for mask.

(2/2)

Item \ Product name		μPD178004A	μPD178006A	μPD178016A	μPD178018A
PLL frequency synthesizer	Division mode	Two types • Direct division mode (VCOL pin) • Pulse swallow mode (VCOH and VCOL pins)			
	Reference frequency	7 types selectable by program (1, 3, 5, 9, 10, 25, 50 kHz)			
	Charge pump	Error out output: 2 (EO0 and EO1 pins Note 1)			
	Phase comparator	Unlock detectable by program			
Frequency counter		• Frequency measurement • AMIFC pin: for 450-kHz count • FMIFC pin: for 450-kHz/10.7-MHz count			
D/A converter (PWM output)		8-/9-bit resolution × 3 channels (shared by 8-bit timer)			
Standby function		• HALT mode • STOP mode			
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Reset by power-ON clear circuit (3-value detection) • Detection of less than 4.5 V Note 2 (CPU clock: f_X) • Detection of less than 3.5 V Note 2 (CPU clock: $f_X/2$ or less and on power application) • Detection of less than 2.5 V Note 2 (in STOP mode)			
Power supply voltage		• V_{DD} = 4.5 to 5.5 V (with PLL operating) • V_{DD} = 3.5 to 5.5 V (with CPU operating, CPU clock: $f_X/2$ or less) • V_{DD} = 4.5 to 5.5 V (with CPU operating, CPU clock: f_X)			
Package		• 80-pin plastic QFP (14 × 14 mm, 0.65-mm pitch)			

Notes 1. The EO1 pin can be set to high impedance for the μPD178016A and 178018A.
The following shows an application example.



LPF : Low path filter
VCO : Voltage controlled oscillator

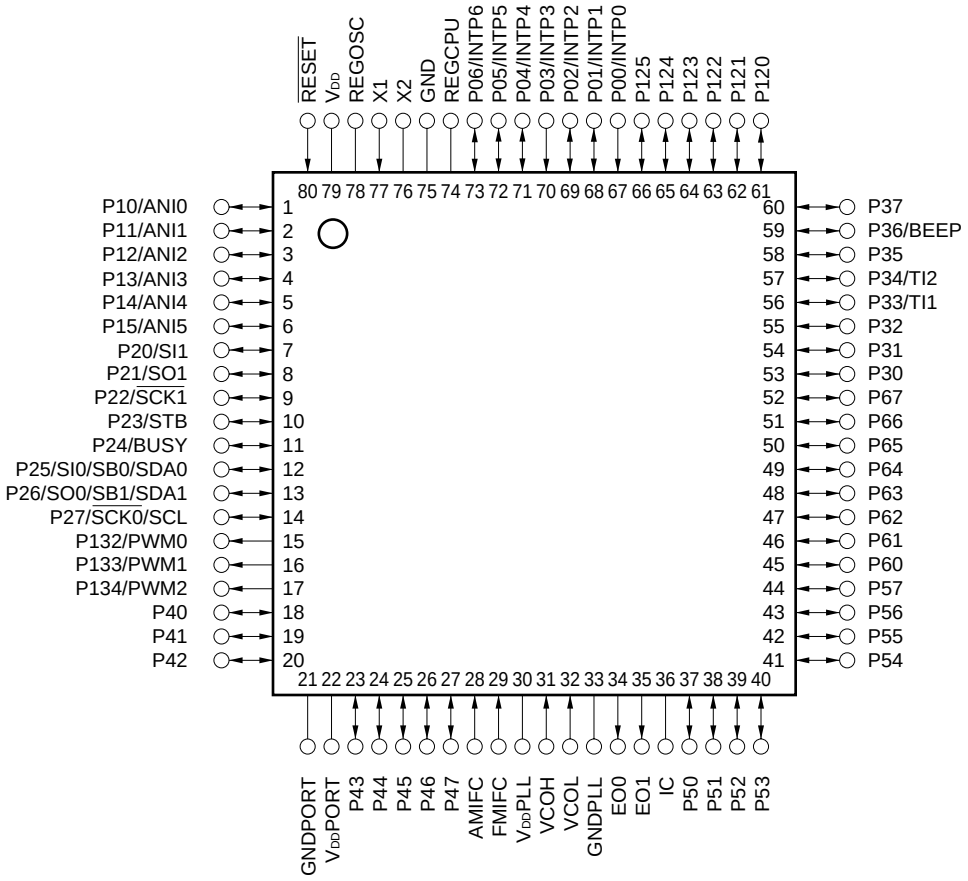
- To lock to a target frequency at high speed
  Setting the EO0 and EO1 pins to error out output improves the output current potential and LPF voltage control potential.
- Normal state
  Setting only the EO0 pin to error out output maintains the LPF stable.

2. These voltage values are maximum values. Reset is actually executed at a voltage lower than these values.

TABLE OF CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **80-PIN PLASTIC QFP (14 × 14 mm, 0.65 mm pitch)**
  μPD178004AGC-×××-3B9, 178006AGC-×××-3B9
  μPD178016AGC-×××-3B9, 178018AGC-×××-3B9



Cautions 1. Connect the Internally Connected (IC) pin to GND directly.

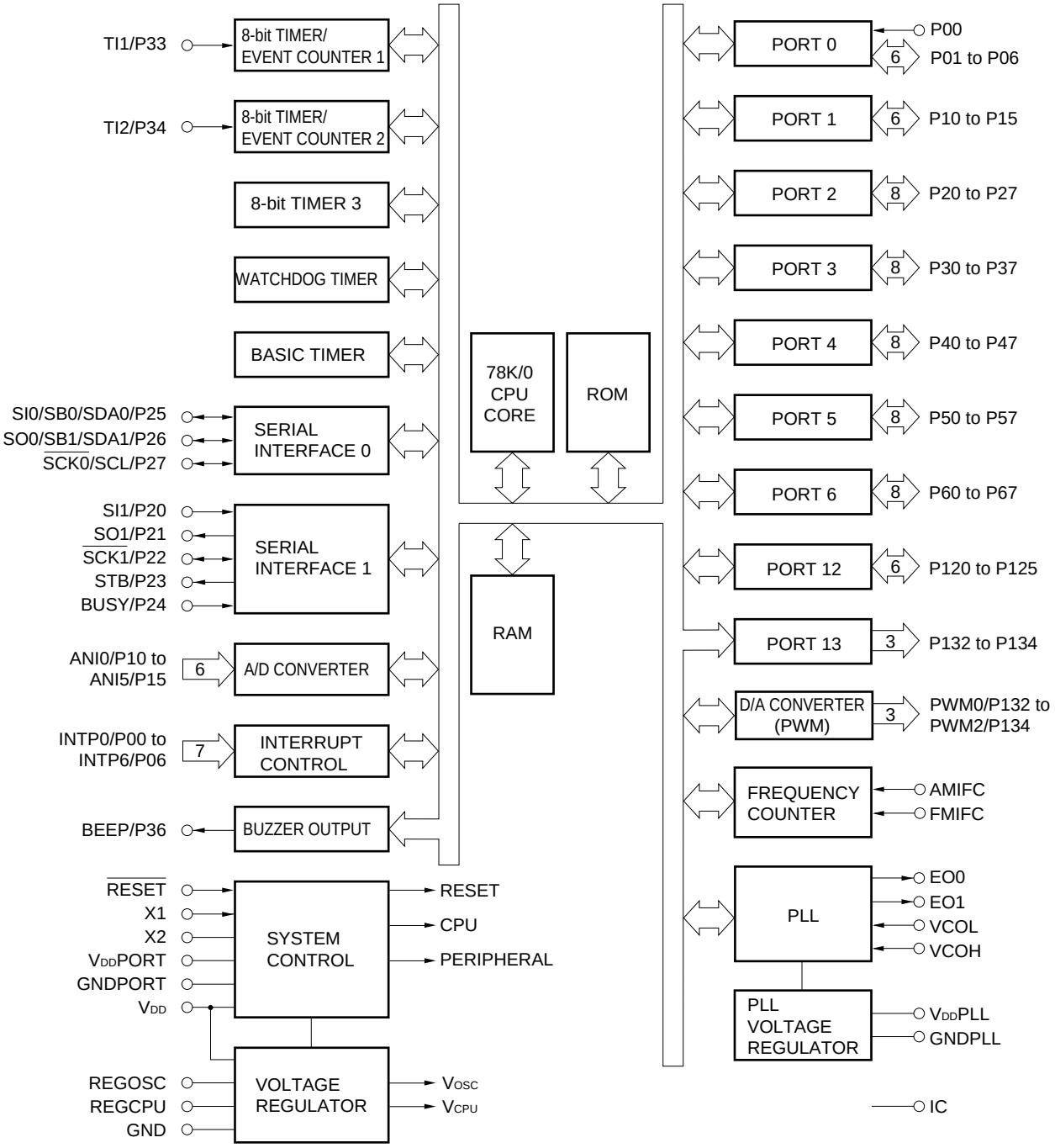
2. Connect V_{DD}PORT and V_{DD}PLL pins to V_{DD}.

3. Connect the GNDPORT and GNDPLL pins to GND.

4. Connect each of the REGOSC and REGCPU pins to GND via a 0.1-μF capacitor.

AMIFC : AM Intermediate Frequency Counter Input
AN10 to AN15 : A/D Converter Input
BEEP : Buzzer Output
BUSY : Busy Output
EO0, EO1 : Error Out Output
FMIFC : FM Intermediate Frequency Counter Input
GND : Ground
GNDPLL : PLL Ground
GNDPORT : Port Ground
IC : Internally Connected
INTP0 to INTP6 : Interrupt Inputs
P00 to P06 : Port 0
P10 to P15 : Port 1
P20 to P27 : Port 2
P30 to P37 : Port 3
P40 to P47 : Port 4
P50 to P57 : Port 5
P60 to P67 : Port 6
P120 to P125 : Port 12
P132 to P134 : Port 13
PWM0 to PWM2 : PWM Output
REGCPU : Regulator for CPU Power Supply
REGOSC : Regulator for Oscillator Circuit
$\overline{\text{RESET}}$: Reset Input
SB0, SB1 : Serial Data Bus Input/Output
$\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$: Serial Clock Input/Output
SCL : Serial Clock Input/Output
SDA0, SDA1 : Serial Data Input/Output
SI0, SI1 : Serial Data Input
SO0, SO1 : Serial Data Output
STB : Strobe Output
TI1, TI2 : Timer Clock Input
VCOL, VCOH : Local Oscillator Input
V_{DD} : Power Supply
V_{DD}PLL : PLL Power Supply
V_{DD}PORT : Port Power Supply
X1, X2 : Crystal Oscillator Connection

2. BLOCK DIAGRAM



Remark The internal ROM and RAM capacities depend on the version.

3. PIN FUNCTION LIST

3.1 PORT PINS

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0. 7-bit input/output port.	Input only	Input	INTP0
P01 to P06	I/O		Input/output mode can be specified bit-wise.	Input	INTP1 to INTP6
P10 to P15	I/O	Port 1. 6-bit input/output port. Input/output mode can be specified bit-wise.		Input	ANI0 to ANI5
P20	I/O	Port 2. 8-bit input/output port. Input/output mode can be specified bit-wise.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB
P24					BUSY
P25					SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{\text{SCK0}}$/SCL
P30 to P32	I/O	Port 3. 8-bit input/output port. Input/output mode can be specified bit-wise.		Input	—
P33					TI1
P34					TI2
P35					—
P36					BEEP
P37					—
P40 to P47	I/O	Port 4. 8-bit input/output port. Input/output mode can be specified in 8-bit units. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	—
P50 to P57	I/O	Port 5. 8-bit input/output port. Input/output mode can be specified bit-wise.		Input	—
P60 to P63	I/O	Port 6. 8-bit input/output port. Input/output mode can be specified bit-wise.	Middle voltage N-ch open drain input/output port. LEDs can be driven directly.	Input	—
P64 to P67					
P120 to P125	I/O	Port 12. 6-bit input/output port. Input/output mode can be specified bit-wise.		Input	—
P132 to P134	Output	Port 13. 3-bit output port. N-ch open-drain output port.		—	PWM0 to PWM2

3.2 PINS OTHER THAN PORT PINS

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP6	Input	External maskable interrupt inputs with specifiable valid edges (rising edge, falling edge, both rising and falling edges).	Input	P00 to P06
SI0	Input	Serial interface serial data input	Input	P25/SB0/SDA0
SI1				P20
SO0	Output	Serial interface serial data output	Input	P26/SB1/SDA1
SO1				P21
SB0	I/O	Serial interface serial data input/output	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{SCK0}$	I/O	Serial interface serial clock input/output	Input	P27/SCL
$\overline{SCK1}$				P22
SCL				P27/$\overline{SCK0}$
STB	Output	Serial interface automatic transmit/receive strobe output	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input	Input	P24
TI1	Input	External count clock input to 8-bit timer (TM1)	Input	P33
TI2		External count clock input to 8-bit timer (TM2)		P34
BEEP	Output	Buzzer output	Input	P36
ANI0 to ANI5	Input	A/D converter analog input	Input	P10 to P15
PWM0 to PWM2	Output	PWM output	—	P132 to P134
EO0, EO1	Output	Error out output from charge pump of the PLL frequency synthesizer	—	—
VCOL	Input	Inputs PLL local band frequency (In HF, MF mode)	—	—
VCOH	Input	Inputs PLL local band frequency (In VHF mode)	—	—
AMIFC	Input	Inputs AM intermediate frequency counter	—	—
FMIFC	Input	Inputs FM intermediate frequency counter	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	System clock oscillation resonator connection	—	—
X2	—		—	—
REGOSC	—	Oscillation regulator. Connected to GND via a 0.1-μF capacitor.	—	—
REGCPU	—	CPU power supply regulator. Connected to GND via a 0.1-μF capacitor.	—	—
V_{DD}	—	Positive power supply	—	—
GND	—	Ground	—	—
V_{DD}PORT	—	Positive power supply for port block	—	—
GNDPORT	—	Ground for port block	—	—
V_{DD}PLL **Note**	—	Positive power supply for PLL	—	—
GNDPLL **Note**	—	Ground for PLL	—	—
IC	—	Internally connected. Connected to GND or GNDPORT.	—	—

Note Connect a capacitor of approximately 1 000 pF between the V_{DD}PLL pin and GNDPLL pin.

3.3 INPUT/OUTPUT CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

Table 3-1 shows the input/output circuit types of pins and the recommended conditions for unused pins.

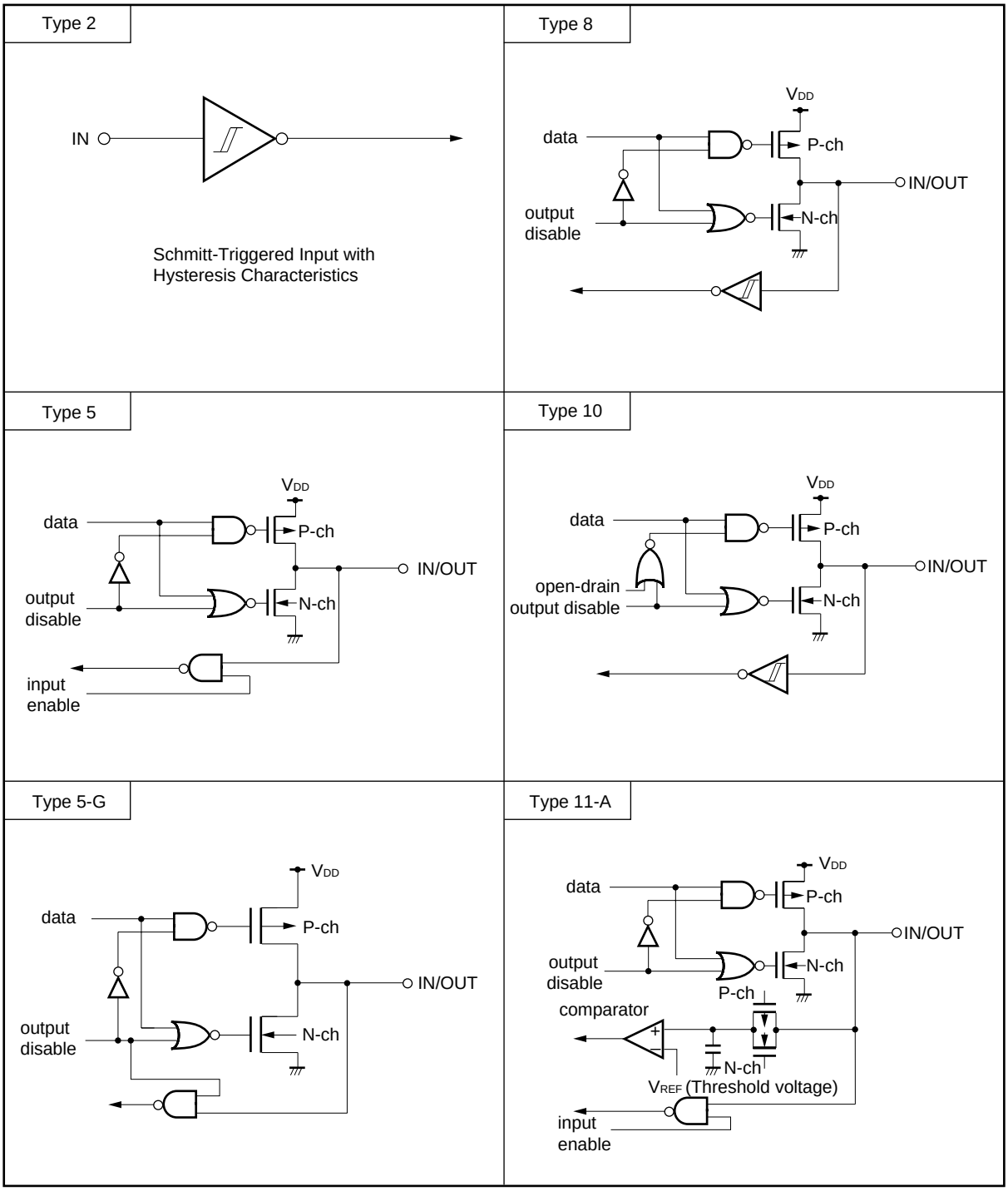
Refer to Figure 3-1 for the configuration of the input/output circuit of each type.

Table 3-1. I/O Circuit Type of Each Circuit

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00/INTP0	2	Input	Connected to GND or GNDPORT
P01/INTP1 to P06/INTP6	8	I/O	Set in general-purpose input port mode by software and individually connected to V_{DD}, V_{DD}PORT, GND, or GNDPORT via resistor.
P10/ANI0 to P15/ANI5	11-A		
P20/SI1	8		
P21/SO1	5		
P22/$\overline{\text{SCK1}}$	8		
P23/STB	5		
P24/BUSY	8		
P25/SI0/SB0/SDA0 P26/SO0/SB1/SDA1 P27/$\overline{\text{SCK0}}$/SCL	10		
P30 to P32	5		
P33/TI1, P34/TI2	8		
P35 P36/BEEP P37	5		
P40 to P47	5-G		
P50 to P57	5		
P60 to P63	13-D		
P64 to P67	5		
P120 to P125			
P132/PWM0 to P134/PWM2	19	Output	Set to low-level output by software and open
EO0	DTS-EO1		Open
EO1	DTS-EO3 **Note**		
VCOL, VCOH	DTS-AMP	Input	Set to disabled status by software and open
AMIFC, FMIFC			
IC	—	—	Connected to GND or GNDPORT directly

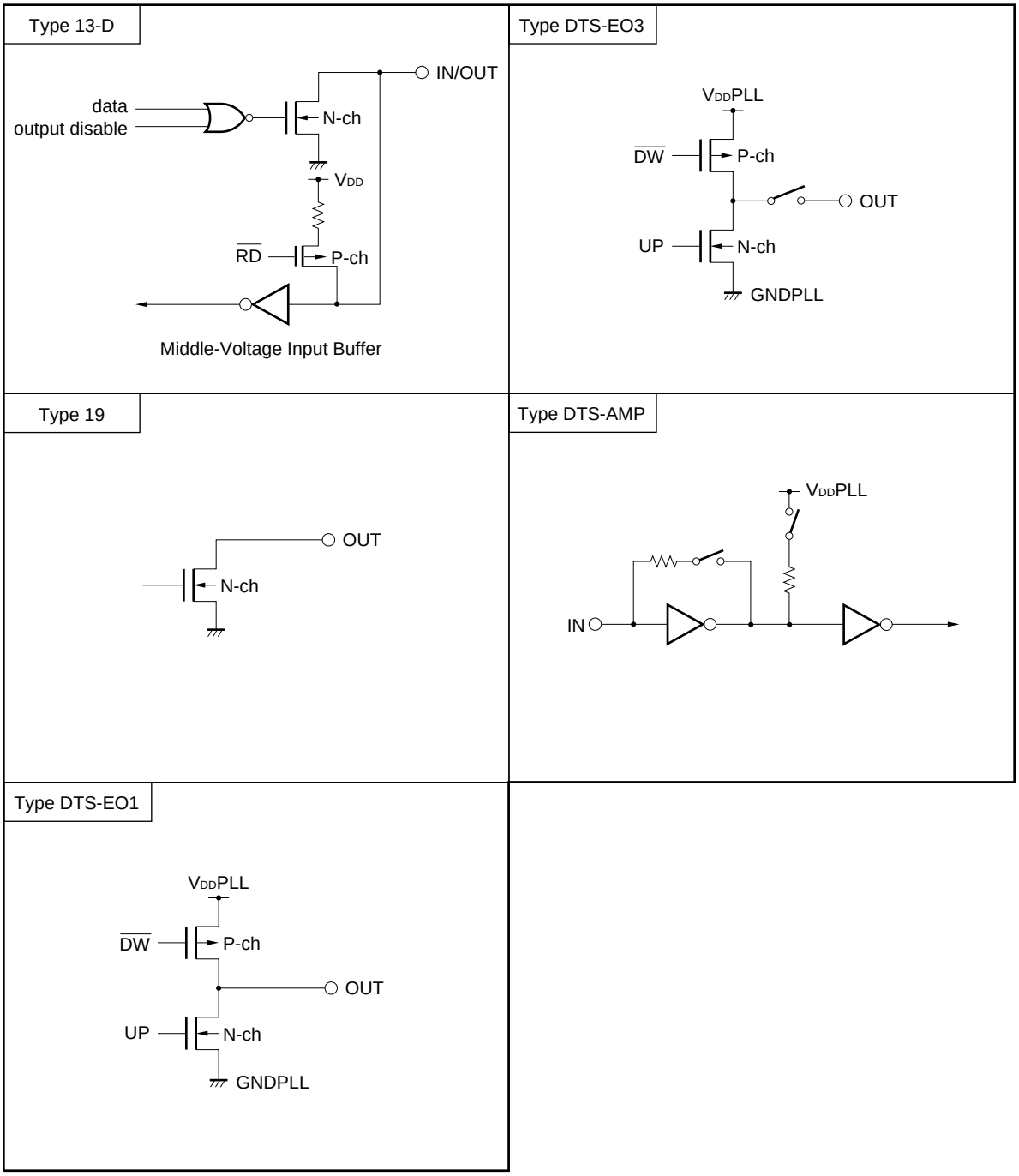
Note For the μPD178004A and 178006A, the I/O circuit type is DTS-EO1.

Figure 3-1. Pin Input/Output Circuit of List (1/2)



Remark All V_{DD} and GND in the above figures are the positive power supply and ground potential of the ports, and should be read as V_{DD}PORT and GNDPORT, respectively.

Figure 3-1. Pin Input/Output Circuit of List (2/2)

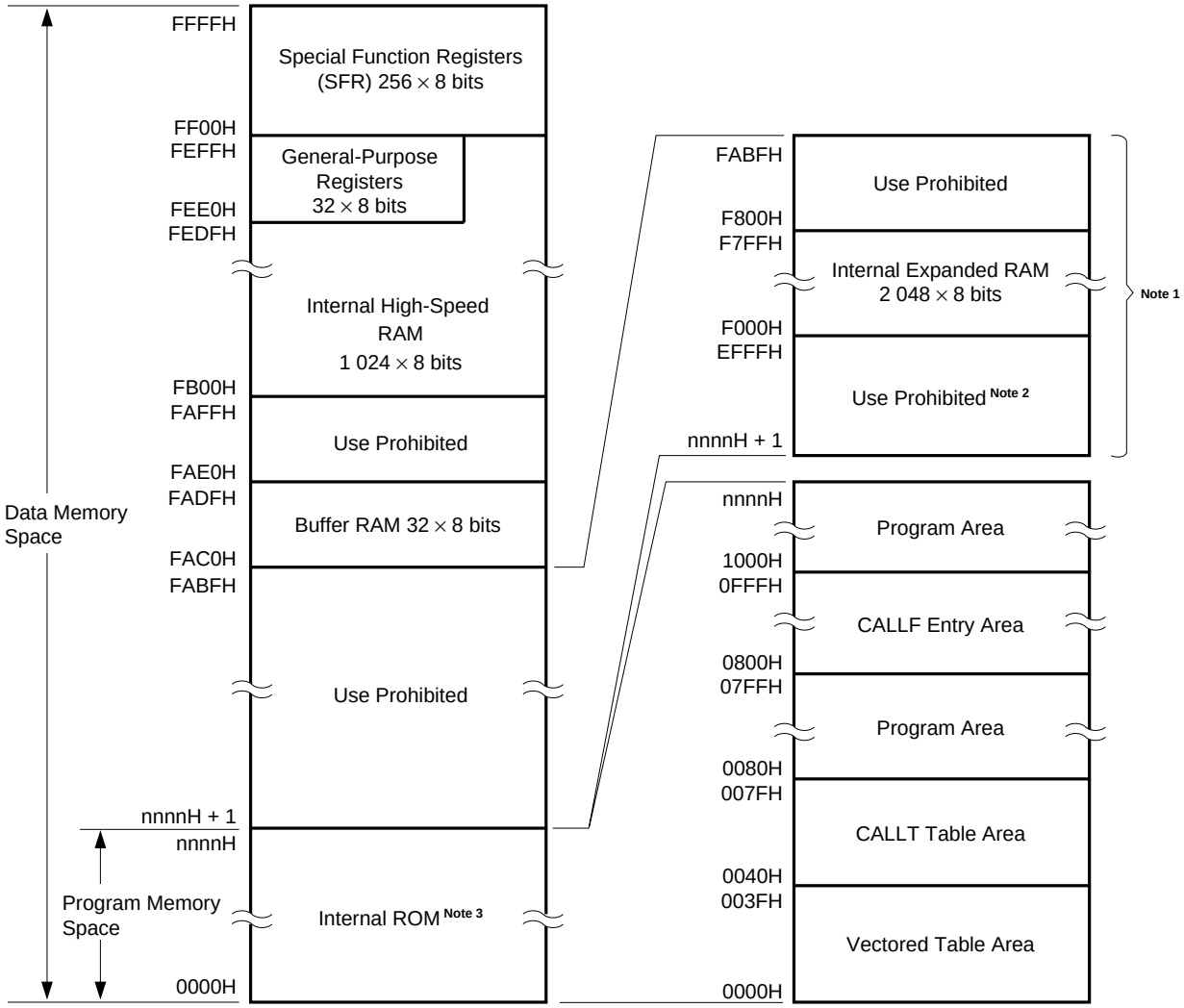


Remark All V_{DD} and GND in the above figures are the positive power supply and ground potential of the ports, and should be read as V_{DD}PORT and GNDPORT, respectively.

4. MEMORY SPACE

Figure 4-1 shows the μPD178004A, 178006A, 178016A, and 178018A memory map.

Figure 4-1. Memory Map



Notes 1. Available only for μPD178016A and 178018A

2. The μPD178018A does not contain this use prohibited area.

3. The internal ROM capacity depends on the version (see the table below).

Corresponding Product Name	Internal ROM Last Address nnnnH
μPD178004A	7FFFH
μPD178006A, 178016A	BFFFH
μPD178018A	EFFFH

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 PORTS

The following 3 types of I/O ports are available.

- CMOS input (P00) : 1
- CMOS input/output (P01 to P06, port 1 to port 5, P64 to P67, port 12) : 54
- N-channel open-drain input/output (P60 to P63) : 4
- N-ch open drain output (Port 13) : 3

Total : 62

Table 5-1. Port Functions

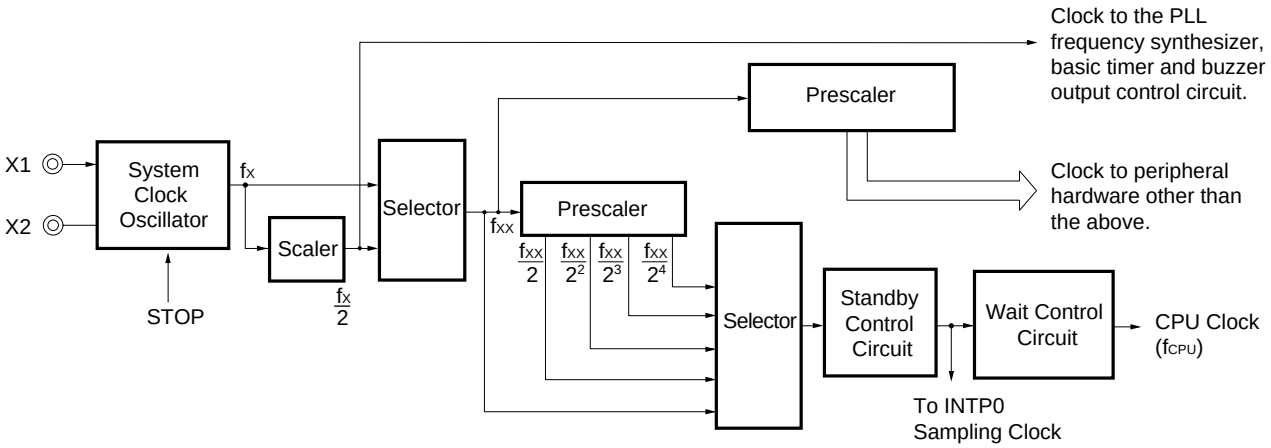
Name	Pin Name	Function
Port 0	P00	Dedicated input port pins
	P01 to P06	Input/output port pins. Input/output specifiable bit-wise.
Port 1	P10 to P15	Input/output port pins. Input/output specifiable bit-wise.
Port 2	P20 to P27	Input/output port pins. Input/output specifiable bit-wise.
Port 3	P30 to P37	Input/output port pins. Input/output specifiable bit-wise.
Port 4	P40 to P47	Input/output port pins. Input/output specifiable in 8-bit units. Test flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port pins. Input/output specifiable bit-wise.
Port 6	P60 to P63	N-channel open-drain input/output port pins. Input/output specifiable bit-wise. LED direct drive capability.
	P64 to P67	Input/output port pins. Input/output specifiable bit-wise.
Port 12	P120 to P125	Input/output port pins. Input/output specifiable bit-wise.
Port 13	P132 to P134	N-ch open drain output port.

5.2 CLOCK GENERATOR

The instruction execution time can be changed as follows.

0.44 μs/0.88 μs/1.78 μs/3.56 μs/7.11 μs/14.22 μs (@ 4.5-MHz crystal oscillator with system clock.)

Figure 5-1. Clock Generator Block Diagram



5.3 TIMER

The μPD178004A, 178006A, 178016A, and 178018A incorporate 5 channels of the timer.

- Basic timer : 1 channel
- 8-bit timer/event counter : 2 channels
- 8-bit timer (D/A converter) Note : 1 channel
- Watchdog timer : 1 channel

Note Used is shared with the 8/9-bit resolution × 3-channel D/A converter (PWM output).

Figure 5-2. Basic Timer Block Diagram

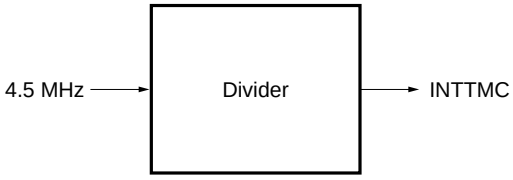


Figure 5-3. 8-Bit Timer/Event Counter Block Diagram

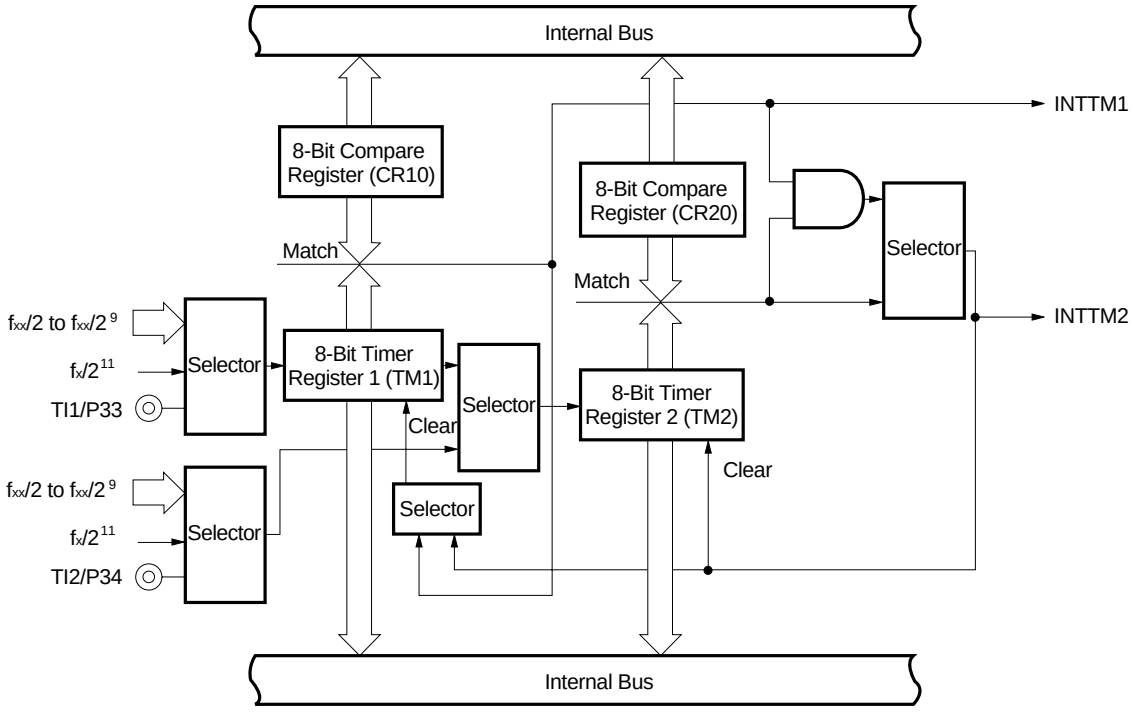
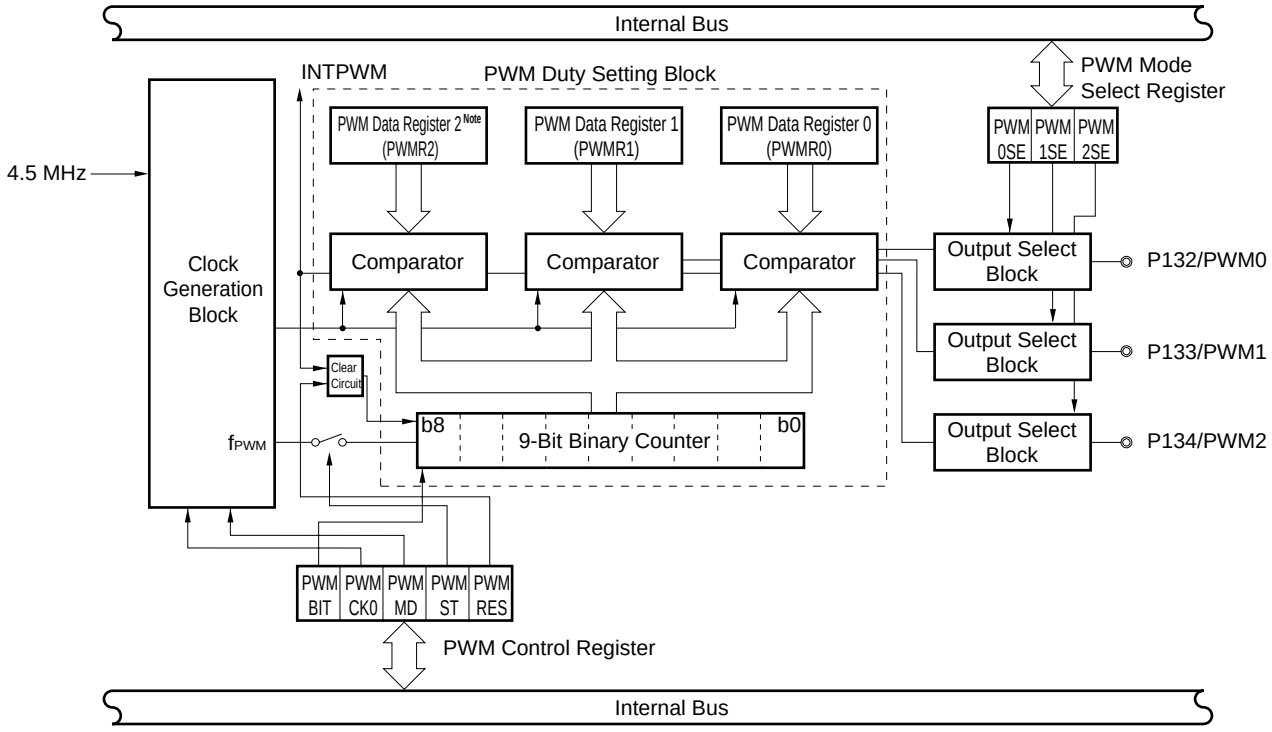
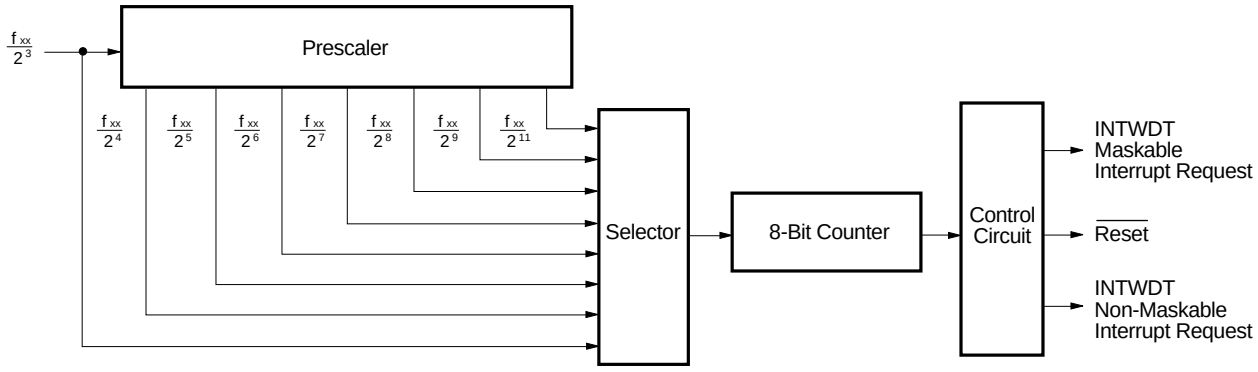


Figure 5-4. 8-Bit Timer (D/A Converter) Block Diagram



Note The PWM data register 2 (PWMR2) is multiplexed with the PWM timer register (PWMTMR).

Figure 5-5. Watchdog Timer Block Diagram

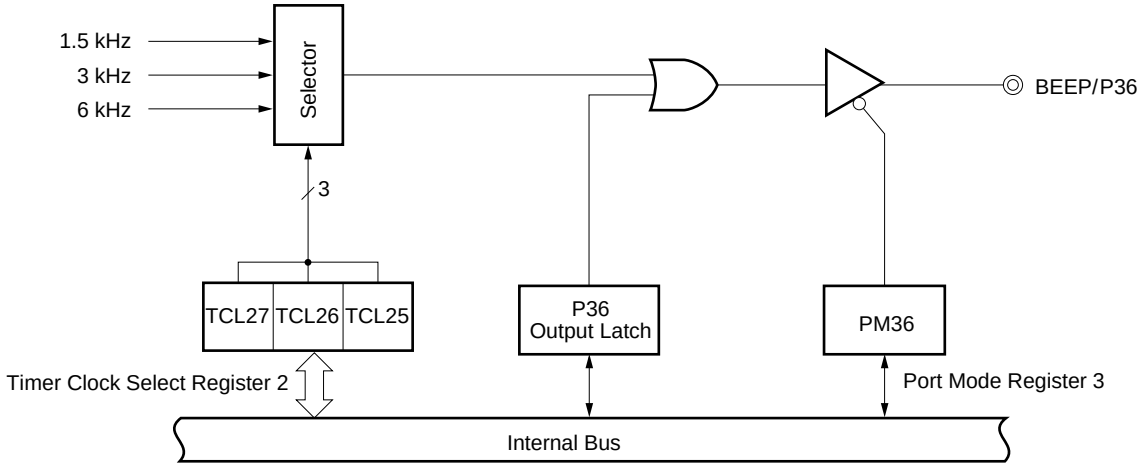


5.4 BUZZER OUTPUT CONTROL CIRCUIT

The clock with the following frequency can be output as a buzzer output.

- 1.5 kHz/3 kHz/6 kHz (@ 4.5-MHz crystal oscillator with system clock)

Figure 5-6. Buzzer Output Control Circuit Block Diagram



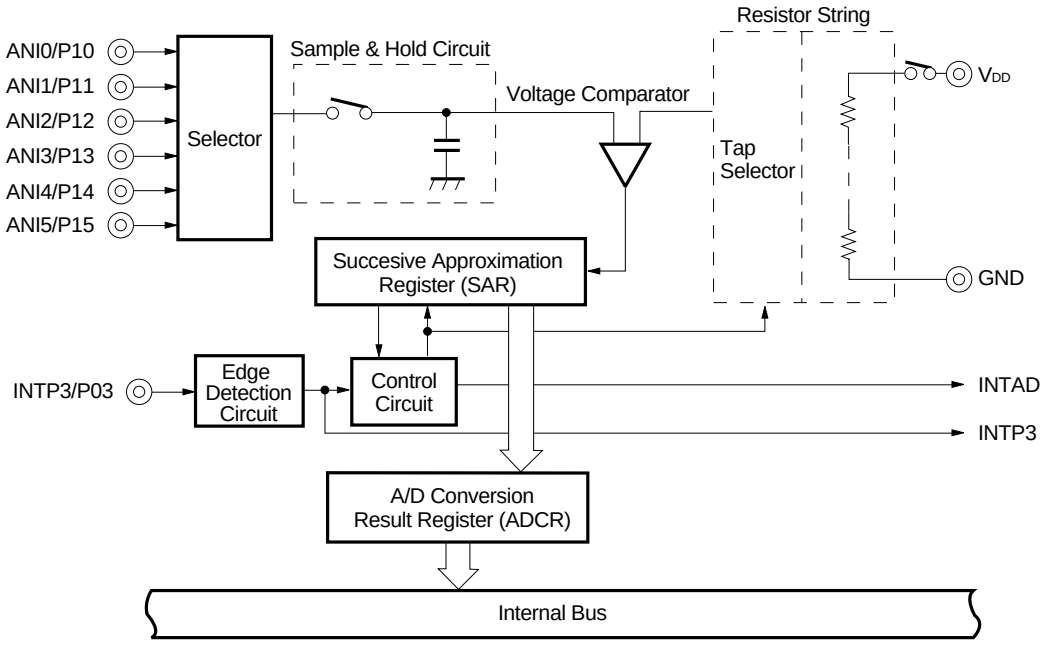
5.5 A/D CONVERTER

An A/D converter of 8-bit resolution × 6 channels is incorporated.

The following two types of the A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Figure 5-7. A/D Converter Block Diagram



5.6 SERIAL INTERFACES

2 channels of the clocked serial interface are incorporated.

- Serial interface channel 0
- Serial interface channel 1

Table 5-2. Types and Functions of Serial Interface

Function	Serial Interface Channel 0	Serial Interface Channel 1
3-wire serial I/O mode	○ (MSB/LSB first switchable)	○ (MSB/LSB first switchable)
3-wire serial I/O mode with automatic transmission/ reception function	—	○ (MSB/LSB first switchable)
SBI (serial bus interface) mode	○ (MSB first)	—
2-wire serial I/O mode	○ (MSB first)	—
I^2C Bus Mode	○ (MSB first)	—

Figure 5-8. Serial Interface Channel 0 Block Diagram

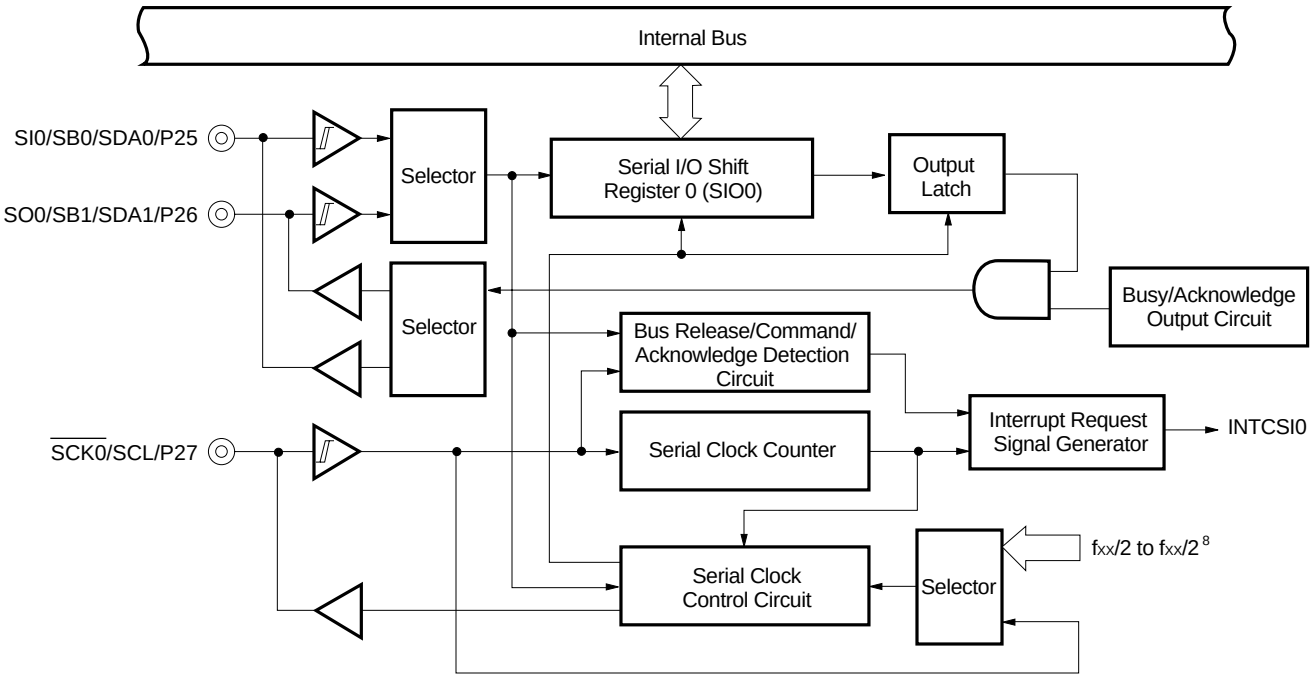
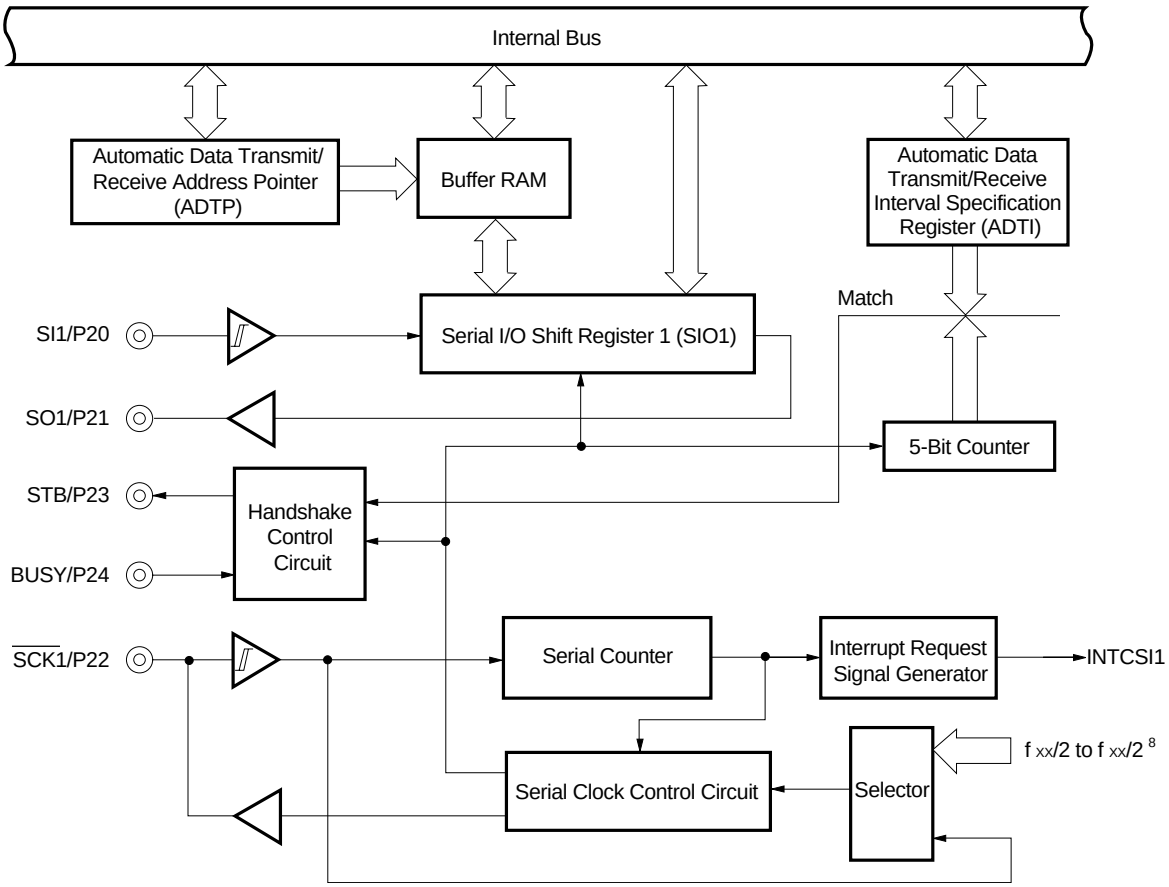
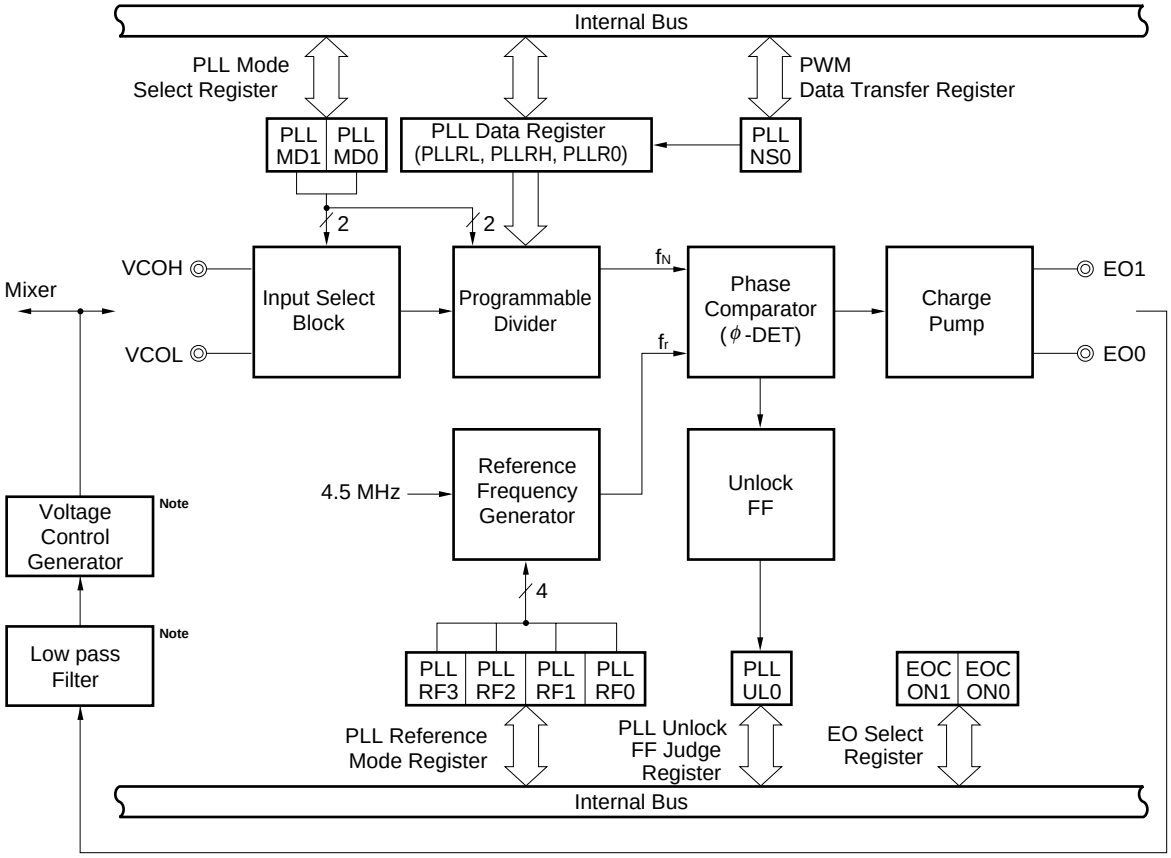


Figure 5-9. Serial Interface Channel 1 Block Diagram



5.7 PLL FREQUENCY SYNTHESIZER

Figure 5-10. PLL Frequency Synthesizer Block Diagram



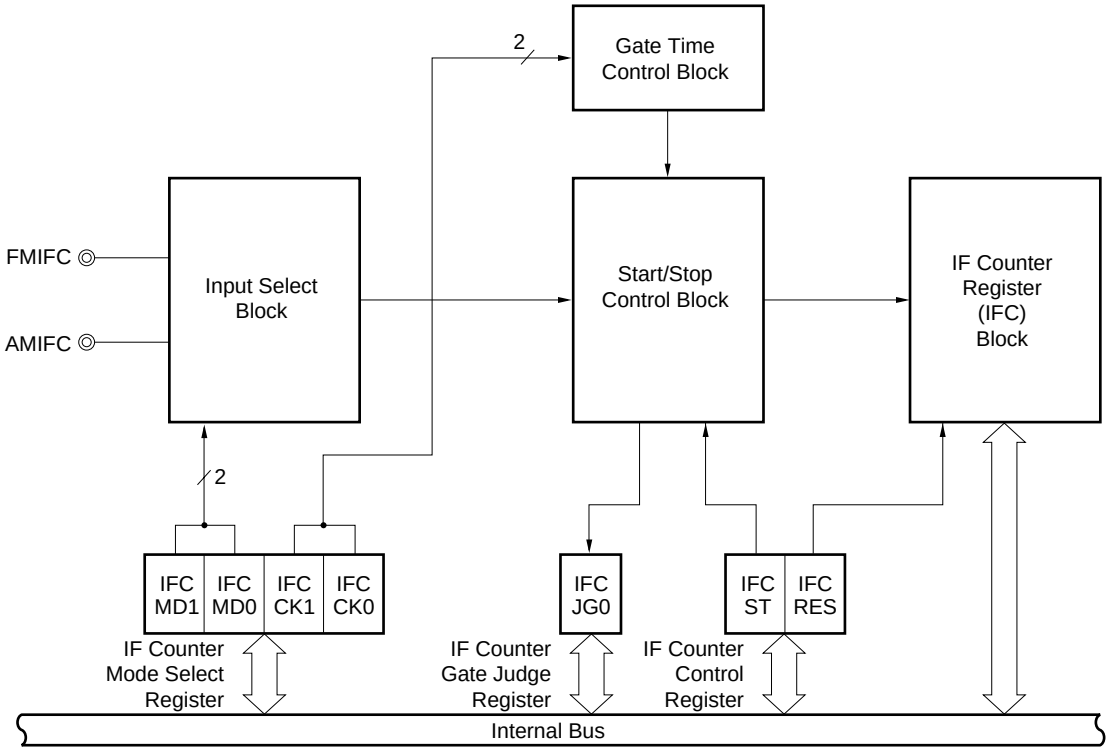
Note External circuit

Cautions 1. Be sure to set EOCON0 to 0.

2. For the μPD178004A and 178006A, do not set EOCON1 to 1.

5.8 FREQUENCY COUNTER

Figure 5-11. Frequency Counter Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 INTERRUPT FUNCTIONS

Interrupt functions include three types and 17 sources, as shown below.

- Non-maskable: 1
- Maskable : 15
- Software : 1

Table 6-1. Interrupt Source List

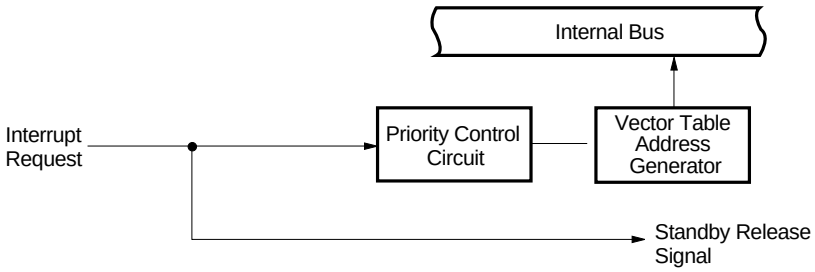
Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTCSI0	End of serial interface channel 0 transfer	Internal	0014H	(B)
	9	INTCSI1	End of serial interface channel 1 transfer		0016H	
	10	INTTMC	Generation of match signal of basic timer		0018H	
	11	INTPWM	Generation of match signal of 8-bit timer		001AH	
	12	INTTM1	Generation of match signal of 8-bit timer/ event counter 1		001CH	
	13	INTTM2	Generation of match signal of 8-bit timer/ event counter 2		001EH	
	14	INTAD	End of conversion by A/D converter		0020H	
Software	—	BRK	BRK instruction execution	Internal	003EH	(E)

Notes 1. The default priority is a priority order when two or more maskable interrupts are generated simultaneously. 0 is the highest order and 14, the lowest.

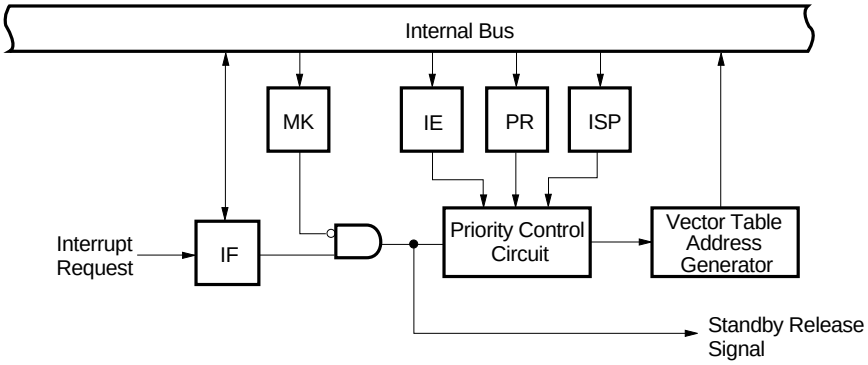
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Figure 6-1. Interrupt Function Basic Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

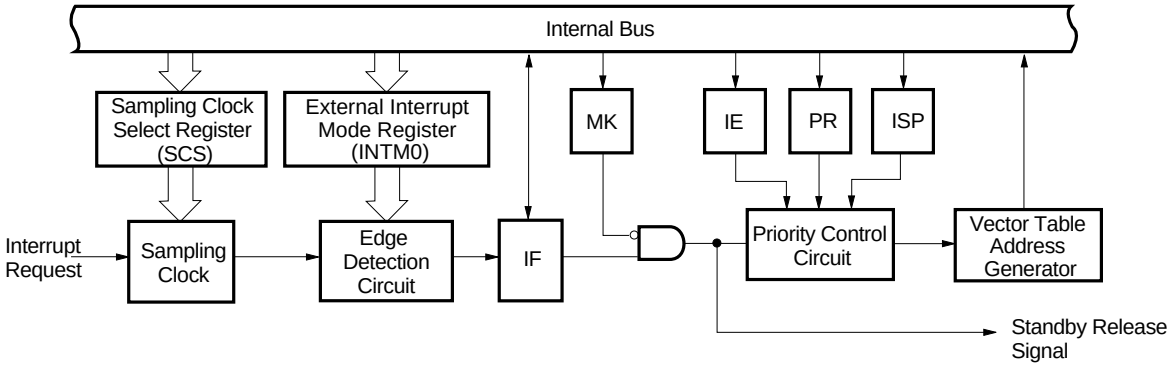
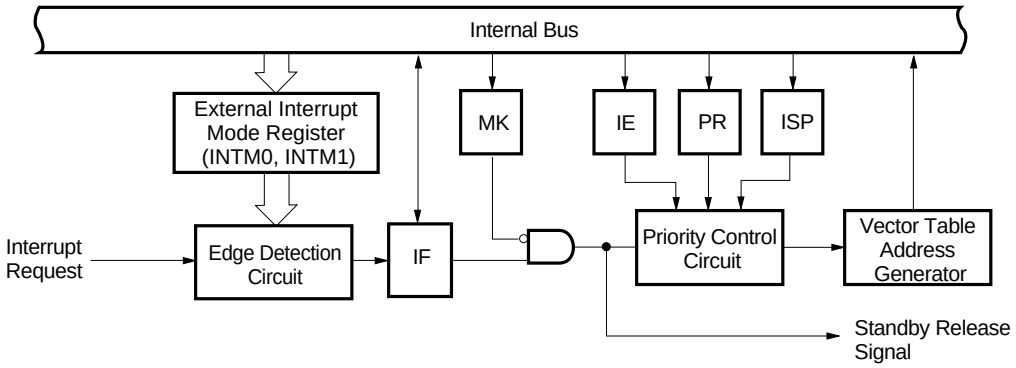
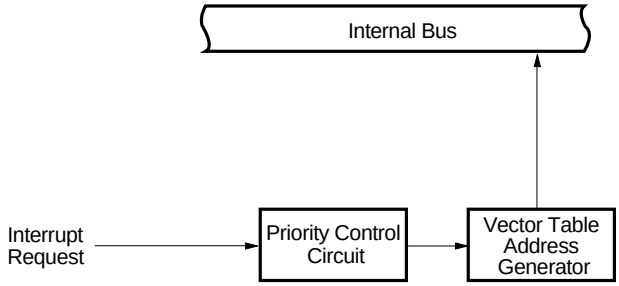


Figure 6-1. Interrupt Function Basic Configuration (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

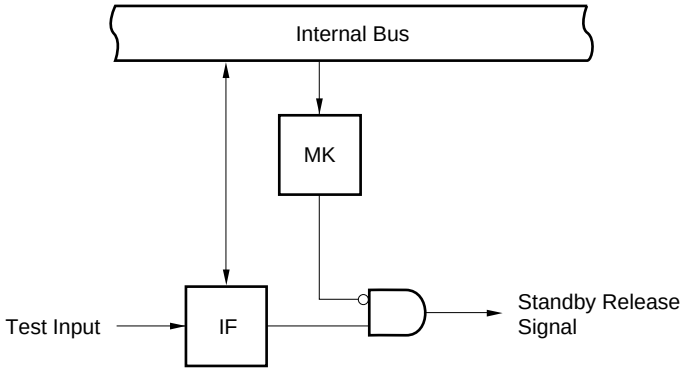
6.2 TEST FUNCTION

A test function with a single source is provided, as shown in Table 6-2.

Table 6-2. Test Input Source List

Test Input Source		Internal/External
Name	Trigger	
INTPT4	Port 4 falling edge detection	External

Figure 6-2. Test Function Basic Configuration



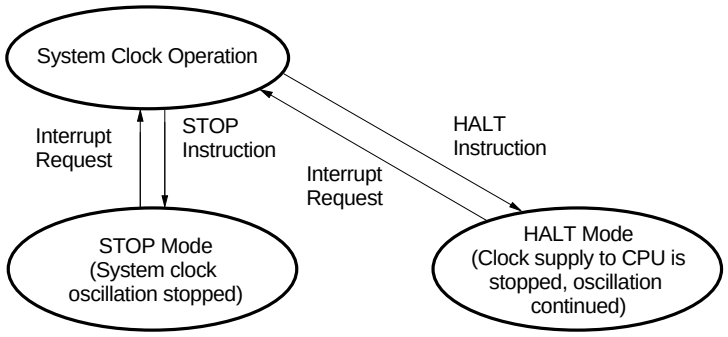
IF : Test input flag
MK : Test mask flag

7. STANDBY FUNCTION

There are the following two standby functions to reduce the system power consumption.

- HALT mode : The CPU operating clock is stopped.
  The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The system clock oscillation is stopped. All operations by the system clock are stopped and current consumption can be considerably reduced.

Figure 7-1. Stand-by Function



8. RESET FUNCTION

There are the following three reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer runaway time detection
- Internal reset by Power-On Clear (POC).

9. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second Operand / First Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B,C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]													
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First Operand \ Second Operand	#word	AX	rp Note	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW Note						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First Operand \ Second Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First Operand \ Second Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Test Conditions			Rating	Unit
Power supply voltage	V_{DD}				–0.3 to + 7.0	V
Input voltage	V_{I1}	Excluding P60 to P63			–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63	N-ch Open-drain		–0.3 to +16	V
Output voltage	V_O				–0.3 to V_{DD} + 0.3	V
Output withstand voltage	V_{BDS}	P132 to P134	N-ch Open-drain		16	V
Analog input voltage	V_{AN}	P10 to P15	Analog input pin		–0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	1 pin			–10	mA
		P01 to P06, P30 to P37, P56, P57, P60 to P67, P120 to P125 total			–15	mA
		P10 to P15, P20 to P27, P40 to P47, P50 to P55, P132 to P134 total			–15	mA
Output current low	I_{OL} **Note**	1 pin		Peak value	15	mA
				Effective value	7.5	mA
Operating ambient temperature	T_A				–40 to +85	°C
Storage temperature	T_{stg}				–65 to +150	°C

Note Effective value should be calculated as follows: [Effective value] = [Peak value] × $\sqrt{\text{duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark The characteristics of alternate-function pins and port pins are the same unless specified otherwise.

RECOMMENDED SUPPLY VOLTAGE RANGES (T_A = –40 to +85 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD1}	During CPU operation and PLL operation.	4.5		5.5	V
	V_{DD2}	While the CPU is operating and the PLL is stopped. Cycle Time: $T_{CY} \geq 0.89\ \mu s$	3.5		5.5	V
	V_{DD3}	While the CPU is operating and the PLL is stopped. Cycle Time: T_{CY} = 0.44 μs	4.5		5.5	V

Remark T_{CY}: Cycle Time (Minimum instruction execution time)

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 3.5 to 5.5 V)

(1/3)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10 to P15, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0.85 V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63 (N-ch Open-drain)		0.7 V_{DD}		15	V
Input voltage low	V_{IL1}	P10 to P15, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125		0		0.3 V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0		0.15 V_{DD}	V
	V_{IL3}	P60 to P63 (N-ch Open-drain)	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3 V_{DD}	V
			3.5 V ≤ V_{DD} < 4.5 V	0		0.2 V_{DD}	V
Output voltage high	V_{OH1}		4.5 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			3.5 V ≤ V_{DD} < 4.5 V, I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 5.5 V, I_{OH} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P15, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P120 to P125, P132 to P134	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, open-drain pulled-up (R = 1 KΩ)			0.2 V_{DD}	V

Remark The characteristics of alternate-function pins and port pins are the same unless specified otherwise.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 3.5 to 5.5 V)

(2/3)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I_{LIH1}	P00 to P06, P10 to P15, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125, $\overline{\text{RESET}}$	$V_{IN} = V_{DD}$			3	μA
	I_{LIH2}	P60 to P63	V_{IN} = 15 V			80	μA
Input leakage current low	I_{LIL1}	P00 to P06, P10 to P15, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P120 to P125, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
	I_{LIL2}	P60 to P63				–3 Note	μA
Output leakage current high	I_{LOH}	P132 to P134	V_{OUT} = 15 V			3	μA
Output leakage current low	I_{LOL}	P132 to P134	V_{OUT} = 0 V			–3	μA
Output off leak current	I_{LOF}	EO0, EO1	$V_{OUT} = V_{DD}$, V_{OUT} = 0 V			±1	μA

Note When an input instruction is executed, the low-level input leakage current for P60 to P63 becomes –200 μA (MAX.) only in one clock cycle (at no wait). It remains at –3 μA (MAX.) for other than an input instruction.

Remark The characteristics of alternate-function pins and port pins are the same unless specified otherwise.

REFERENCE CHARACTERISTICS (T_A = 25 °C, V_{DD} = 5 V)

(1/2)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Output current high	I_{OH1}	EO0	$V_{OUT} = V_{DD}$ – 1 V		–4		mA
		EO1 (EOCON0 = 0)		–1.8			mA
Output current low	I_{OL1}	EO0	V_{OUT} = 1 V		6		mA
		EO1 (EOCON0 = 0)		3.5			mA

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 3.5 to 5.5 V)

(3/3)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Power Supply Note 1 Current	I_{DD1}	While the CPU is operating and the PLL is stopped f_X = 4.5 MHz operation	T_{CY} = 0.89 μs Note 2		2.5	15	mA
	I_{DD2}		T_{CY} = 0.44 μs Note 3 V_{DD} = 4.5 to 5.5 V		4.0	27	mA
	I_{DD3}	While the CPU is operating and the PLL is stopped HALT Mode Pin X1 sine wave input V_{IN} = V_{DD}. f_X = 4.5 MHz operation	T_{CY} = 0.89 μs Note 2		0.7	1.5	mA
	I_{DD4}		T_{CY} = 0.44 μs Note 3 V_{DD} = 4.5 to 5.5 V		1.0	2.0	mA
Data Hold Power Supply Voltage	V_{DR1}	When the crystal is oscillating	T_{CY} = 0.44 μs	4.5		5.5	V
	V_{DR2}		T_{CY} = 0.89 μs	3.5		5.5	V
	V_{DR3}	When the crystal oscillator is stopped When power off by Power On Clear is detected		2.6		5.5	V
Data Hold Power Supply Current	I_{DR1}	While the crystal oscillator is stopped	T_A = 25 °C, V_{DD} = 5V		2	4	μA
	I_{DR2}				2	30	μA

Notes 1. The port current is not included.

2. When the Processor Clock Control register (PCC) is set at 00H, and the Oscillation Mode Select register (OSMS) is set at 00H.

3. When PCC is set at 00H and OSMS is set at 01H.

Remarks 1. T_{CY}: Cycle Time (Minimum instruction execution time)

2. fx: System clock oscillator frequency.

REFERENCE CHARACTERISTICS (T_A = 25 °C, V_{DD} = 5 V)

(2/2)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Power Supply Current	I_{DD5}	During CPU operation and PLL operation. VCOH pin sine wave input f_{IN} = 130 MHz, V_{IN} = 0.15 V_{p-p}	T_{CY} = 0.44 μs Note		7		mA

Note When the Processor Clock Control register (PCC) is set at 00H, and the Oscillation Mode Select register (OSMS) is set at 01H.

Remark T_{CY}: Cycle Time (Minimum instruction execution time)

AC CHARACTERISTICS

(1) BASIC OPERATION (T_A = –40 to +85 °C, V_{DD} = 3.5 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Minimum instruction execution time)	T_{CY}	$f_{XX} = f_X/2$ Note 1, f_X = 4.5 MHz operation		0.89		14.22	μs
		$f_{XX} = f_X$ Note 2, f_X = 4.5 MHz operation	4.5 ≤ V_{DD} ≤ 5.5 V	0.44		7.11	μs
			3.5 ≤ V_{DD} < 4.5 V	0.89		7.11	μs
TI1, TI2 input frequency	f_{TI}	4.5 ≤ V_{DD} ≤ 5.5 V		0		4.5	MHz
		3.5 V ≤ V_{DD} ≤ 4.5 V		0		275	kHz
TI1, TI2 input high/low-level width	t_{TIH}, t_{TIL}	4.5 ≤ V_{DD} ≤ 5.5 V		111			ns
		3.5 V ≤ V_{DD} ≤ 4.5 V		1.8			μs
Interrupt input high/low-level width	T_{INTH}, T_{INTL}	INTP0		8/f_{sam} Note 3			μs
		INTP1 to INTP6		10			μs
$\overline{RESET}$ low level width	t_{RSL}			10			μs

Notes 1. When oscillation mode selection (OSMS) register is set at 00H.

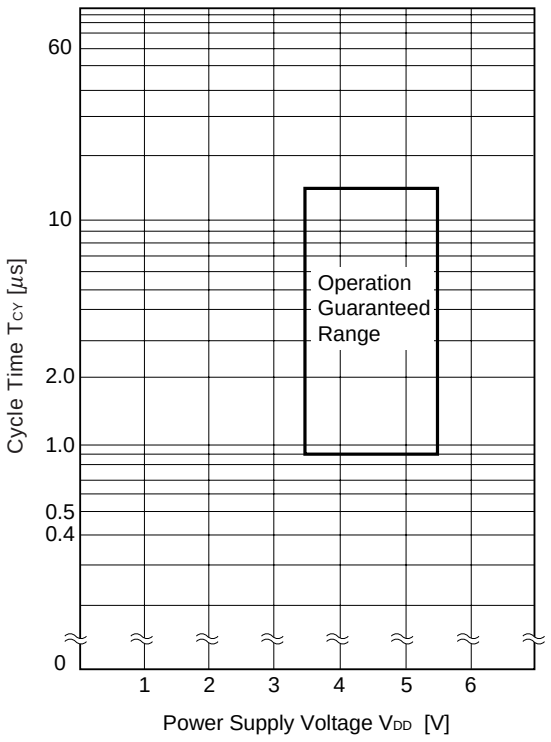
2. When OSMS is set at 01H.

3. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible between $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$ and $f_{XX}/128$ (when N = 0 to 4).

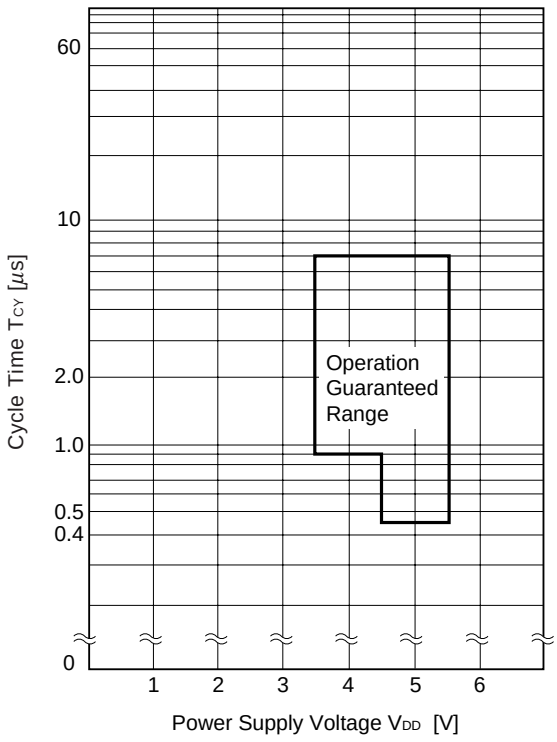
Remarks 1. f_{XX}: System clock frequency (f_X or $f_X/2$)

2. f_X: System clock oscillation frequency

T_{CY} vs V_{DD} (At $F_{XX} = F_X/2$ system clock operation)



T_{CY} vs V_{DD} (At $F_{XX} = F_X$ system clock operation)



(2) SERIAL INTERFACE (T_A = –40 to +85 °C, V_{DD} = 3.5 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		3.5 V ≤ V_{DD} < 4.5 V	1 600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}, t_{KL1}	4.5 V ≤ V_{DD} ≤ 5.5 V	$t_{KCY1}/2$ – 50			ns
		3.5 V ≤ V_{DD} < 4.5 V	$t_{KCY1}/2$ – 100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		3.5 V ≤ V_{DD} < 4.5 V	150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		3.5 V ≤ V_{DD} < 4.5 V	1 600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		3.5 V ≤ V_{DD} < 4.5 V	800			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF **Note**			300	ns
$\overline{SCK0}$ at rising or falling edge time	t_{R2}, t_{F2}				1 000	ns

Note C is the load capacitance of SO0 output line.

(iii) SBI mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		3.5 V ≤ V_{DD} < 4.5 V		3 200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH3}, t_{KL3}	4.5 V ≤ V_{DD} ≤ 5.5 V		$t_{KCY3}/2 - 50$			ns
		3.5 V ≤ V_{DD} < 4.5 V		$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		3.5 V ≤ V_{DD} < 4.5 V		300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			$t_{KCY3}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO3}	R = 1 kΩ, C = 100 pF Note	4.5 V ≤ V_{DD} ≤ 5.5 V	0		250	ns
			3.5 V ≤ V_{DD} < 4.5 V	0		1 000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistance and load capacitance of SB0 and SB1 output line.

(iv) SBI mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		3.5 V ≤ V_{DD} < 4.5 V		3 200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH4}, t_{KL4}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		3.5 V ≤ V_{DD} < 4.5 V		1 600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	4.5 V ≤ V_{DD} ≤ 5.5 V		100			ns
		3.5 V ≤ V_{DD} < 4.5 V		300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF Note	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			3.5 V ≤ V_{DD} < 4.5 V	0		1 000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ at rising or falling edge time	t_{R4}, t_{F4}					1 000	ns

Note R and C are the load resistance and load capacitance of SB0 and SB1 output line.

(v) 2-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ		1 600			ns
$\overline{SCK0}$ high-level width	t_{KH5}	C = 100 pF Note		$t_{KCY5}/2 - 160$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		$4.5\ V \le V_{DD} \le 5.5\ V$	$t_{KCY5}/2 - 50$			ns
			$3.5\ V \le V_{DD} < 4.5\ V$	$t_{KCY5}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK5}		$4.5\ V \le V_{DD} \le 5.5\ V$	300			ns
			$3.5\ V \le V_{DD} < 4.5\ V$	350			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}\downarrow$	t_{KSO5}			0		300	ns

Note R and C are the load resistance and load capacitance of $\overline{SCK0}$, SB0 and SB1 output line.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}			1 600			ns
$\overline{SCK0}$ high-level width	t_{KH6}			650			ns
$\overline{SCK0}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}\downarrow$	t_{KSO6}	R = 1 kΩ	$4.5\ V \le V_{DD} \le 5.5\ V$	0		300	ns
		C = 100 pF Note	$3.5\ V \le V_{DD} < 4.5\ V$	0		500	ns
$\overline{SCK0}$ at rising or falling edge time	t_{R6}, t_{F6}					1 000	ns

Note R and C are the load resistance and load capacitance of SB0 and SB1 output line.

(vii) I²C Bus mode (SCL ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY7}	R = 1 kΩ		10			μs
SCL high-level width	t_{KH7}	C = 100 pF Note		t_{KCY7} – 160			ns
SCL low-level width	t_{KL7}				t_{KCY7} – 50		ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK7}				200		ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI7}			0			ns
SDA0, SDA1 output delay time (from SCL↓)	t_{KSO7}		4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			3.5 V ≤ V_{DD} < 4.5 V	0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns

Note R and C are the load resistance and load capacitance of SCL, SDA0 and SDA1 output line.

(viii) I²C Bus mode (SCL ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY8}			1 000			ns
SCL high-/low-level width	t_{KH8}, t_{KL8}			400			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK8}				200		ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI8}			0			ns
SDA0, SDA1 output delay time from SCL↓	t_{KSO8}	R = 1 kΩ	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
		C = 100 pF Note	3.5 V ≤ V_{DD} < 4.5 V	0		500	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns
SCL at rising or falling edge time	t_{R8}, t_{F8}					1 000	ns

Note R and C are the load resistance and load capacitance of SDA0 and SDA1 output line.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		3.5 V ≤ V_{DD} < 4.5 V	1 600			ns
$\overline{SCK1}$ high/low-level width	t_{KH9}, t_{KL9}	4.5 V ≤ V_{DD} ≤ 5.5 V	$t_{KCY9}/2 - 50$			ns
		3.5 V ≤ V_{DD} < 4.5 V	$t_{KCY9}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		3.5 V ≤ V_{DD} < 4.5 V	150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time (from $\overline{SCK1}$↓)	t_{KSO9}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		3.5 V ≤ V_{DD} < 4.5 V	1 600			ns
$\overline{SCK1}$ high/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		3.5 V ≤ V_{DD} < 4.5 V	800			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI10}		400			ns
SO1 output delay time (from $\overline{SCK1}$↓)	t_{KSO10}	C = 100 pF **Note**			300	ns
$\overline{SCK1}$ at rising or falling edge time	t_{R10}, t_{F10}				1 000	ns

Note C is the load capacitance of SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		3.5 V ≤ V_{DD} < 4.5 V	1 600			ns
$\overline{SCK1}$ high/low-level width	t_{KH11}, t_{KL11}	4.5 V ≤ V_{DD} ≤ 5.5 V	t_{KCY11}/2 – 50			ns
		3.5 V ≤ V_{DD} < 4.5 V	t_{KCY11}/2 – 100			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK11}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		3.5 V ≤ V_{DD} < 4.5 V	150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI11}		400			ns
SO1 output delay time (from $\overline{SCK1}$↓)	t_{KSO11}	C = 100 pF [Note]			300	ns
STB↑ from SCK1↑	t_{SBD}		t_{KCY11}/2 – 100		t_{KCY11}/2 + 100	ns
Strobe signal high-level width	t_{SBW}		t_{KCY11}/ – 30		t_{KCY11} + 30	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		3.5 V ≤ V_{DD} < 4.5 V	150			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				2t_{KCY11}	ns

Note C is the load capacitance of SO1 output line.

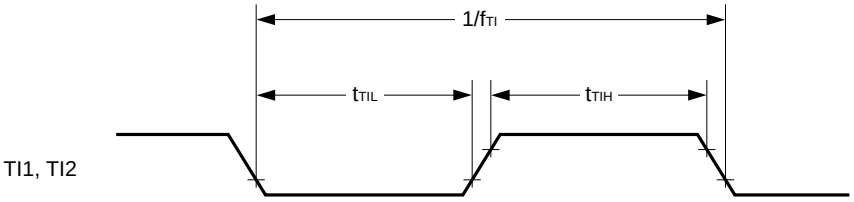
(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY12}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		3.5 V ≤ V_{DD} < 4.5 V	1 600			ns
$\overline{SCK1}$ high/low-level width	t_{KH12}, t_{KL12}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		3.5 V ≤ V_{DD} < 4.5 V	800			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK12}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI12}		400			ns
SO1 output delay time (from $\overline{SCK1}$↓)	t_{KSO12}	C = 100 pF [Note]			300	ns
$\overline{SCK1}$ at rising or falling edge time	t_{R12}, t_{F12}				1 000	ns

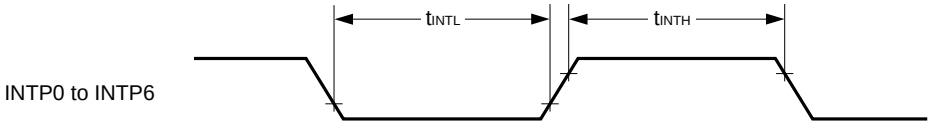
Note C is the load capacitance of SO1 output line.

AC TIMING TEST POINT (EXCLUDING X1 INPUT)

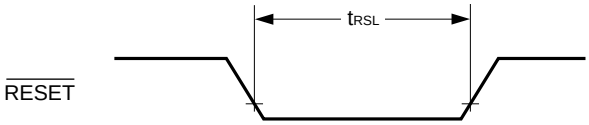
TI Timing



Interrupt Input Timing

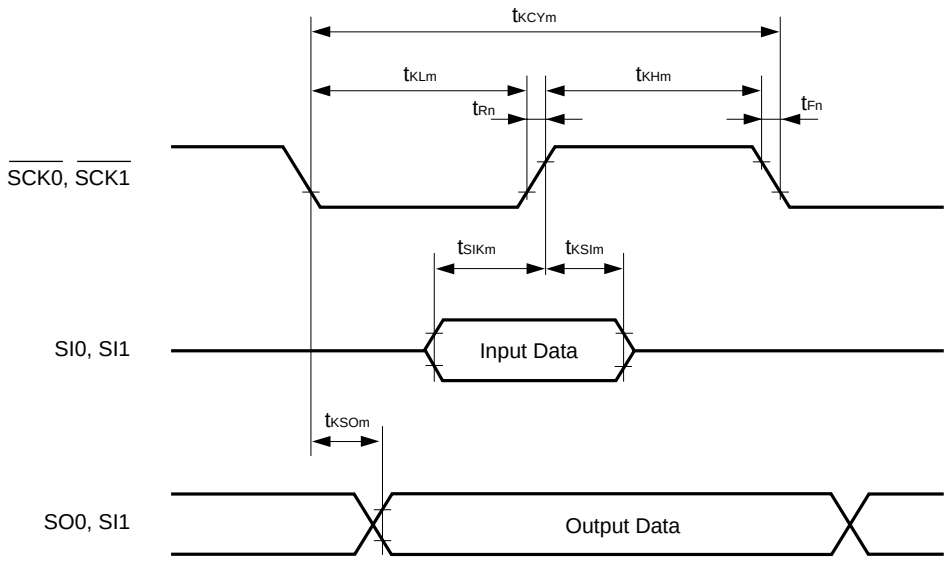


$\overline{\text{RESET}}$ Input Timing



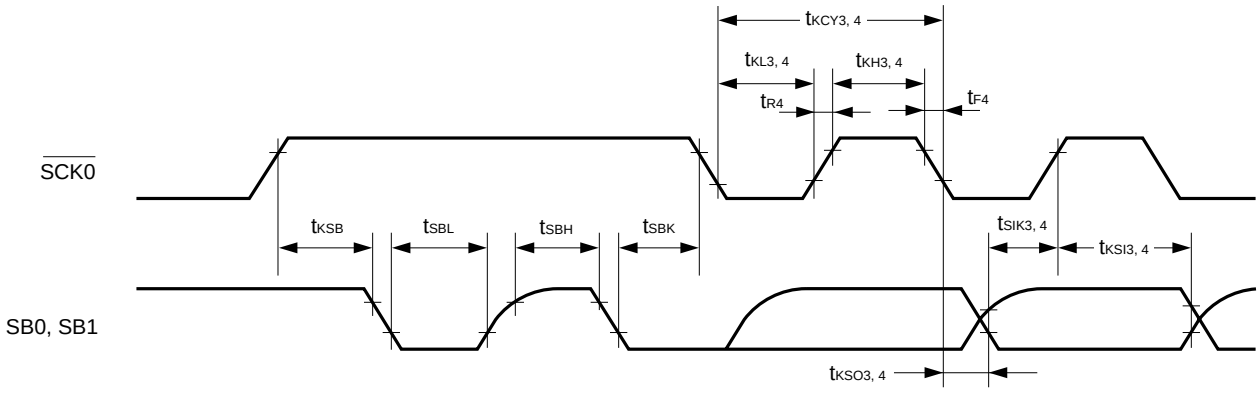
SERIAL TRANSFER TIMING

3-Wire Serial I/O Mode:

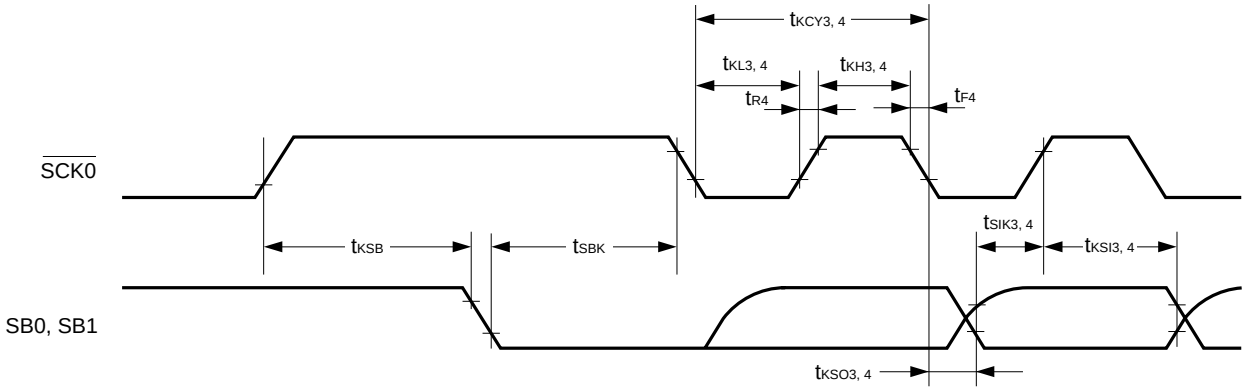


Remark m = 1, 2, 9, 10
n = 2, 10

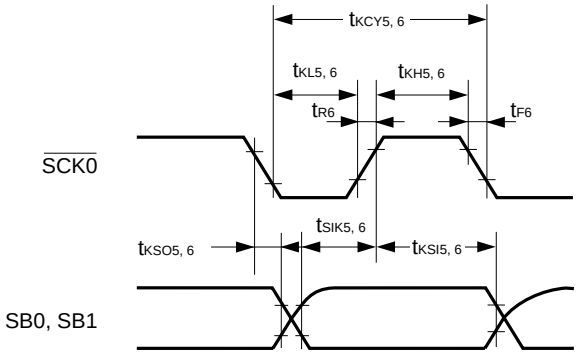
SBI Mode (Bus Release Signal Transfer):



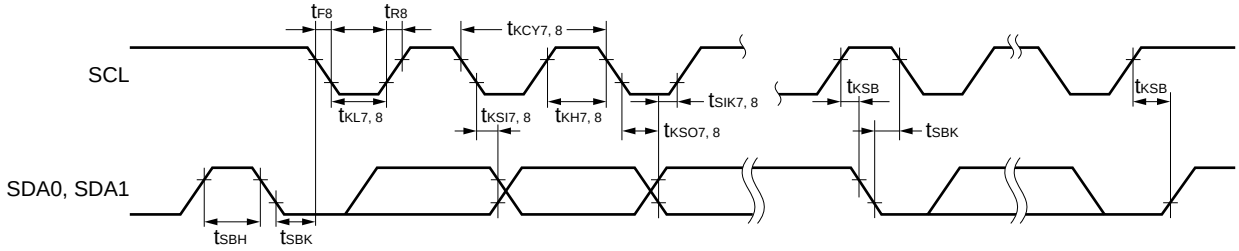
SBI Mode (Command Signal Transfer):



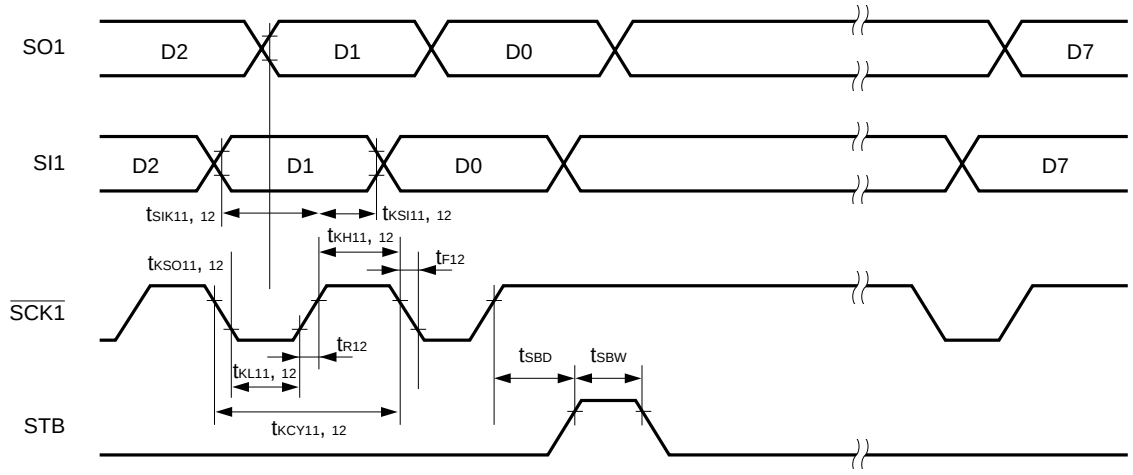
2-Wire Serial I/O Mode:



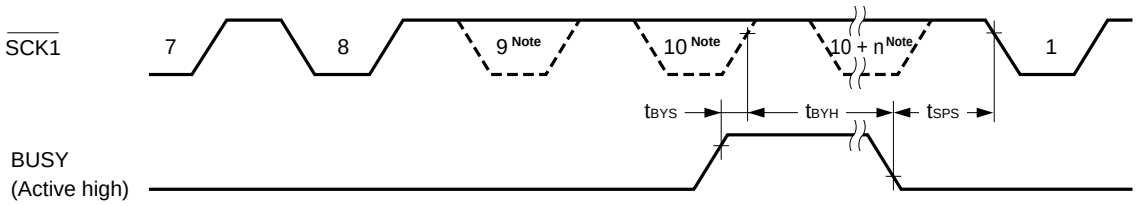
I²C Bus Mode:



3-Wire Serial I/O Mode with Automatic Transmit/Receive Function:



3-Wire Serial I/O Mode with Automatic Transmit/Receive Function (Busy Processing):



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Conversion total error					±3.0	LSB
Conversion time	t_{CONV}		22.2		44.4	μs
Sampling time	t_{SAMP}		15/f_{XX}			μs
Analog input voltage	V_{IAN}		0		V_{DD}	V

Remarks 1. f_{XX}: System clock frequency (f_X/2)

2. f_X: System clock oscillation frequency

PLL CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Operating Frequency	f_{IN1}	VCOL Pin MF Mode Sine wave input V_{IN} = 0.1 V_{p-p}	0.5		3	MHz
	f_{IN2}	VCOL Pin HF Mode Sine wave input V_{IN} = 0.2 V_{p-p}	9		55	MHz
	f_{IN3}	VCOH Pin VHF Mode Sine wave input V_{IN} = 0.15 V_{p-p}	60		160	MHz

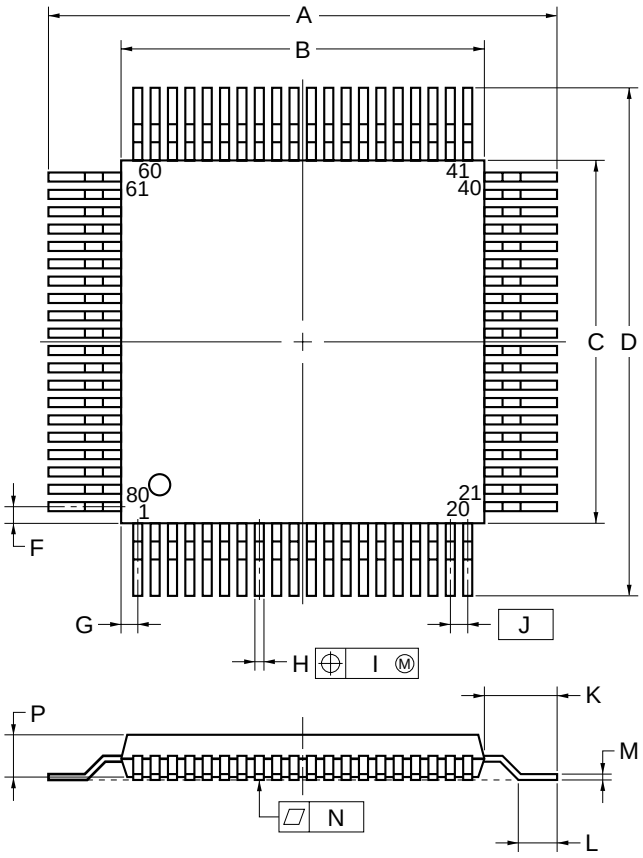
IFC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Operating Frequency	f_{IN4}	AMIFC Pin AMIF Count Mode Sine wave input V_{IN} = 0.1 V_{p-p} **Note**	0.4		0.5	MHz
	f_{IN5}	FMIFC Pin FMIF Count Mode Sine wave input V_{IN} = 0.1 V_{p-p} **Note**	10		11	MHz
	f_{IN6}	FMIFC Pin AMIF Count Mode Sine wave input V_{IN} = 0.1 V_{p-p} **Note**	0.4		0.5	MHz

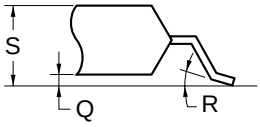
Note The condition of a sine wave input of V_{IN} = 0.1 V_{p-p} is the standard value for operation of this device during stand-alone operation, so in consideration of the effect of noise, it is recommended that operation be at an input amplitude condition of V_{IN} = 0.15 V_{p-p}.

11. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-4

12. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 12-1. Surface Mounting Type Soldering Conditions

μPD178004AGC-×××-3B9 : 80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)
μPD178006AGC-×××-3B9 : 80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)
μPD178016AGC-×××-3B9 : 80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)
μPD178018AGC-×××-3B9 : 80-pin plastic QFP (14 × 14 mm, 0.65 mm pitch)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Three times max.	IR35-00-3
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Three times max.	VP15-00-3
Wave soldering	Solder bath temperature : 260 °C max., Duration : 10 sec. max., Number of times : once, Preheating temperature : 120 °C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max. Duration: 3 sec. max. (per pin row)	—

Caution Do not use different soldering method together (except for partial heating).

APPENDIX A. DIFFERENCES BETWEEN μPD178018A AND μPD178018 SUBSERIES

Item \ Product name		μPD178018A Subseries				μPD178018 Subseries			
		μPD178004A	μPD178006A	μPD178016A	μPD178018A μPD178P018A Note	μPD178004	μPD178006	μPD178016	μPD178018 μPD178P018
PLL frequency synthe-sizer	Reference frequency	7 types selectable by program (1, 3, 5, 9, 10, 25, 50 kHz)				11 types selectable by program (1, 1.25, 2.5, 3, 5, 6.25, 9, 10, 12.5, 25, 50 kHz)			
	EO0 pin output format	Buffer type							
	EO1 pin output format	Buffer type				Constant-current power supply type			
	EO1 pin high-impedance function	Not supported		Supported		Not supported			

Note Under development

Remark The mask ROM of mask versions (μPD178018A and μPD178018) is replaced with one-time PROM or EPROM in the one-time PROM versions (μPD178P018A and μPD178P018).

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD178018A Subseries.

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	78K/0 Series common assembler package
CC78K/0 Notes 1, 2, 3, 4	78K/0 Series common C compiler package
DF178018 Notes 1, 2, 3, 4, 8	μPD178018A Subseries common device file
CC78K/0-L Notes 1, 2, 3, 4	78K/0 Series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PG-178P018GC	Programmer adapters connected to a PG-1500
PA-178P018KK-T	
PG-1500 controller Notes 1, 2	PG-1500 control program

Debugging Tools

IE-78000-R	In-circuit emulator common to 78K/0 Series
IE-78000-R-A	In-circuit emulator common to 78K/0 Series (for the integration debugger)
IE-78000-R-BK	Break board common to 78K/0 Series
IE-178018-R-EM	Emulation board common to μPD178018A Subseries
IE-78000-R-SV3	Interface adapter and cable when using EWS as a host machine (for IE-78000-R-A)
IE-70000-98-IF-B	Interface adapter when using the PC-9800 Series (except notebooks) as a host machine (for IE-78000-R-A)
IE-70000-98N-IF	Interface adapter and cable when using the PC-9800 Series notebook as a host machine (for IE-78000-R-A)
IE-70000-PC-IF-B	Interface adapter when using IBM PC/AT™ as a host machine (for IE-78000-R-A)
EP-78230GC-R	Emulation probe common to μPD78234 Subseries
EV-9200GC-80	Socket for mounting on target system board created for 80-pin plastic QFP (GC-3B9 type)
EV-9900	Jig used when removing the μPD178P018AKK-T from the EV-9200GC-80.
SM78K0 Notes 5, 6, 7	78K/0 Series common system simulator
ID78K0 Notes 4, 5, 6, 7	Integration debugger for IE-78000-R-A
SD78K/0 Notes 1, 2	IE-78000-R screen debugger
DF178018 Notes 1, 2, 4, 5, 6, 7, 8	μPD178018A Subseries device file

Real-Time OS

RX78K/0 Notes 1, 2, 3, 4	78K/0 Series real-time OS
MX78K0 Notes 1, 2, 3, 4	78K/0 Series OS

Notes 1. PC-9800 Series (MS-DOS™) based
2. IBM PC/AT and compatible (PC DOS™/IBM-DOS™/MS-DOS) based
3. HP9000 Series 300™ based
4. HP9000 Series 700™ (HP-UX™) based, SPARCstation™ (SunOS™) based, EWS4800 Series (EWS-UX/V) based
5. PC-9800 Series (MS-DOS + Windows™) based
6. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based
8. Under development

Fuzzy Inference Development Support System

FE9000 Note 1/FE9200 Note 2	Fuzzy knowledge data creation tool
FT9080 Note 1/FT9085 Note 3	Translator
FI78K0 Notes 1, 3	Fuzzy inference module
FD78K0 Notes 1, 3	Fuzzy inference debugger

Notes 1. PC-9800 Series (MS-DOS) based
2. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based
3. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS) based

Remarks 1. Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on third party development tools.
2. The RA78K/0, CC78K/0, SD78K/0, ID78K/0, SM78K/0 and RX78K/0 are used in combination with the DF178018.

APPENDIX C. RELATED DOCUMENTS

Device Documents

Title		Document No. (Japanese)	Document No. (English)
μPD178018A Subseries User's Manual		To be prepared	To be prepared
78K/0 Series User's Manual—Instruction		U12326J	U12326E
78K/0 Series Instruction Set		U10904J	—
78K/0 Series Instruction Table		U10903J	—
μPD178018A Subseries Special Function Register Table		To be prepared	—
78K/0 Series Application Note	Basics (II)	U10121J	U10121E

Development Tool Documents (User's Manual)

Title		Document No. (Japanese)	Document No. (English)
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly Language	U11801J	U11801E
	Structured Assembly Language	U11789J	U11789E
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K/0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Notes	Programming Know-how	EEA-618	EEA-1208
CC78K Series Library Source File		U12322J	—
PG-1500 PROM Programmer		U11940J	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	U10540E
IE-78000-R		U11376J	U11376E
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-178018-R-EM		U10668J	U10668E
EP-78230		EEU-985	EEU-1515
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External Parts User open Interface Specifications	U10092J	U10092E
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	U11151E
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E
SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) Based	Introduction	EEU-852	U10539E
	Reference	U10952J	—
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) Based	Introduction	EEU-5024	EEU-1414
	Reference	U11279J	U11279E

Caution The contents of the above documents are subject to change without notice. Please ensure that the latest versions are used in design work, etc.

Related Documents for Embedded Software (User's Manual)

Title		Document No. (Japanese)	Document No. (English)
78K/0 Series Realtime OS	Basics	U11537J	—
	Installation	U11536J	—
78K/0 Series OS MX78K0	Basics	U12257J	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System—Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System—Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System —Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Title	Document No. (Japanese)	Document No. (English)
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Guides on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability and Quality Control	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Semiconductor Device Quality Assurance Guide	C11893J	MEI-1202
Microcomputer-related Product Guide (Products by other Manufacturers)	U11416J	—

Caution The contents of the above documents are subject to change without notice. Ensure that the latest versions are used in design work, etc.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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J96. 8

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