

DRAM

1024K x 16 DYNAMIC RAM

EDO PAGE MODE

FEATURES

- Industry-standard x 16 pinouts and timing functions.
- Single 5V (±10%) power supply.
- All device pins are TTL- compatible.
- 1K-cycle refresh in 16ms.
- Refresh modes: $\overline{\text{RAS}}$ only, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ (CBR) and HIDDEN.
- Extended data-out (EDO) PAGE MODE access cycle.
- BYTE WRITE and BYTE READ access cycles.

OPTION

TIMING	MARKING
45ns	-45
50ns	-50
60ns	-60

PACKAGE

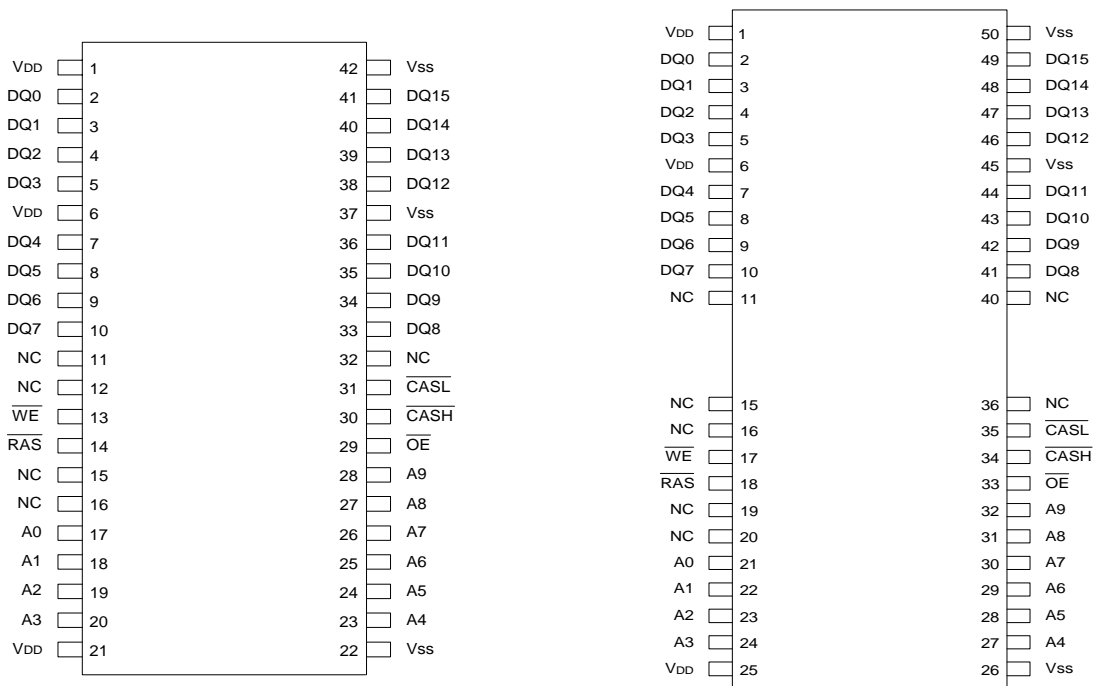
42-pin SOJ	J
44/50-pin TSOPII	S

GENERAL DESCRIPTION

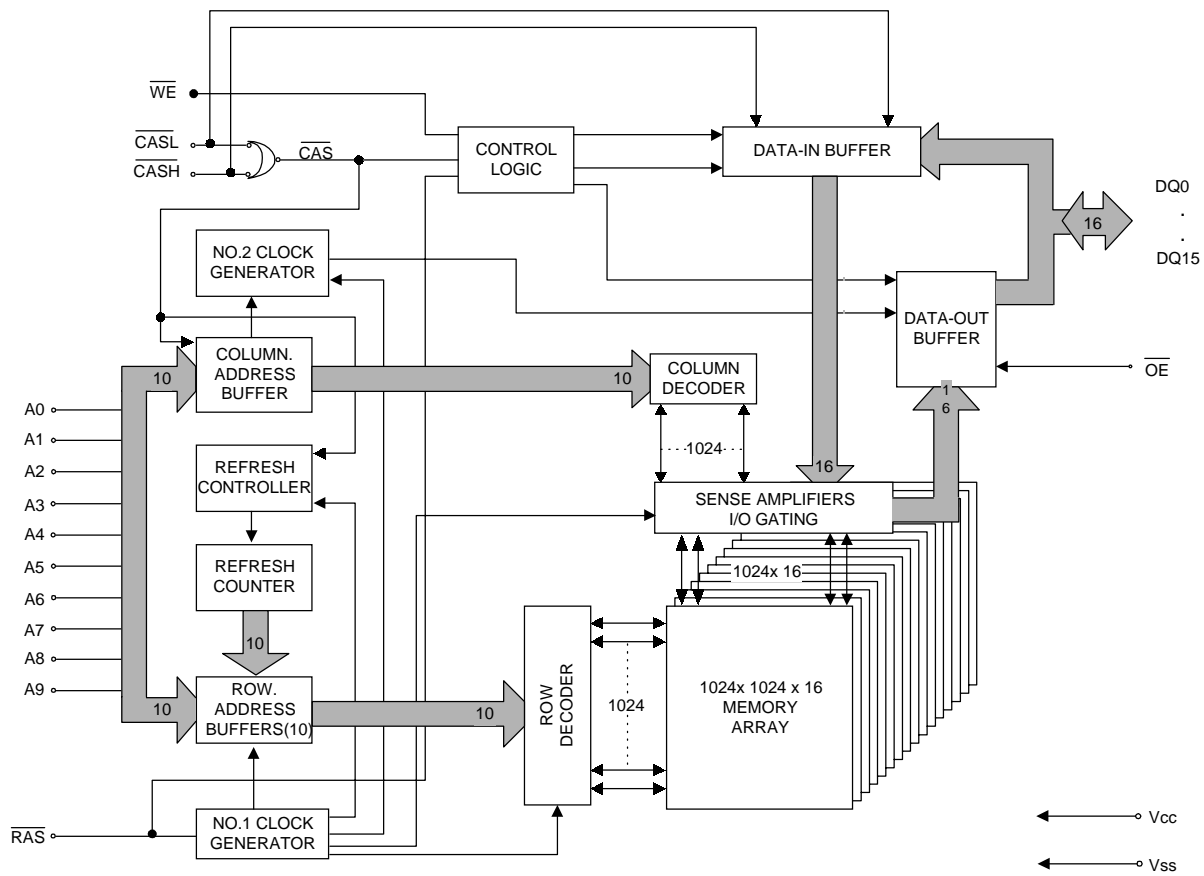
The T2316162A is a randomly accessed solid state memory containing 16,777,216 bits organized in a x16 configuration. The T2316162A has both BYTE WRITE and WORD WRITE access cycles via two $\overline{\text{CAS}}$ pins. It offers Fast Page mode with Extended Data Output.

The T2316162A $\overline{\text{CAS}}$ function and timing are determined by the first $\overline{\text{CAS}}$ to transition low and by the last to transition back high. Use only one of the two $\overline{\text{CAS}}$ and leave the other staying high during WRITE will result in a BYTE WRITE. $\overline{\text{CASL}}$ transiting low in a WRITE cycle will write data into the lower byte (DQ0~DQ7), and $\overline{\text{CASH}}$ transiting low will write data into the upper byte (DQ8~DQ15).

PIN ASSIGNMENT (Top View)



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SYM.	TYPE	DESCRIPTION
A0-A9	Input	Address Input
$\overline{\text{RAS}}$	Input	Row Address Strobe
$\overline{\text{CASH}}$	Input	Column Address Strobe /Upper Byte Control
$\overline{\text{CASL}}$	Input	Column Address Strobe /Lower Byte Control
$\overline{\text{WE}}$	Input	Write Enable
$\overline{\text{OE}}$	Input	Output Enable
DQ0 – DQ15	Input/ Output	Data Input/ Output
Vcc	Supply	Power, 5V
Vss	Ground	Ground
NC	-	No Connect

CAPACITANCE

(Ta =25°C, Vcc =5V ±10 %)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (address)	C _{I1}	-	5	pF	1
Input Capacitance (clocks)	C _{I2}	-	7	pF	1
Output Capacitance (data-in, data-out)	C _{DQ}	-	10	pF	1

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

AC ELECTRICAL CHARACTERISTICS (note 14)

(Ta =0 to 70°C, Vcc=5V ±10 %, Vss=0V)

Test Conditions (note 29)

AC CHARACTERISTICS PARAMETER	SYM	-45		-50		-60		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Read or Write Cycle Time	t _{RC}	80		84		110		ns	
Read Write Cycle Time	t _{RWC}	105		113		140		ns	
EDO-Page-Mode Read or Write Cycle Time	t _{PC}	16		20		25		ns	22
EDO-Page-Mode Read-Write Cycle Time	t _{PCM}	46		58		70		ns	22
Access Time From $\overline{\text{RAS}}$	t _{RAC}		45		50		60	ns	4
Access Time From $\overline{\text{CAS}}$	t _{CAC}		11		13		15	ns	5,20
Access Time From $\overline{\text{OE}}$	t _{OAC}		11		13		15	ns	13,20
Access Time From Column Address	t _{AA}		19		25		30	ns	
Access Time From $\overline{\text{CAS}}$ Precharge	t _{ACP}		22		27		35	ns	20
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	45	10K	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ Pulse Width (EDO Page Mode)	t _{RASC}	45	100K	50	100K	60	100K	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	11		13		15		ns	27
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	28		30		40		ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	6	10K	8	10K	15	10K	ns	26
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	40		40		60		ns	19
$\overline{\text{CAS}}$ Precharge Time (EDO Page Mode)	t _{CP}	5		6		10		ns	23
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	10	34	12	37	20	45	ns	7,18
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5		5		5		ns	19
Row Address Setup Time	t _{ASR}	0		0		0		ns	
Row Address Hold Time	t _{RAH}	5		8		10		ns	
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	8	26	10	28	12	30	ns	8
Column Address Setup Time	t _{ASC}	0		0		0		ns	18
Column Address Hold Time	t _{CAH}	6		8		10		ns	18
Column Address Hold Time (Reference to $\overline{\text{RAS}}$)	t _{AR}	35		38		45		ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	19		23		30		ns	

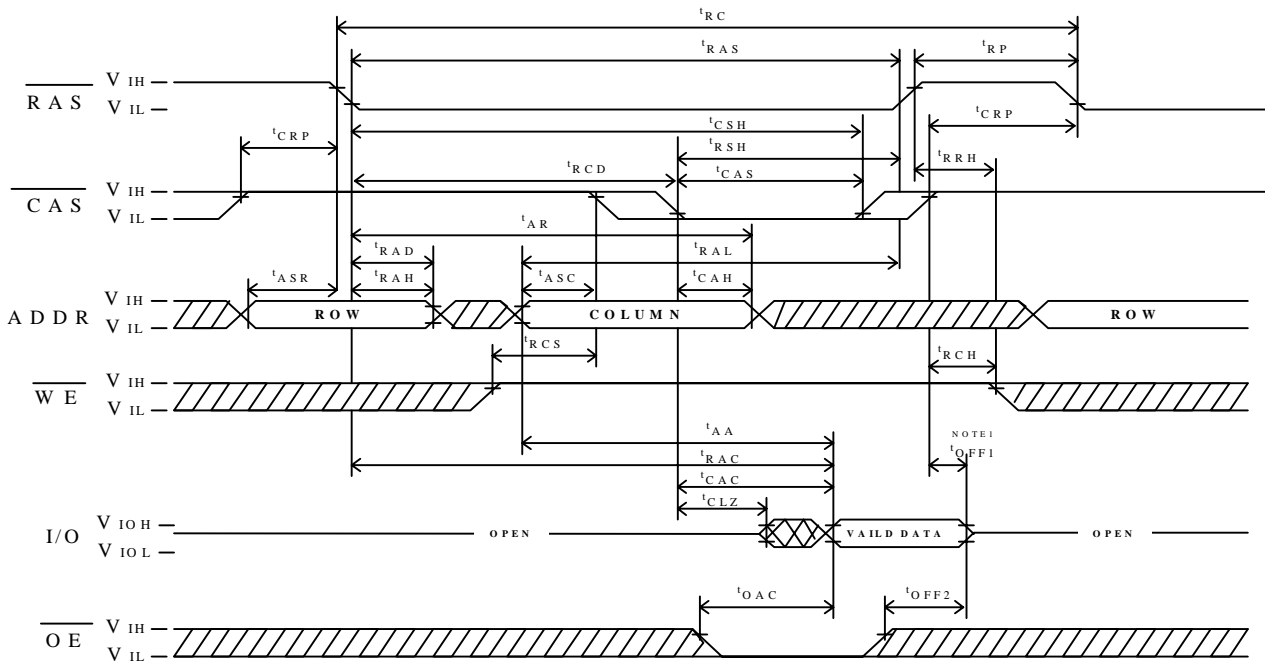
AC ELECTRICAL CHARACTERISTICS (continued)

AC CHARACTERISTICS PARAMETER	SYM	-45		-50		-60		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Command Setup Time	t _{RCS}	0		0		0		ns	15,18
Read Command Hold Time Reference to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	9,15,19
Read Command Hold Time Reference to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	9
$\overline{\text{CAS}}$ to Output in Low-Z	t _{CLZ}	3		3		3		ns	20
Output Buffer Turn-off Delay From $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$	t _{OFF1}	3	15	3	15	3	15	ns	10,17,20
Output Buffer Turn-off to $\overline{\text{OE}}$	t _{OFF2}		8		8		15	ns	17,28
Write Command Setup Time	t _{WCS}	0		0		0		ns	11,15,18
Write Command Hold Time	t _{WCH}	6		8		10		ns	15,27
Write Command Hold Time (Reference to $\overline{\text{RAS}}$)	t _{WCR}	35		38		45		ns	15
Write Command Pulse Width	t _{WP}	6		8		15		ns	15
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	9		9		10		ns	15
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	8		8		10		ns	15,19
Data-in Setup Time	t _{DS}	0		0		0		ns	12,20
Data-in Hold Time	t _{DH}	6		8		10		ns	12,20
Data-in Hold Time (Reference to $\overline{\text{RAS}}$)	t _{DHR}	35		38		45		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	61		64		85		ns	11
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	35		39		55		ns	11
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	27		27		40		ns	11,18
Transition Time (rise or fall)	t _T	2.5	50	2.5	50	2.5	50	ns	2,3
Refresh Period (1024 cycles)	t _{REF}		16		16		16	ms	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	t _{RPC}	10		10		10		ns	
$\overline{\text{CAS}}$ Setup Time (CBR REFRESH)	t _{CSR}	10		10		10		ns	1,18
$\overline{\text{CAS}}$ Hold Time (CBR REFRESH)	t _{CHR}	10		10		10		ns	1,19
$\overline{\text{OE}}$ Hold Time From $\overline{\text{WE}}$ During Read-Modify-Write Cycle	t _{OEH}	6		10		15		ns	16
$\overline{\text{OE}}$ Low to $\overline{\text{CAS}}$ High Setup Time	t _{OES}	5		5		5		ns	
$\overline{\text{OE}}$ High Hold Time From $\overline{\text{CAS}}$ High	t _{OEHC}	3		5		10		ns	
$\overline{\text{OE}}$ High Pulse Width	t _{OEP}	2		5		10		ns	
$\overline{\text{OE}}$ Setup Prior to $\overline{\text{CAS}}$ During Hidden Refresh Cycle	t _{ORD}	0		0		0		ns	
Last $\overline{\text{CAS}}$ Going Low to First $\overline{\text{CAS}}$ Returning High	t _{CLCH}	6		10		10		ns	21
Data Output Hold After $\overline{\text{CAS}}$ Returning Low	t _{COH}	4		5		5		ns	
Output Disable Delay From $\overline{\text{WE}}$	t _{WHZ}	3	7	3	10	3	15	ns	

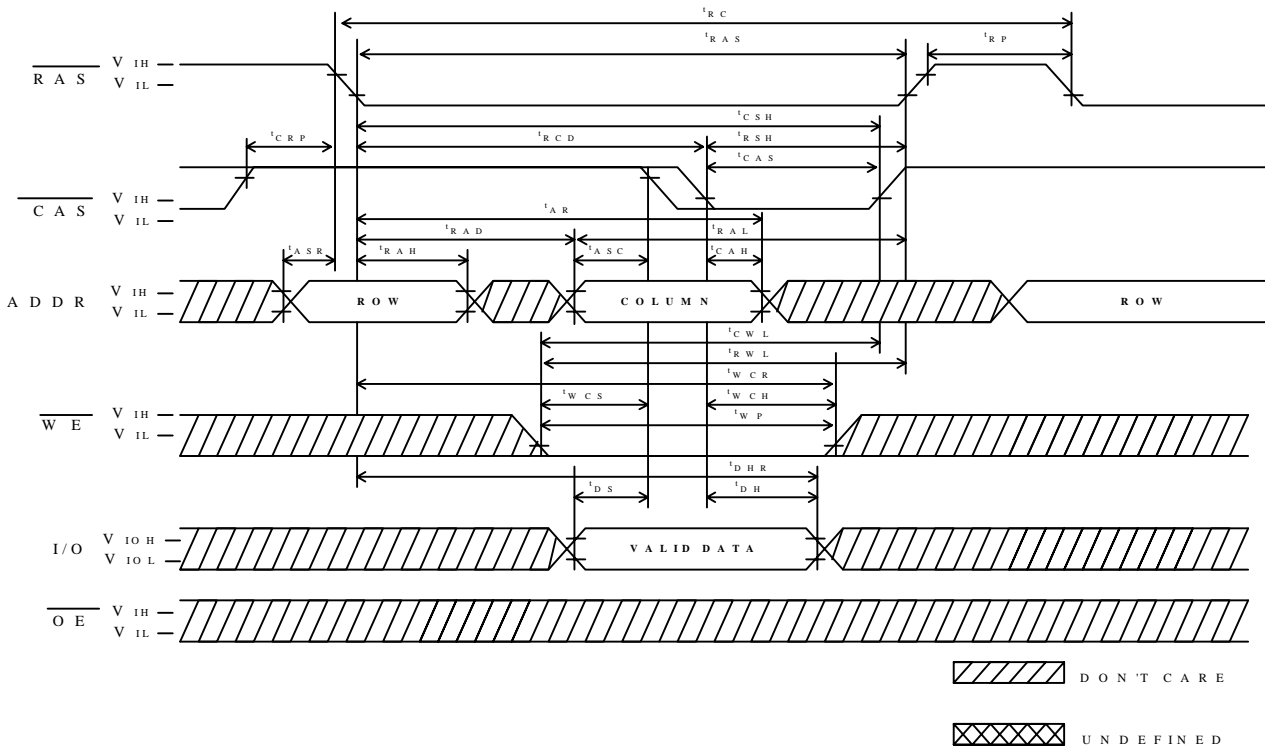
Notes:



1. Enables on-chip refresh and address counters.
2. $V_{IH}(2.4V)$ and $V_{IL}(0.8V)$ are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (2.4V) and V_{IL} (0.8V).
3. In addition to meet the transition rate specification, all input signals must transit between V_{IH} and V_{IL} in a monotonic manner.
4. Assume that $t_{RCD} < t_{RCD(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assume that $t_{RCD} \geq t_{RCD(max)}$.
6. If \overline{CAS} is low at the falling edge of \overline{RAS} , data-out will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, \overline{CAS} and \overline{RAS} must be pulsed high.
7. Operation within the $t_{RCD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, access time is controlled by t_{CAC} .
8. Operation within the t_{RAD} limit ensures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, access time is controlled by t_{AA} .
9. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
10. $t_{OFF1(max)}$ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL} .
11. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If $t_{WCS} \geq t_{WCS(min)}$, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CWD} \geq t_{CWD(min)}$, the cycle is READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until \overline{CAS} and \overline{RAS} or \overline{OE} go back to V_{IH}) is indeterminate. \overline{OE} held high and \overline{WE} taken low after \overline{CAS} goes low result in a LATE WRITE (\overline{OE} - controlled) cycle.
12. These parameters are referenced to \overline{CAS} leading edge in EARLY WRITE cycles and \overline{WE} leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
13. During a READ cycle, if \overline{OE} is low then taken HIGH before \overline{CAS} goes high, I/O goes open, if \overline{OE} is tied permanently low, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
14. An initial pause of 100ms is required after power-up followed by eight \overline{RAS} refresh cycles (\overline{RAS} only or CBR) before proper device operation is assured. The eight \overline{RAS} cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
15. WRITE command is defined as \overline{WE} going low.
16. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OFF2} and t_{OEH} met (\overline{OE} high during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycles.
17. The I/Os open during READ cycles once t_{OFF1} or t_{OFF2} occur.
18. The first \overline{CAS} edge to transition low.
19. The last \overline{CAS} edge to transition high.
20. Output parameter (I/O) is referenced to corresponding \overline{CAS} input, IO1~8 by \overline{CASL} and IO9~16 by \overline{CASH} .
21. Last falling \overline{CAS} edge to first rising \overline{CAS} edge.
22. Last rising \overline{CAS} edge to next cycle's last rising \overline{CAS} edge.
23. Last rising \overline{CAS} edge to first falling \overline{CAS} edge.
24. First IOs controlled by the first \overline{CAS} to go low.
25. Last IOs controlled by the last \overline{CAS} to go high.
26. Each \overline{CAS} must meet minimum pulse width.
27. Last \overline{CAS} to go low.
28. All IOs controlled, regardless \overline{CASL} and \overline{CASH} .
29. Data outputs are measured with a load of 50pF. The output reference levels are $V_{OH}/V_{OL} = 2.0V/0.8V$; The input levels are $V_{IH}/V_{IL} = 3.0V/0V$.

READ CYCLE



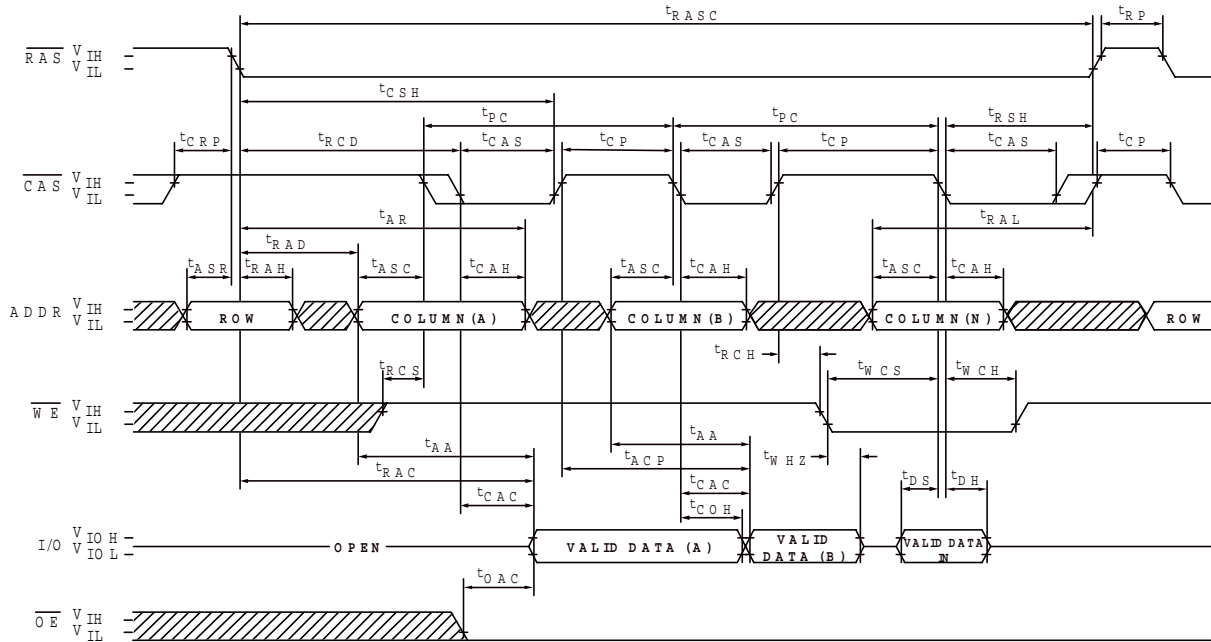
EARLY WRITE CYCLE



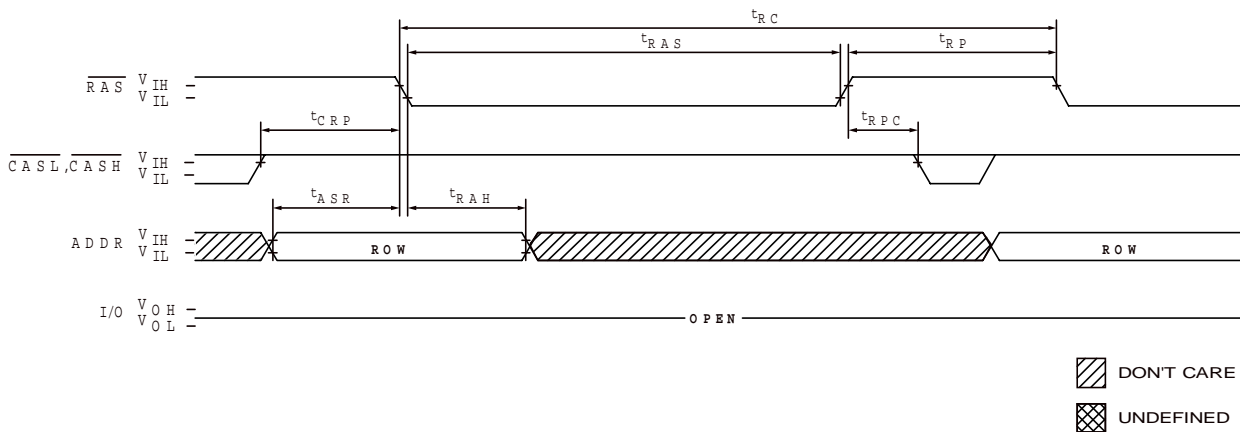
 DONT CARE
 UNDEFINED

Note: 1. t_{OFF1} is referenced from the rising edge of \overline{RAS} or \overline{CAS} , whichever occurs last.

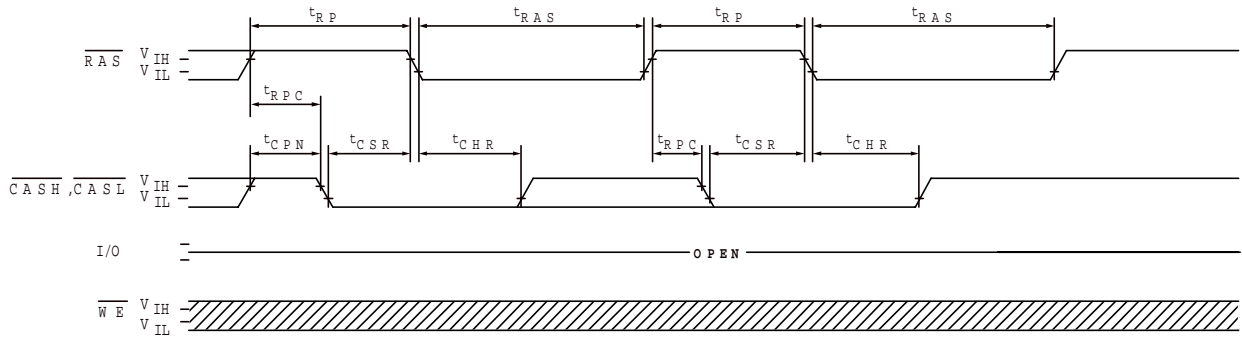
EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



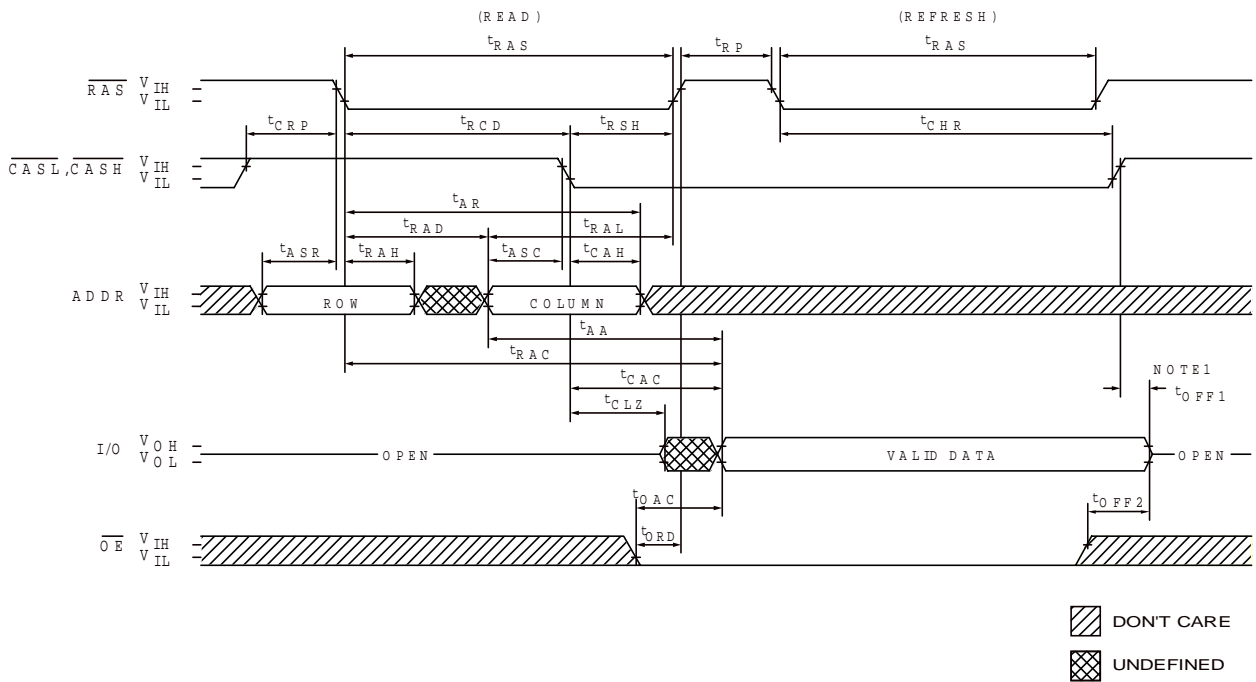
RAS ONLY REFRESH CYCLE
(ADDR=A0-A8 ; OE, WE =DON'T CARE)



CBR REFRESH CYCLE
(A0-A8 ; \overline{OE} =DON'T CARE)

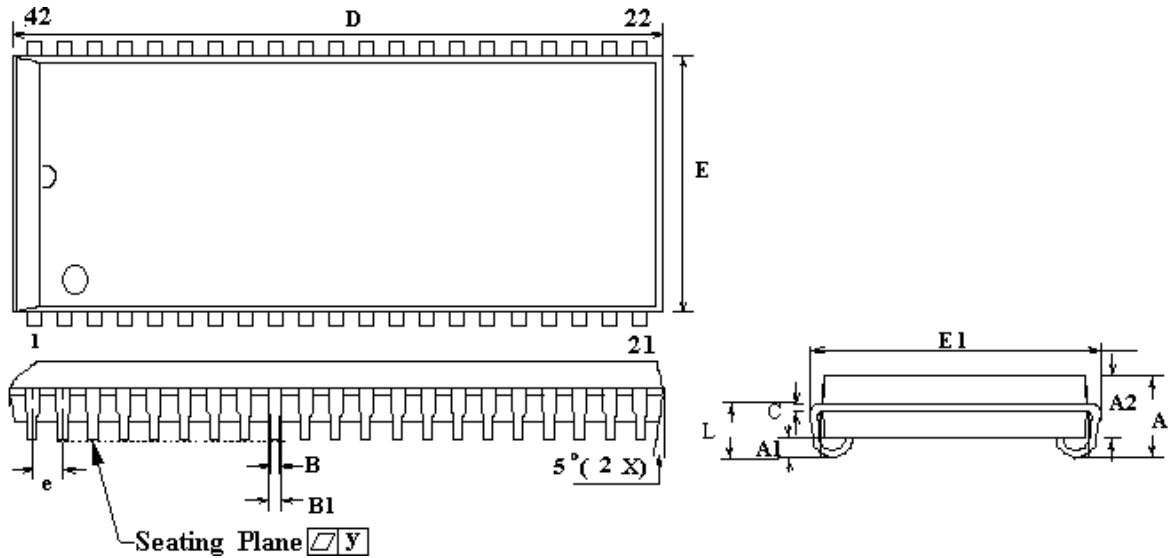


HIDDEN REFRESH CYCLE
(\overline{WE} =HIGH ; \overline{OE} =LOW)



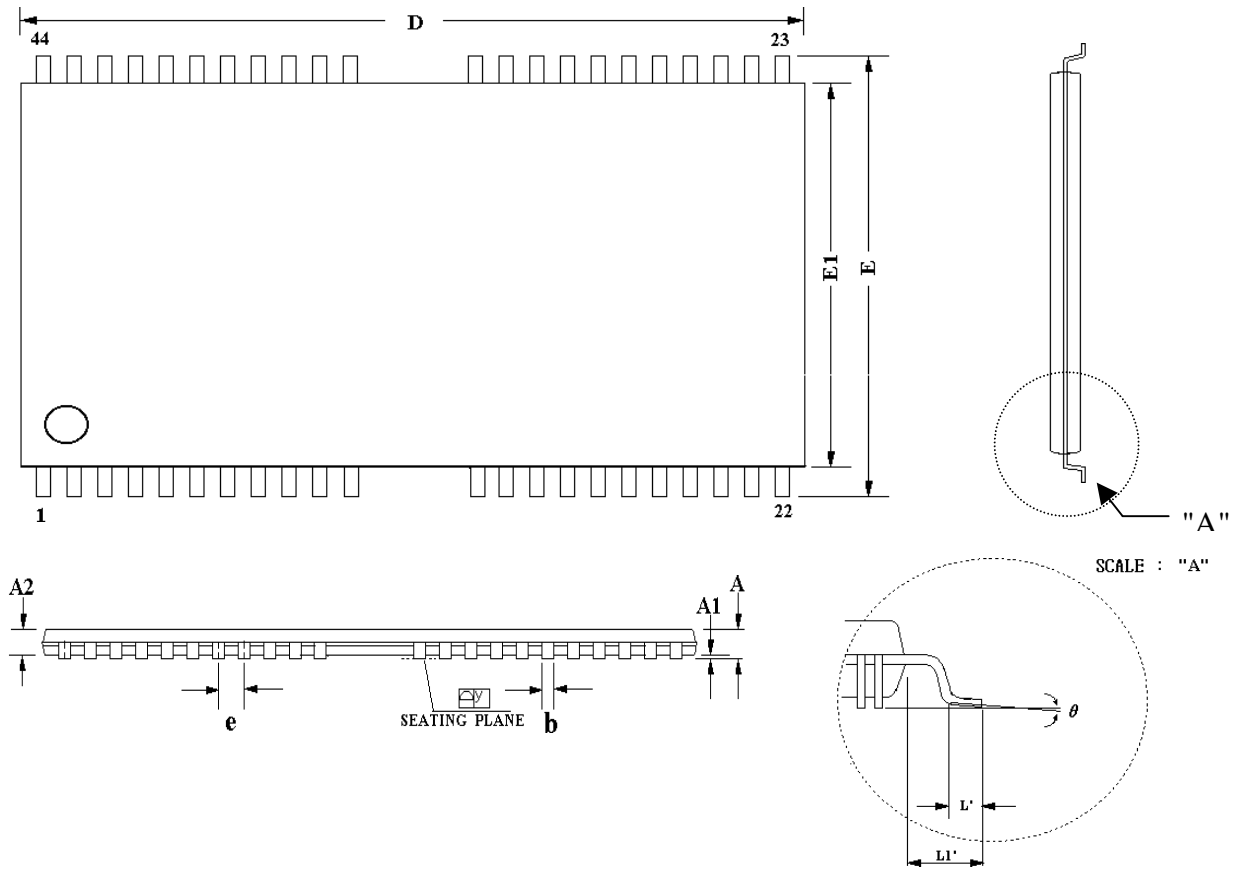
Note: 1. t_{OFF1} is referenced from the rising edge of \overline{RAS} or \overline{CAS} , whichever occurs last.

PACKAGE DIMENSIONS
42-LEAD SOJ DRAM (400 mil)



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.128~0.148	3.251~3.759
A1	0.025(MIN)	0.635(MIN)
A2	0.105~0.115	2.657~2.920
B	0.026~0.032	0.660~0.813
b	0.015~0.020	0.381~0.508
c	0.007~0.013	0.178~0.330
D	1.070~1.080	27.178~27.432
E	0.395~0.405	10.033~10.287
e	0.050	1.270
E1	0.435~0.445	11.049~11.303
L	0.082(MIN)	2.083(MIN)
y	0.004(MAX)	0.102(MAX)

PACKAGE DIMENSIONS
44/50L LEAD TSOPII DRAM (400 mil)



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.047	1.200(MAX)
A1	0.002~0.006	0.050~0.150
A2	0.037~0.041	0.950~1.050
b	0.012~0.018	0.300~0.450
c	0.005~0.008	0.120~0.210
D	0.820~0.830	20.820~21.080
E	0.455~0.471	11.560~11.960
e	0.031	0.800
E1	0.395~0.405	10.030~10.290
L	0.016~0.024	0.400~0.600
L1	0.031	0.800
θ	0°~5°	0°~5°