


### Description

The MK74CB214 Buffalo™ is a monolithic CMOS high speed clock driver which is ideal for Pentium™, 486, and RISC processor systems. It consists of two identical single input to seven low-skew output, non-inverting clock drivers. When combined with MicroClock's MK14xx series of low jitter clock synthesizers, the two chips form an unequalled high performance clocking scheme for new processors. This is the only solution on the market that meets Intel's specs for skew *and* jitter. Many new Pentium systems require up to seven outputs each of two low-skew clocks. This monolithic solution eliminates any concern for part-to-part skew matching. The MK74CB214 is packaged in the tiny 20 pin SSOP, which uses the same board space as the narrow 14 pin SOIC. An added feature of the chip is the ability to produce both 3.3V and 5V amplitude clocks by connecting different voltages to VDDA and VDDDB. See MAN03 for dual voltage operation.

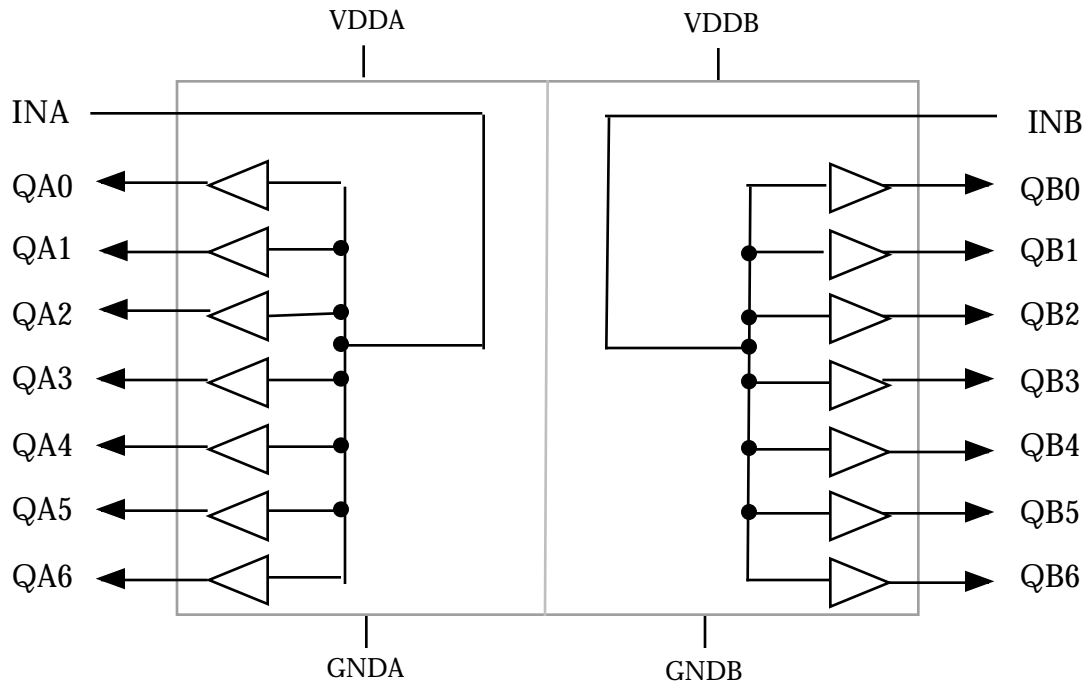
### Features

- Tiny 20 pin SSOP (150 mil) package 
- Dual one input to seven output clock drivers
- Outputs are skew matched to within 250ps
- A outputs and B outputs matched to 500ps
- 3.3V±10% and/or 5V±10% supply voltage
- Each set of seven clock drivers can run from different supply voltages, making it possible to have 3.3V and 5V amplitude clock outputs from the same chip
- Clock speeds up to 66.67 MHz

### Family of MicroClock Parts

The MK74CB214 Buffalo™ is designed to be used with MicroClock's clock synthesizer devices, which will produce the CPU, memory, and local bus clocks. The inputs of the Buffalo are matched to the outputs of MicroClock clock synthesizers. Consult MicroClock for applications support.

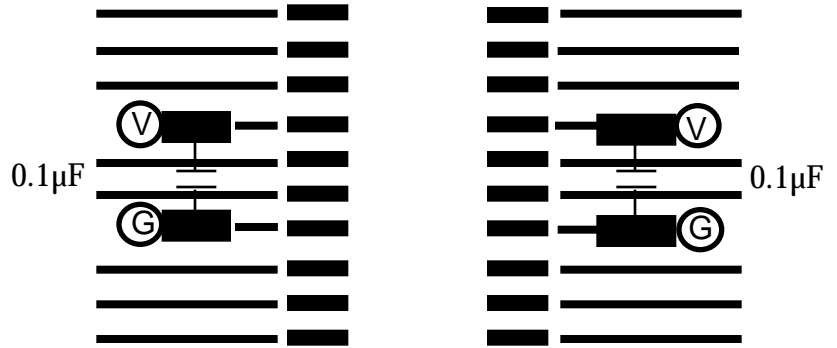
### Block Diagram



### Pin Assignment

INA	1	20	INB
QA0	2	19	QB0
QA1	3	18	QB1
VDDA	4	17	VDDB
QA2	5	16	QB2
QA3	6	15	QB3
GNDA	7	14	GNDB
QA4	8	13	QB4
QA5	9	12	QB5
QA6	10	11	QB6

### Suggested Layout



For simplicity, terminating resistors (if needed) are not shown for the outputs, but should be placed as close to the device as possible. It is most critical to have the 0.1µF decoupling capacitors closest.

V = connect to VDD     
 G = connect to GND

### Pin Descriptions

Number	Name	Type	Description
1	INA	I	Clock input for seven A outputs.
2, 3	QA0, QA1	O	Clock A outputs.
4	VDDA	P	Power supply for seven A buffers. Connect to +3.3V or +5V. Clock amplitude will match.
5, 6	QA2, QA3	O	Clock A outputs.
7	GNDA	P	Connect to ground.
8, 9, 10	QA4, QA5, QA6	O	Clock A outputs.
11, 12, 13	QB6, QB5, QB4	O	Clock B outputs.
14	GNDB	P	Connect to ground.
15, 16	QB3, QB2	O	Clock B outputs.
17	VDDB	P	Power supply for seven B buffers. Connect to +3.3V or +5V. Clock amplitude will match.
18, 19	QB1, QB0	O	Clock B outputs.
20	INB	I	Clock input for seven B outputs.

Type: I = Input, O = output, P = power supply connection

### Electrical Specifications

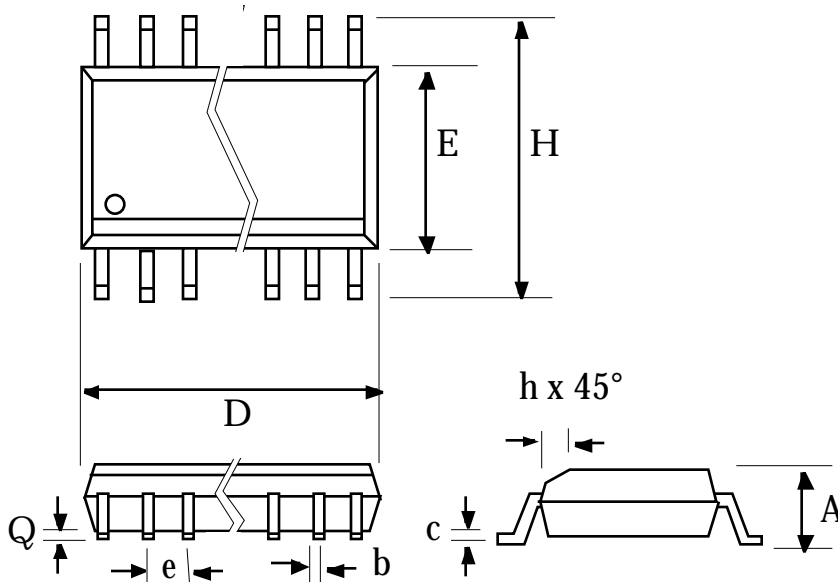
Parameter	Conditions	Minimum	Typical	Maximum	Units
<b>ABSOLUTE MAXIMUM RATINGS (Note 1)</b>					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	0.5		VDD+0.5	V
Clock Outputs	Referenced to GND	0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage Temperature		-65		150	°C
<b>DC CHARACTERISTICS (VDD = 5V unless noted)</b>					
Operating Voltage, VDD		3.0		5.5	V
Input High Voltage, VIH (INA, INB pins)		VDD-1	VDD/2		V
Input Low Voltage, VIL (INA, INB pins)			VDD/2	1	V
Output High Voltage, 3.3V and 5V	IOH=-8mA	VDD-0.4			V
Output High Voltage, 3.3V and 5V	IOH=-12mA	2.4			V
Output Low Voltage, 3.3V and 5V	IOL=12mA			0.8	V
Operating Supply Current, IDD, at 66.6MHz	No Load		20		mA
Short Circuit Current	Each output		±70		mA
Short Circuit Current at 3.3V	Each output		±35		mA
Input Capacitance			7		pF
<b>AC CHARACTERISTICS (VDD = 5V unless noted)</b>					
Input Clock Frequency				67	MHz
Propagation Delay with load=10pF		2	3.5	5	ns
Propagation Delay with load=10pF	At VDD=3.3V	2.5	4.5	6.5	ns
Output Clock Rise Time, 3.3V and 5V	0.8 to 2.0V			1.5	ns
Output Clock Fall Time, 3.3V and 5V	2.0 to 0.8V			1.5	ns
Output Clock Rising Edge Skew, 3.3V and 5V	At VDD/2. Note 2		50	250	ps
Output Clock A to B Skew, 3.3V and 5V	At VDD/2. Note 3		100	500	ps
Maximum load per output pin	At 66.66 MHz			25	pF
Maximum load per side of 7 outputs	Note 4			105	pF

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. Between any two A outputs, or any two B outputs, with equal loading.
3. Between any clock A output and any clock B output with INA connected to INB. With VDDA=VDDDB and equal loading. Combined with the 250ps uncertainty of MicroClock's Clock Synthesizers, this adds to a 750ps total.
4. This is the load sum of all A outputs, or all B outputs, at 66.66MHz. The formula for per side load is  $C_L (F) = \frac{7 \times 10^{-3}}{f \text{ (in Hz)}}$

### Package Outline and Package Dimensions

### 20 pin SSOP



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.061	0.068	1.55	1.73
b	0.008	0.012	0.203	0.305
c	0.007	0.010	0.191	0.254
D	0.337	0.344	8.560	8.740
E	0.150	0.160	3.810	4.064
H	0.230	0.245	5.842	6.223
e	.025 BSC		0.64 BSC	
h		0.016		0.406
Q	0.005	0.01	0.127	0.254

### Ordering Information

Part/Order Number	Marking	Package	Temperature
MK74CB214R	74CB214R	20 pin SSOP	0-70°C
MK74CB214RTR	74CB214R	Add Tape & Reel	0-70°C

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