Product Preview

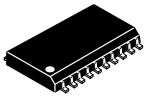
1:4 ÷1/÷2 ECL/PECL Clock Fanout Buffer

MC100LVEL37

The MC100LVEL37 is a fully differential 1:4 fanout buffer. The device offers two outputs at ÷1 of the input frequency, and two outputs at ÷2 of the input frequency. The Low Output–Output Skew of the device makes it ideal for distributing1x and 1/2x frequency synchronous signals.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to V_{EE}, The D input will bias around $V_{CC}/2$ and the Q output will go LOW.

- Differential Inputs and Outputs
- 20–Lead SOIC Packaging
- 700ps Typical Propagation Delays
- 50ps Output–Output Skews
- Low Voltage 100K ECL
- >2000V ESD Protection



DW SUFFIX
20–LEAD PLASTIC SOIC WIDE PACKAGE
CASE 751D–04

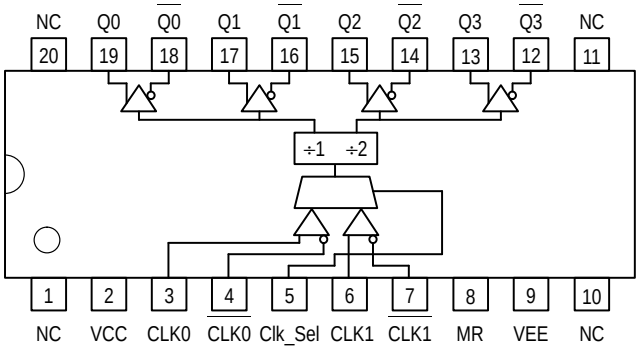


Figure 1. 20–Lead Pinout (Top View)

PIN NAMES

Pins	Function
Qna, Qna	Differential Clock Outputs
CLKn, CLKn	Differential Clock Inputs
Clk_Sel	Input Clock Selection '0' Selects CLK0; '1' Selects CLK1
MR	Asynchronous Master Reset '1' Resets Dividers

MC100LVEL37
DC CHARACTERISTICS (V_{EE} = –3.0V to –3.8V; V_{CC} = GND)

		–40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		38			38			38			38		mA
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{INL}	Input LOW Current CLKn CLKn	0.5 –300			0.5 –300			0.5 –300			0.5 –300			µA

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

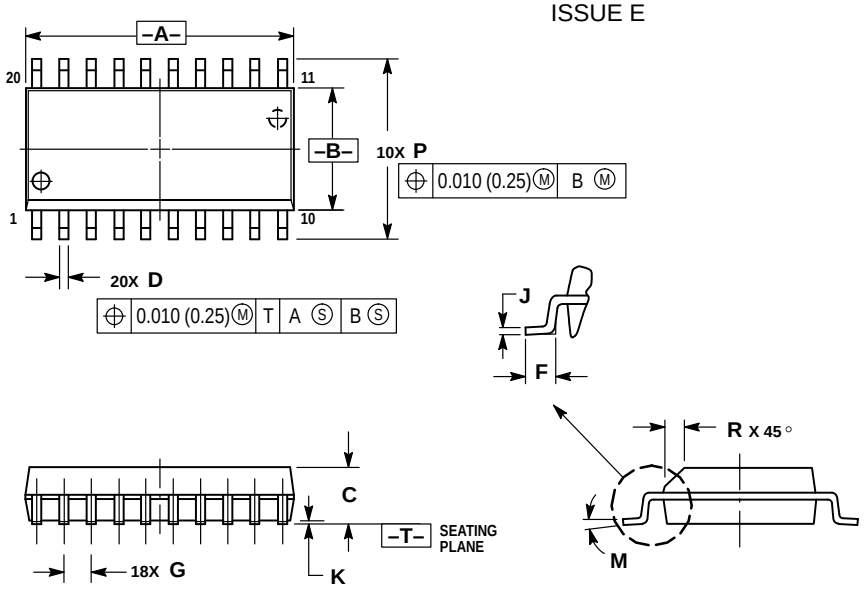
MC100LVEL37
AC CHARACTERISTICS (V_{EE} = –3.0V to –3.8V; V_{CC} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CLK}\rightarrow Q/\overline{Q}$ Clk_Sel→Q MR→Q		 700 800 800			 700 800 800			 700 800 800			 700 800 800		ps
$t_{sk(O)}$	Output–Output Skew			50			50			50			50	ps
$t_{sk(DC)}$	Duty Cycle Skew $\lvert t_{PLH} - t_{PHL} \rvert$			 50			 50			 50			 50	ps
V_{PP}	Minimum Input Swing (Note 1.)	150		1000	150		1000	150		1000	150		1000	mV
V_{CMR}	Common Mode Range (Note 2.) V_{PP} < 500mV $V_{PP} \geq$ 500mV	 –2.0 –1.8		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	230		500	ps

1. Minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR}(min) will be fixed at 3.3V – $|V_{CMR}(min)|$.

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC WIDE PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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