

SANYO

No. ※ 5010

LC895170W**CD-ROM Error Correction LSI**

Preliminary

Overview

The LC895170W is an upwardly compatible version of the LC89517K that supports a larger external buffer RAM capacity and is provided in a more compact package.

Functions

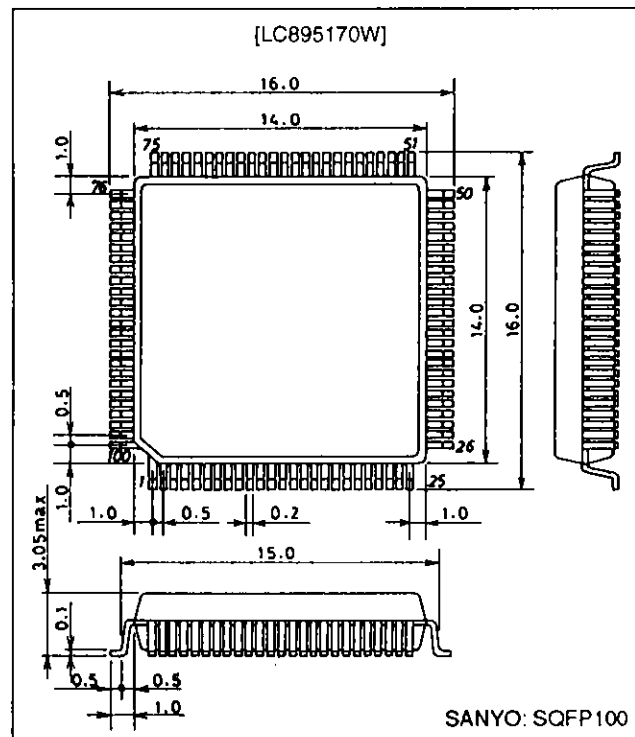
- CD-ROM ECC function, subcode read function, AT interface

Features

- Support for double-speed operation at a 16.9344 MHz operating frequency
Either SRAM (120 ns), DRAM (80 ns), or PSRAM (85 ns) can be used.
- Support for quad-speed operation at a 33.8688 MHz operating frequency
SRAM (70 ns) must be used.
- On-chip 12-byte output FIFO for sub-CPU to host computer transfers
- On-chip 12-byte input FIFO for host computer to sub-CPU transfers
- Subcode data can be written to SRAM by connecting the CD-DSP SUB-CODE pin and the sub-CPU can read the subcode values.
- The sub-CPU can access buffer RAM through the LC895170W.
- On-chip data transfer function for buffer RAM to buffer RAM transfers
- Pseudo-SRAM (up to 128 kwords × 8 bits × 1) can be used.
- DRAM (256 kwords × 4 bits × 2, or 1 Mwords × 4 bits × 2) can be used.
- Transfer speed: 2.8 Mbytes/s
(The transfer speed depends on the operating frequency.)
- Operating frequencies: 16.9344 MHz (double speed) or 33.8688 MHz (quad speed)

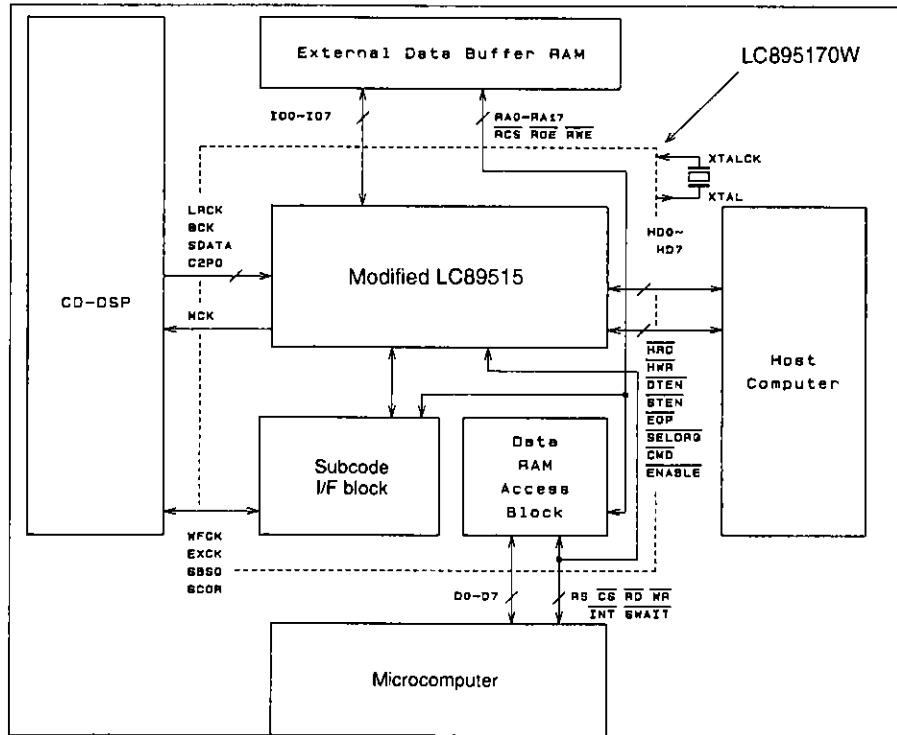
Package Dimensions

unit: mm

3181-SQFP100

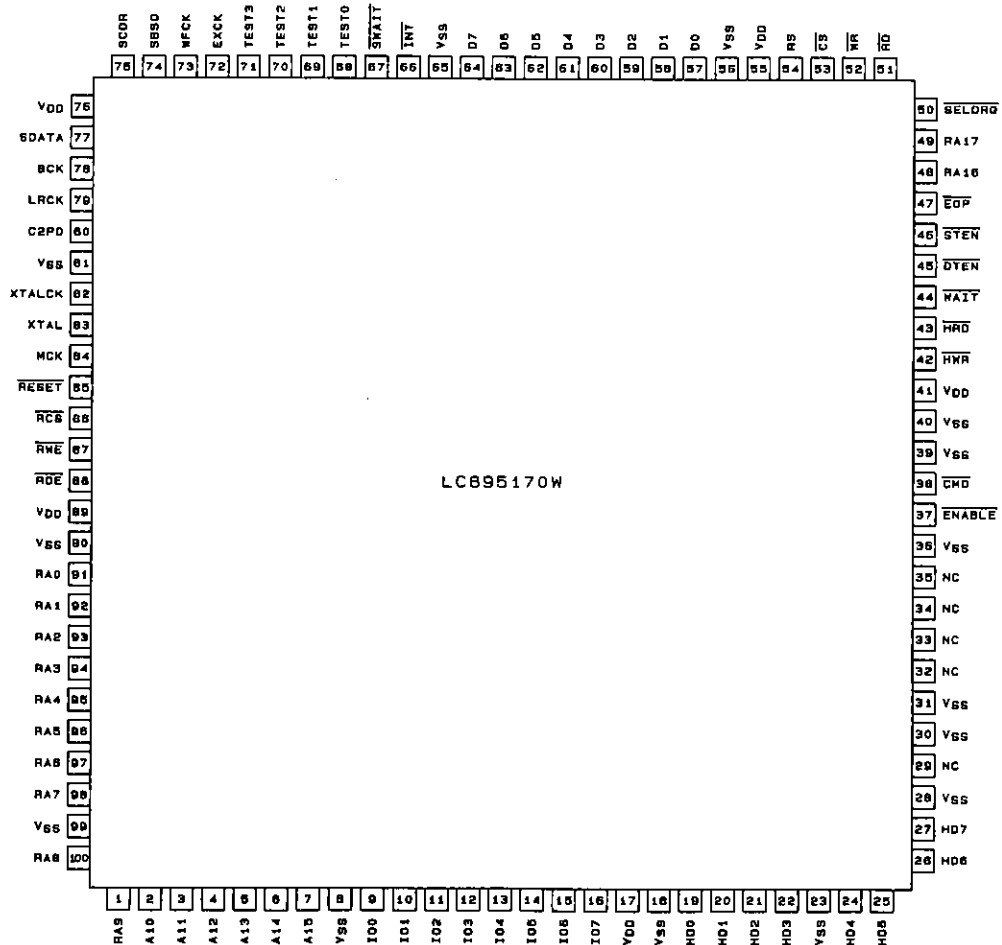
LC895170W

Block Diagram



A03114

Pin Assignment



A03113

Top View

LC895170W

Pin Functions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Unconnected pin

| Pin No. | Pin | Type | Function |
|---------|---------------------|------|--|
| 1 | RA9 | O | Data buffer RAM address signal outputs |
| 2 | RA10 | O | |
| 3 | RA11 | O | |
| 4 | RA12 | O | |
| 5 | RA13 | O | |
| 6 | RA14 | O | |
| 7 | RA15 | O | |
| 8 | V _{SS} | P | |
| 9 | IO0 | B | Data buffer RAM data signal outputs Pull-up resistors on chip |
| 10 | IO1 | B | |
| 11 | IO2 | B | |
| 12 | IO3 | B | |
| 13 | IO4 | B | |
| 14 | IO5 | B | |
| 15 | IO6 | B | |
| 16 | IO7 | B | |
| 17 | V _{DD} | P | |
| 18 | V _{SS} | P | |
| 19 | HD0 | B | Host data signals Pull-up resistors on chip |
| 20 | HD1 | B | |
| 21 | HD2 | B | |
| 22 | HD3 | B | |
| 23 | V _{SS} | P | |
| 24 | HD4 | B | Host data signals Pull-up resistors on chip |
| 25 | HD5 | B | |
| 26 | HD6 | B | |
| 27 | HD7 | B | |
| 28 | V _{SS} | P | |
| 29 | | NC | |
| 30 | V _{SS} | P | |
| 31 | V _{SS} | P | |
| 32 | | NC | |
| 33 | | NC | |
| 34 | | NC | |
| 35 | | NC | |
| 36 | V _{SS} | P | |
| 37 | ENABLE | I | Host chip select signal input |
| 38 | CMD | I | Host command/data selection signal input |
| 39 | V _{SS} | P | |
| 40 | V _{SS} | P | |
| 41 | V _{DD} | P | |
| 42 | HWR | I | Host data write signal input |
| 43 | HRD | I | Host data read signal input |
| 44 | WAIT | O | Host wait signal. Can be switched to function as a DRQ signal. |
| 45 | DTEN | O | Data enable signal output |
| 46 | STEN | O | Status enable signal output |
| 47 | EOP | O | End of process signal output. Used during DMA data transfers. |
| 48 | RA16 | O | Data buffer RAM address signal outputs |
| 49 | RA17 | O | |
| 50 | SELD \overline RQ | I | Host data transfer mode selection signal input |

Continued on next page.

LC895170W

Continued from preceding page.

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Unconnected pin

| Pin No. | Pin | Type | Function |
|---------|--------------------|------|--|
| 51 | \overline{RD} | I | Microprocessor data read signal input |
| 52 | \overline{WR} | I | Microprocessor data write signal input |
| 53 | \overline{CS} | I | Chip select signal input (from microprocessor) |
| 54 | RS | I | Register selection signal |
| 55 | V _{DD} | P | |
| 56 | V _{SS} | P | |
| 57 | D0 | B | Microprocessor data signals Pull-up resistors on chip |
| 58 | D1 | B | |
| 59 | D2 | B | |
| 60 | D3 | B | |
| 61 | D4 | B | |
| 62 | D5 | B | |
| 63 | D6 | B | |
| 64 | D7 | B | |
| 65 | V _{SS} | P | |
| 66 | \overline{INT} | O | Interrupt request signal output (to the microprocessor) Open-drain output with on-chip pull-up resistor |
| 67 | \overline{SWAIT} | O | Sub-CPU wait signal |
| 68 | TEST0 | I | Test inputs should be tied low in normal operation. |
| 69 | TEST1 | I | |
| 70 | TEST2 | I | |
| 71 | TEST3 | I | |
| 72 | EXCK | O | Subcode I/O pins |
| 73 | WFCK | I | |
| 74 | SBSO | I | |
| 75 | SCOR | I | |
| 76 | V _{DD} | P | |
| 77 | SDATA | I | Serial data input |
| 78 | BCK | I | Serial data input clock |
| 79 | LRCK | I | 44.1 kHz strobe signal input |
| 80 | C2PO | I | C2 pointer input |
| 81 | V _{SS} | P | |
| 82 | XTALCK | I | Crystal oscillator circuit input |
| 83 | XTAL | O | Crystal oscillator circuit output |
| 84 | MCK | O | XTALCK-divided-by-2 output |
| 85 | \overline{RESET} | I | Reset. The LC895170W is reset on a low level input. |
| 86 | \overline{RCS} | O | RAM chip select |
| 87 | \overline{RWE} | O | RAM data write signal |
| 88 | \overline{ROE} | O | RAM data read signal |
| 89 | V _{DD} | P | |
| 90 | V _{SS} | P | |
| 91 | RA0 | O | Data buffer RAM address signals output. |
| 92 | RA1 | O | |
| 93 | RA2 | O | |
| 94 | RA3 | O | |
| 95 | RA4 | O | |
| 96 | RA5 | O | |
| 97 | RA6 | O | |
| 98 | RA7 | O | |
| 99 | V _{SS} | P | |
| 100 | RA8 | O | Data buffer RAM address signal output. |

Specifications

Absolute Maximum Ratings at $V_{SS} = 0$ V

| Parameter | Symbol | Conditions | Ratings | Unit |
|--|--------------|-----------------------------|------------------------|------------------|
| Maximum supply voltage | V_{DD} max | $T_a = 25^\circ\text{C}$ | -0.3 to +7.0 | V |
| I/O voltages | $V_{I/O}$ | $T_a = 25^\circ\text{C}$ | -0.3 to $V_{DD} + 0.3$ | V |
| Allowable power dissipation | P_d max | $T_a \leq 70^\circ\text{C}$ | 350 | mW |
| Operating temperature | T_{opr} | | -30 to +70 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +125 | $^\circ\text{C}$ |
| Soldering thermal stress limit (pins only) | | 10 seconds | 260 | $^\circ\text{C}$ |

Allowable Operating Ranges at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0$ V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---------------------|----------|------------|-----|-----|----------|------|
| Supply voltage | V_{DD} | | 4.5 | 5.0 | 5.5 | V |
| Input voltage range | V_{IN} | | 0 | | V_{DD} | V |

DC Characteristics at $T_a = -30$ to $+70^\circ\text{C}$, $V_{SS} = 0$ V, $V_{DD} = 4.5$ to 5.5 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---------------------------|-----------|---|-----|-----|-----|---------------|
| Input high level voltage | V_{IH1} | All input pins other than (1) and XTALCK | 2.2 | | | V |
| Input low level voltage | V_{IL1} | | | | 0.8 | V |
| Input high level voltage | V_{IH2} | RESET, all bus pins (HRD, HWR, ENABLE, CMD, RD, CS, WR, WFCK, SBSO, SCOR) (1) | 2.5 | | | V |
| Input low level voltage | V_{IL2} | | | | 0.6 | V |
| Output high level voltage | V_{OH1} | $I_{OH1} = -2$ mA: All output pins (including bus pins) other than (2) and XTALCK | 2.4 | | | V |
| Output low level voltage | V_{OL1} | $I_{OL1} = 2$ mA: All output pins (including bus pins) other than (2) and XTALCK | | | 0.4 | V |
| Output low level voltage | V_{OL2} | $I_{OL2} = 2$ mA: INT (on-chip pull-up resistor, open drain) (2) | | | 0.4 | V |
| Output high level voltage | V_{OH3} | $I_{OH3} = -6$ mA: HD0 to HD7 | 2.4 | | | V |
| Output low level voltage | V_{OL3} | $I_{OL3} = 6$ mA: HD0 to HD7 | | | 0.4 | V |
| Input leakage current | I_L | $V_I = V_{SS}$, V_{DD} : All input pins | -25 | | +25 | μA |
| Pull-up resistance | R_{UP} | All bus pins, INT | 40 | 80 | 160 | k Ω |

- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use;
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.