v00.0204

HMC311ST89

InGaP HBT GAIN BLOCK MMIC AMPLIFIER, DC - 6.0 GHz

Typical Applications

The HMC311ST89 is an ideal RF/IF gain block or LO buffer amplifier for:

- Cellular / PCS / 3G
- Fixed Wireless & WLAN
- CATV & Cable Modem
- Microwave Radio

Features

P1dB Output Power: +15.5 dBm

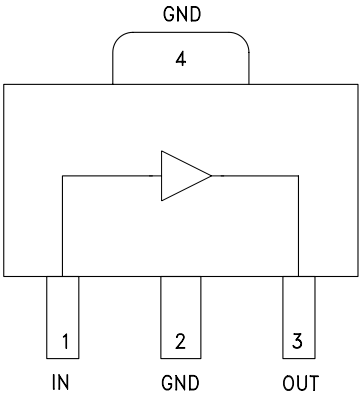
Output IP3: +31.5 dBm

Gain: 16 dB

50 Ohm I/O's

Industry Standard SOT89 Package

Functional Diagram



General Description

The HMC311ST89 is a GaAs InGaP Heterojunction Bipolar Transistor (HBT) Gain Block MMIC SMT DC to 6 GHz amplifier. Packaged in an industry standard SOT89, the amplifier can be used as either a cascadable 50 Ohm gain stage or to drive the LO of HMC mixers with up to +16.5 dBm output power. The HMC311ST89 offers 16 dB of gain and an output IP3 of +31.5 dBm while requiring only 54 mA from a +5V supply. The Darlington feedback pair used results in reduced sensitivity to normal process variations and yields excellent gain stability over temperature while requiring a minimal number of external bias components.

Electrical Specifications, Vs= 5.0 V, Rbias= 22 Ohm, T_A = +25° C

Parameter		Min.	Typ.	Max.	Units
Gain	DC - 1.0 GHz 1.0 - 4.0 GHz 4.0 - 6.0 GHz	14.0 13.0 12.5	16.0 15.0 14.5		dB dB dB
Gain Variation Over Temperature	DC - 2.0 GHz 2.0 - 4.0 GHz 4.0 - 6.0 GHz		0.004 0.007 0.012	0.007 0.012 0.016	dB/ °C dB/ °C dB/ °C
Return Loss Input / Output	DC - 2.0 GHz 2.0 - 5.0 GHz 5.0 - 6.0 GHz		8 7 8		dB dB dB
Reverse Isolation	DC - 6.0 GHz		20		dB
Output Power for 1 dB Compression (P1dB)	DC - 2.0 GHz 2.0 - 4.0 GHz 4.0 - 6.0 GHz	13.5 12.0 10.0	15.5 15.0 13.0		dBm dBm dBm
Output Third Order Intercept (IP3)	DC - 1.0 GHz 1.0 - 2.0 GHz 2.0 - 4.0 GHz 4.0 - 6.0 GHz		31.5 30 27 24		dBm dBm dBm dBm
Noise Figure	DC - 4.0 GHz 4.0 - 6.0 GHz		4.5 5		dB
Supply Current (Icq)			54		mA

Note: Data taken with broadband bias tee on device output.

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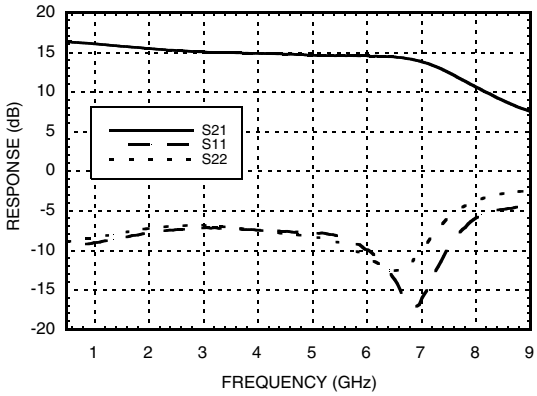
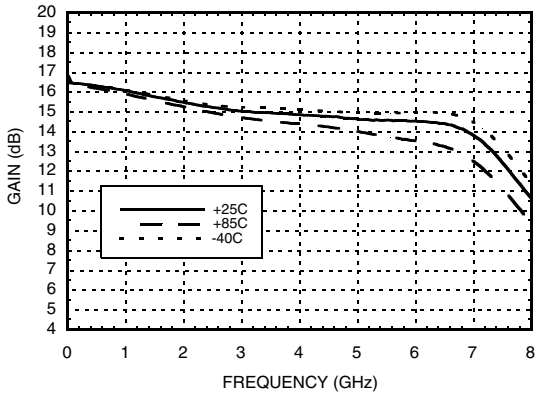
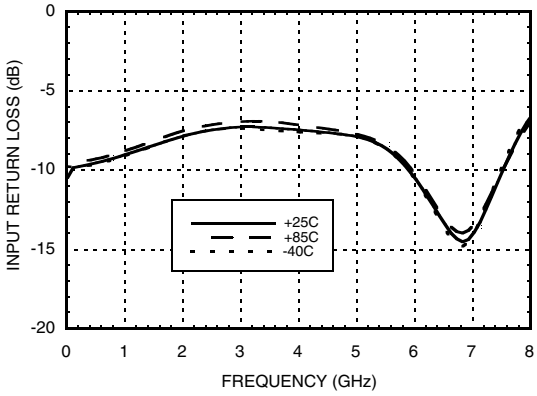
Broadband Gain & Return Loss



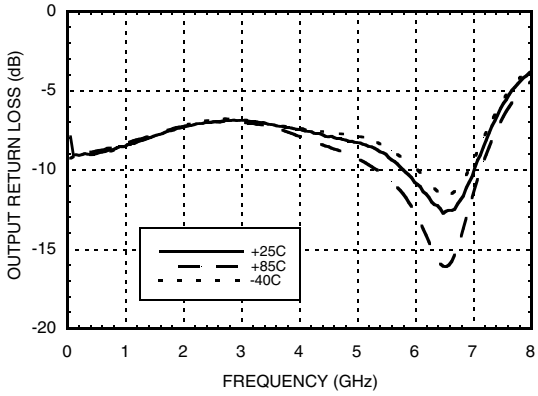
Gain vs. Temperature



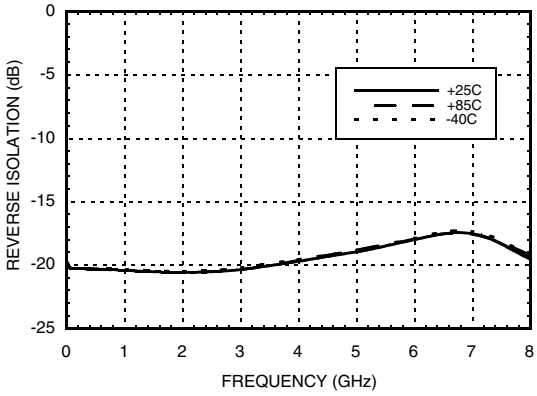
Input Return Loss vs. Temperature



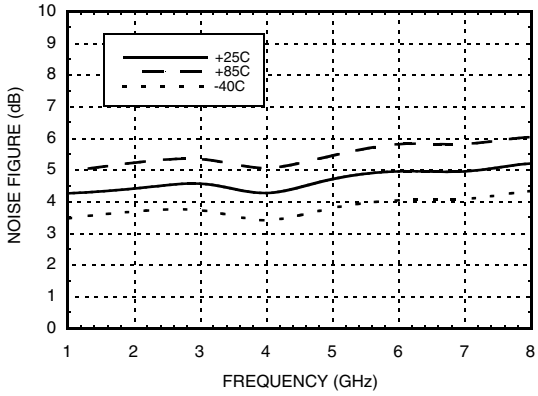
Output Return Loss vs. Temperature



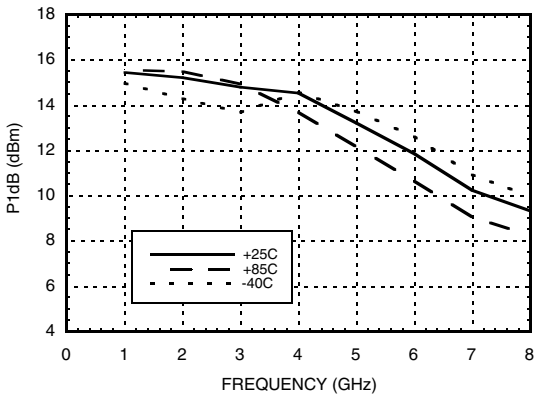
Reverse Isolation vs. Temperature



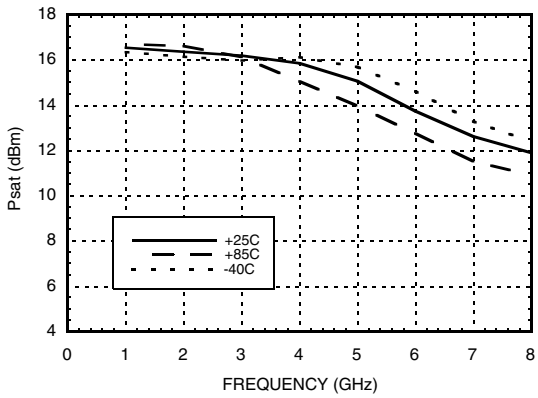
Noise Figure vs. Temperature



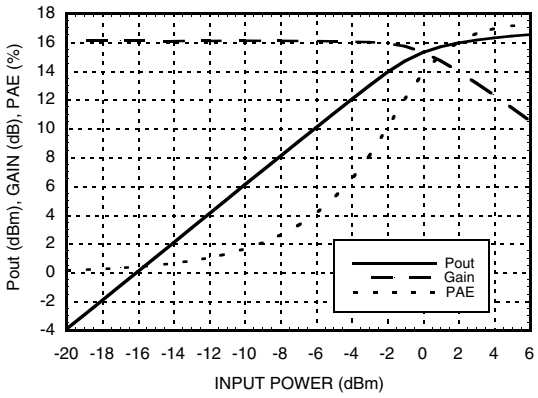
P1dB vs. Temperature



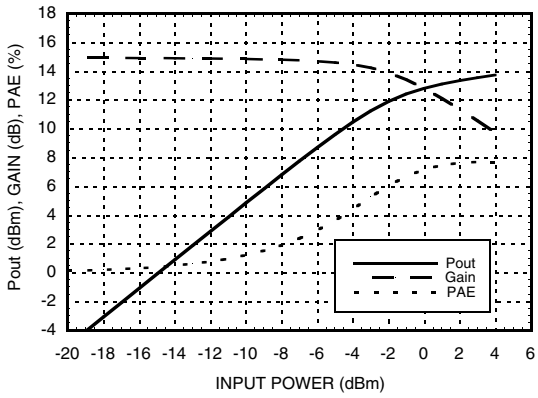
Psat vs. Temperature



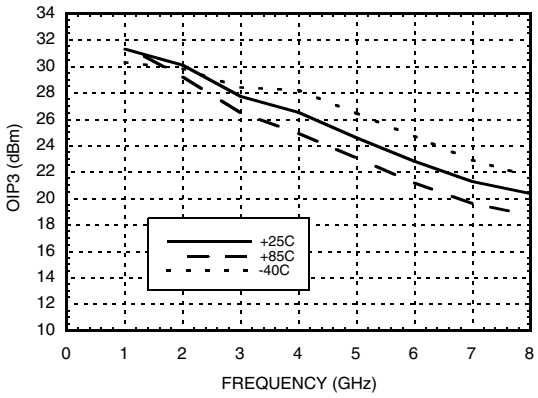
Power Compression @ 1 GHz



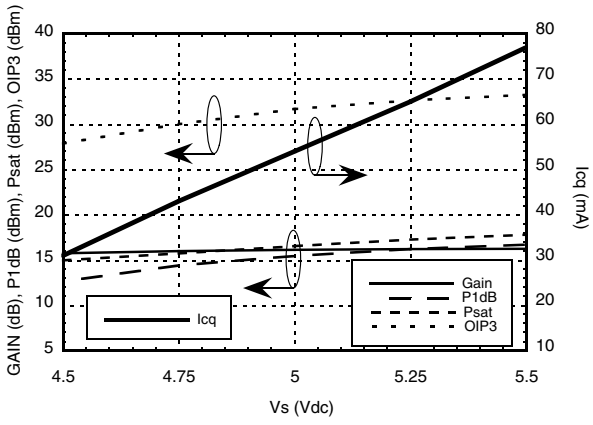
Power Compression @ 6 GHz



Output IP3 vs. Temperature



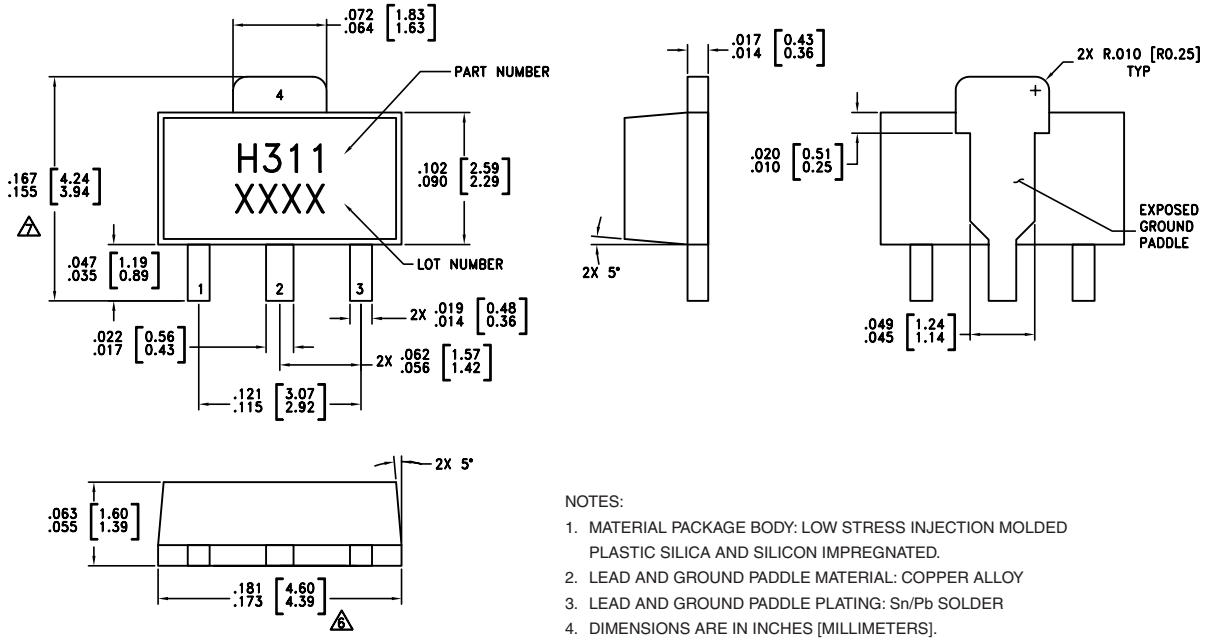
Gain, Power, OIP3 & Supply Current vs. Supply Voltage @ 1 GHz



Absolute Maximum Ratings

Collector Bias Voltage (Vcc)	+7 Volts
RF Input Power (RFin)(Vcc = +3.9 Vdc)	+10 dBm
Junction Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 5.21 mW/°C above 85 °C)	0.34 W
Thermal Resistance (junction to lead)	191 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

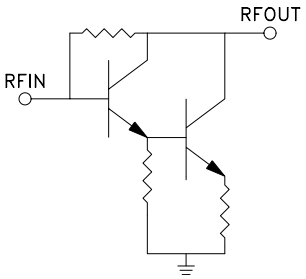
Outline Drawing



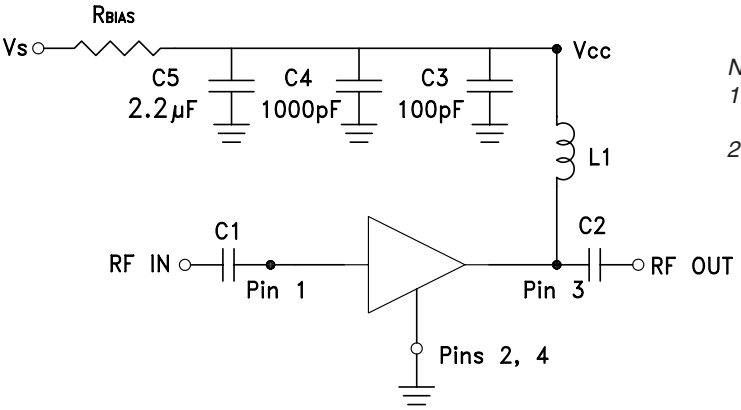
NOTES:

1. MATERIAL PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY
3. LEAD AND GROUND PADDLE PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
6. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	RFIN	This pin is DC coupled. An off chip DC blocking capacitor is required.	
3	RFOUT	RF output and DC Bias for the output stage.	
2, 4	GND	These pins and package bottom must be connected to RF/DC ground.	

Application Circuit



Note:

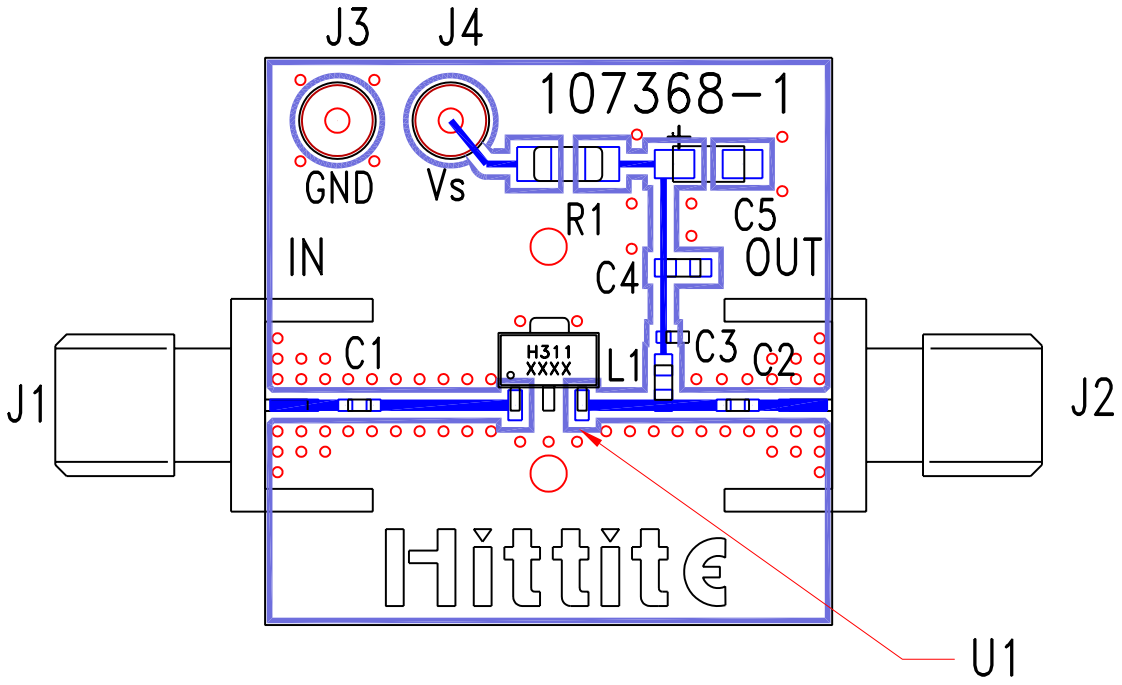
1. *Select Rbias to achieve Icq using equation below, Rbias ≥ 22 Ohm.*
2. *External blocking capacitors are required on RFIN and RFOUT.*

$$Icq = \frac{Vs - 3.9}{Rbias}$$

Recommended Component Values

Component	Frequency (MHz)							
	50	900	1900	2200	2400	3500	5200	5800
L1	270 nH	56 nH	18 nH	18 nH	15 nH	8.2 nH	3.3 nH	3.3 nH
C1, C2	0.01 µF	100 pF	100 pF	100 pF	100 pF	100 pF	100 pF	100 pF

Evaluation PCB



List of Materials for Evaluation PCB 108313*

Item	Description
J1 - J2	PC Mount SMA Connector
J3 - J4	DC Pin
C1, C2	Capacitor, 0402 Pkg.
C3	100 pF Capacitor, 0402 Pkg.
C4	1000 pF Capacitor, 0603 Pkg.
C5	2.2 µF Capacitor, Tantalum
R1	Resistor, 0805 Pkg.
L1	Inductor, 0603 Pkg.
U1	HMC311ST89
PCB**	107368 Evaluation PCB
** Circuit Board Material: Rogers 4350	

* Reference this number when ordering complete evaluation PCB.

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.