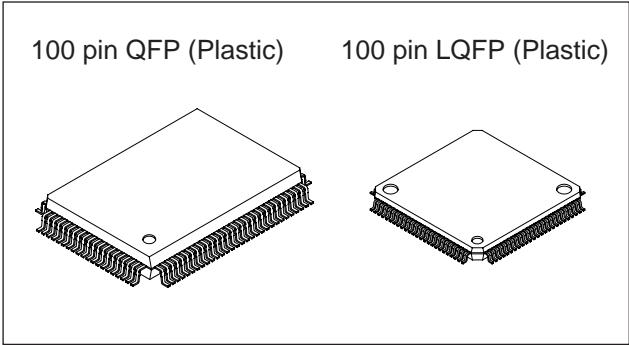


**CMOS 8-bit Single Chip Microcomputer**

**Description**

The CXP740056/740096/740010 is a CMOS 8-bit microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, capture timer/counter, remote control receive circuit, PWM output, and the like besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP740056/740096/740010 also provides the sleep/stop functions that enables lower power consumption.



**Structure**

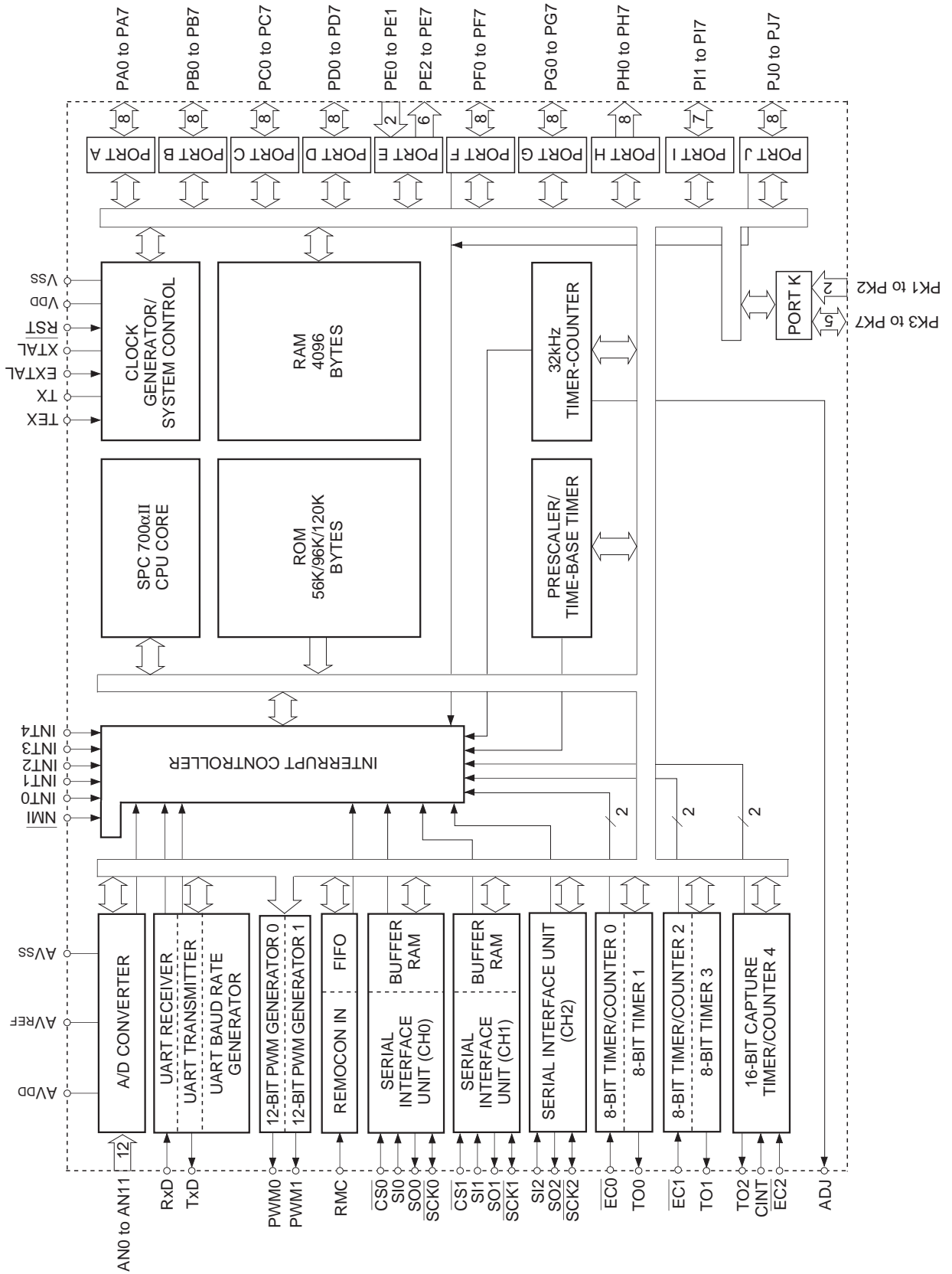
Silicon gate CMOS IC

**Features**

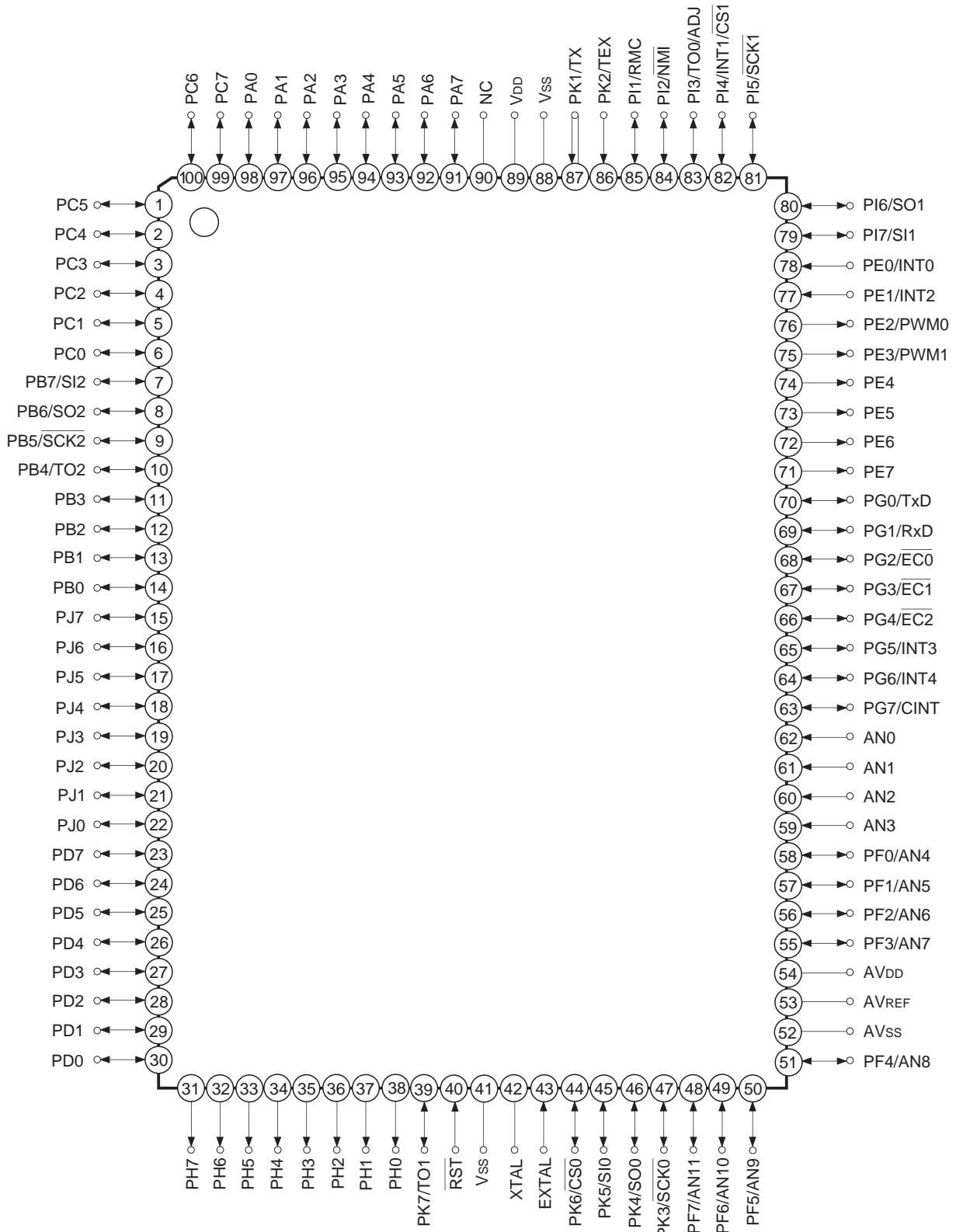
- A wide instruction set (211 instructions) which covers various types of data.
  - 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
  - 167ns at 24MHz operation (4.5 to 5.5V)
  - 333ns at 12MHz operation (2.7 to 5.5V)
  - 122µs at 32kHz operation (2.7 to 5.5V)
- Incorporated ROM capacity
  - 56K bytes (CXP740056)
  - 96K bytes (CXP740096)
  - 120K bytes (CXP740010)
- Incorporated RAM capacity
  - 4096 bytes
- Peripheral functions
  - A/D converter
    - 8 bits, 8 channels, successive approximation method (Conversion time 10.3µs at 24MHz)
  - Serial interface
    - Start-stop synchronization (UART), 1 channel
    - Incorporated buffer RAM (Auto transfer for 1 to 32 bytes), 2 channels
    - 8-bit clock synchronization (MSB/LSB first selectable), 1 channel
  - Timer
    - 8-bit timer 2 channels, 8-bit timer/counter 2 channels,
    - 19-bit time-base timer, 16-bit capture timer/counter
    - 32kHz timer/counter
  - Remote control receive circuit
    - Noise elimination circuit
    - 8-bit pulse measuring counter, 6-stage FIFO
  - PWM output
    - 12 bits, 2 channels
- Interruption
  - 22 factors, 15 vectors, multi-interruption possible
- Standby mode
  - Sleep/stop
- Package
  - 100-pin plastic QFP/LQFP
- Piggy/evaluation chip
  - CXP740000

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Block Diagram

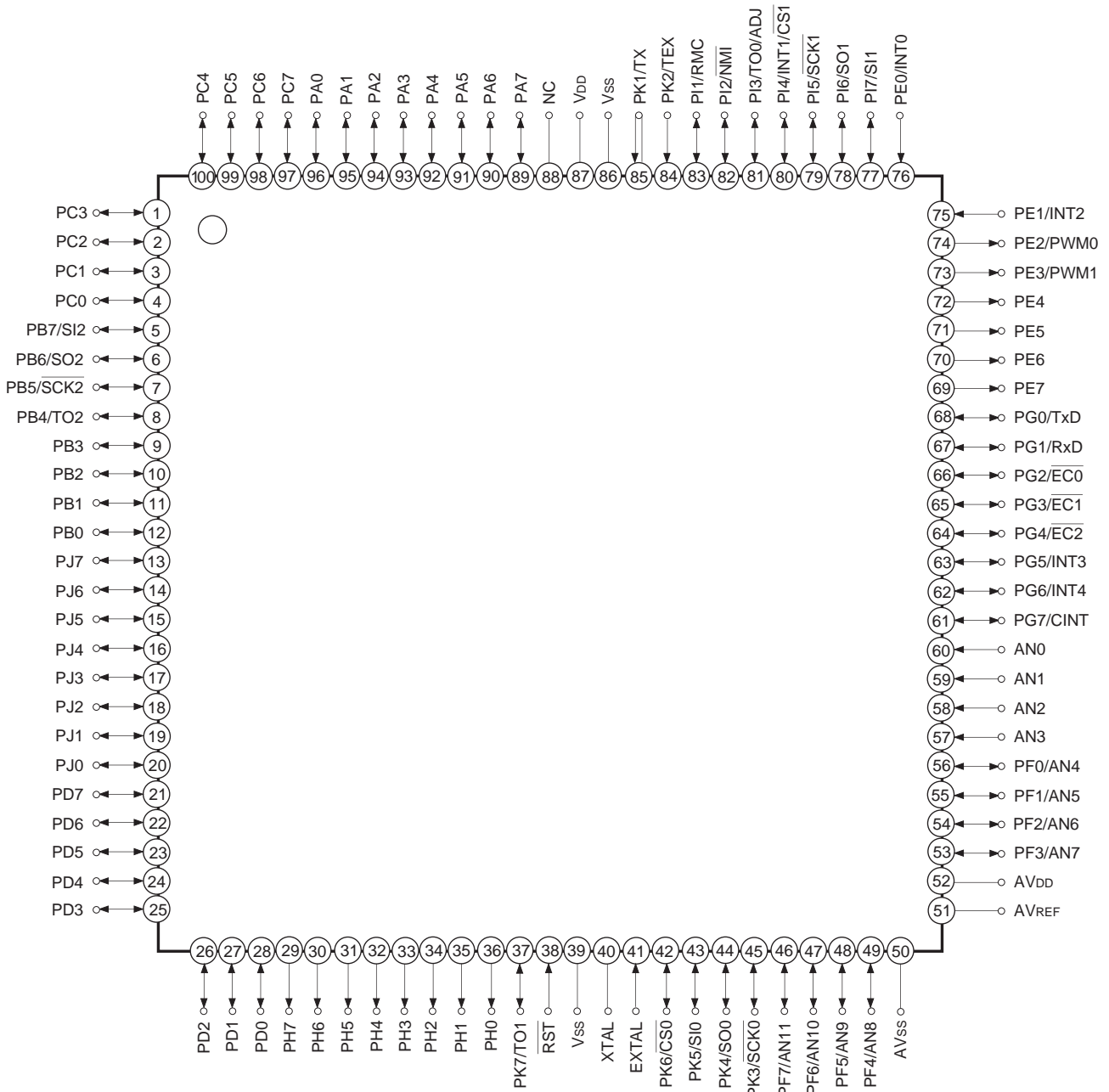


Pin Assignment (Top View) 100-pin QFP package



- Note)** 1. NC (Pin 90) is left open.  
 2. Vss (Pins 41 and 88) are both connected to GND.

Pin Assignment (Top View) 100-pin LQFP package



- Note**
1. NC (Pin 88) is left open.
  2. Vss (Pins 39 and 86) are both connected to GND.

Pin Description

Symbol	I/O	Description	
PA0 to PA7	I/O	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PB0 to PB3	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	16-bit timer/counter rectangular wave output.
PB4/TO2	I/O/Output		Serial clock I/O (CH2).
PB5/SCK2	I/O/I/O		Serial data output (CH2).
PB6/SO2	I/O/Output		Serial data input (CH2).
PB7/SI2	I/O/Input		
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sink current. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PE0/INT0	Input/Input	(Port E) 8-bit port. Lower 2 bits are for input; upper 6 bits are for output. (8 pins)	External interrupt inputs. (2 pins)
PE1/INT1	Input/Input		12-bit PWM outputs. (2 pins)
PE2/PWM0	Output/Output		
PE3/PWM1	Output/Output		
PE4 to PE7	Output		
PF0/AN4 to PF7/AN11	I/O	(Port F) 8-bit I/O port. PF4 to PF7 can be set in a unit of single bits as standby release inputs. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	Analog inputs to A/D converter. (8 pins)

Symbol	I/O	Description		
PG0/TxD	I/O/Output	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	UART transmission data output.	
PG1/RxD	I/O/Input		UART reception data input.	
PG2/ $\overline{\text{EC0}}$	I/O/Input		External event input for 8-bit timer/counter 0.	
PG3/ $\overline{\text{EC1}}$	I/O/Input		External event input for 8-bit timer/counter 2.	
PG4/ $\overline{\text{EC2}}$	I/O/Input		External event input for 16-bit timer/counter.	
PG5/INT3	I/O/Input		External interrupt inputs. (2 pins)	
PG6/INT4	I/O/Input			
PG7/CINT	I/O/Input		External capture input to 16-bit timer/counter.	
PH0 to PH7	Output	(Port H) 8-bit I/O port. Operated as N-ch open drain output for medium voltage drive (12V) and large current (12mA). (8 pins)		
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (7 pins)	Remote control receiver circuit input.	
PI2/ $\overline{\text{NMI}}$	I/O/Input		Non-maskable interrupt input.	
PI3/TO0/ ADJ	I/O/Output/ Output		Output for the 8-bit timer/counter 1 rectangular waves and 32-kHz oscillation frequency demultiplication.	
PI4/INT1/ $\overline{\text{CS1}}$	I/O/Input/ Input		External interrupt input.	Chip select input for serial interface (CH1).
PI5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock I/O (CH1).	
PI6/SO1	I/O/Output		Serial data output (CH1).	
PI7/SI1	I/O/Input		Serial data input (CH1).	
PJ0 to PJ7	I/O		(Port J) 8-bit I/O port. I/O can be set in a unit of single bits. Standby release input can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the program in a unit of single bits. (8 pins)	
PK1/TX	Input	(Port K) 7-bit port. lower 2 bits are for input; upper 5 bits are for I/O. I/O can be set in a unit of single bits. For PK3 to PK7, incorporation of pull-up resistor can be set through the program in a unit of single bits. (7 pins)	Crystal connectors for 32-kHz timer/counter clock oscillation circuit.	
PK2/TEX	Input/Input		For usage as event count, connect clock oscillation source to TEX, and leave TX open.	
PK3/ $\overline{\text{SCK0}}$	I/O/I/O		Serial clock I/O (CH0).	
PK4/SO0	I/O/Output		Serial data output (CH0).	
PK5/SI0	I/O/Input		Serial data input (CH0).	
PK6/ $\overline{\text{CS0}}$	I/O/Input		Chip select input for serial interface (CH0).	
PK7/TO1	I/O/Output		8-bit timer/counter 3 rectangular wave output.	

Symbol	I/O	Description
AN0 to AN3	Input	Analog inputs to A/D converter. (4 pins)
EXTAL	Input	Connects a crystal for system clock oscillation. When a clock is supplied externally, input it to EXTAL pin and input a reversed phase clock to XTAL pin.
XTAL		
$\overline{\text{RST}}$	Input	System reset; active at Low level.
NC		Not connected. Leave this pin open for normal operation.
AVDD		Positive power supply of A/D converter.
AVREF	Input	Reference voltage input of A/D converter.
AVSS		GND of A/D converter.
VDD		Positive power supply.
VSS		GND. Connect both Vss pins to GND.

I/O Circuit Format for Pins

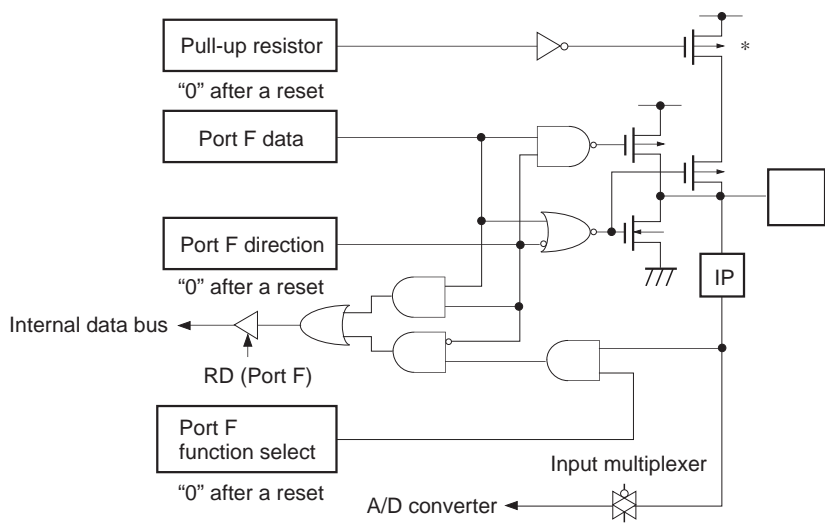
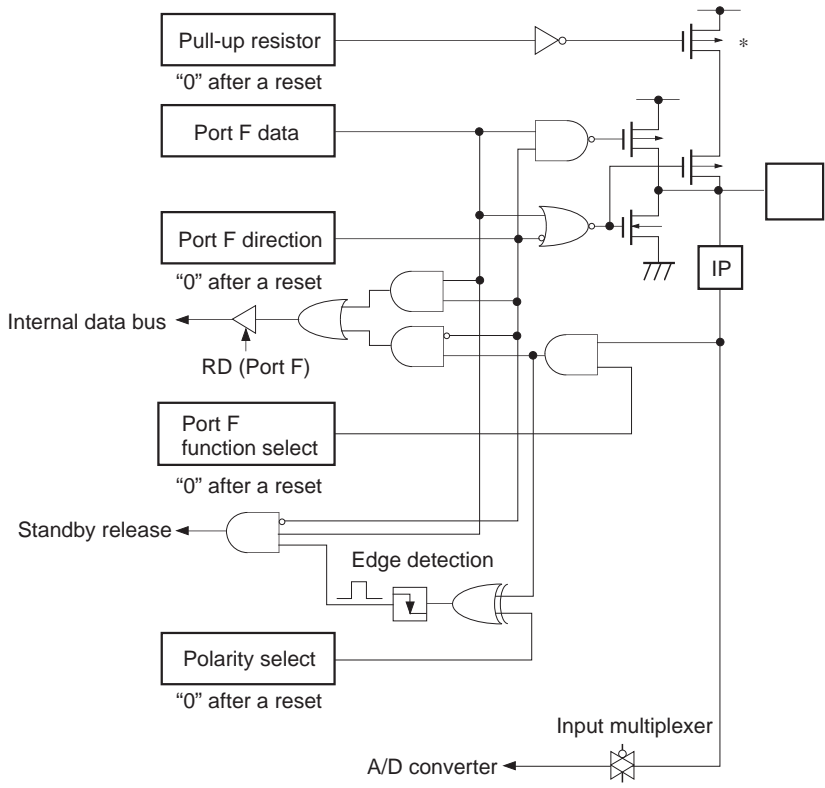
Pin	Circuit format		After a reset
PA0 to PA7 PB0 PB2 PC0 to PC7  18 pins	Port A Port B Port C		Hi-Z
PB1 PB3  2 pins	Port B		Hi-Z
PB4/TO2 PI3/TO0/ADJ PK7/TO1  3 pins	Port I Port K		Hi-Z

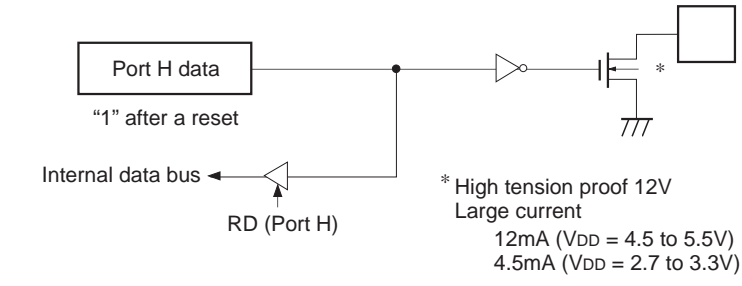
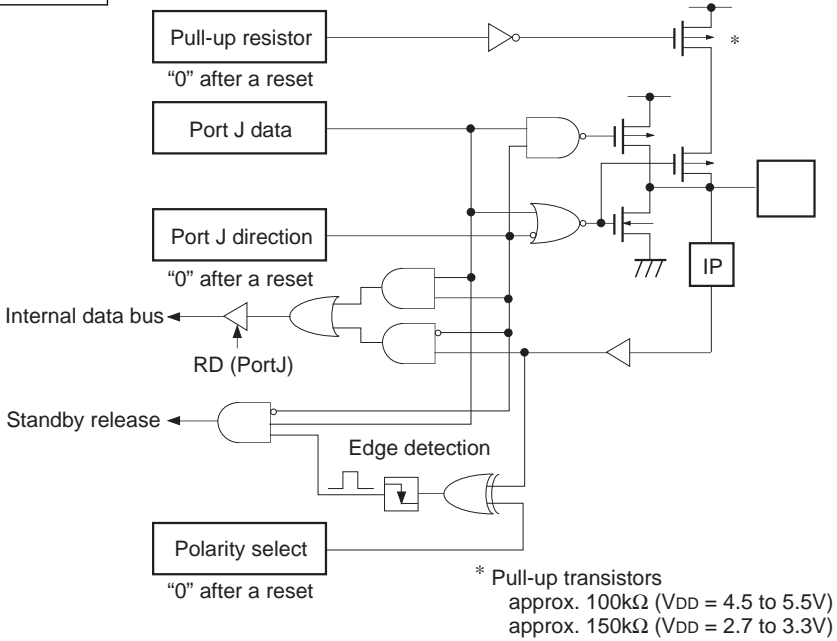
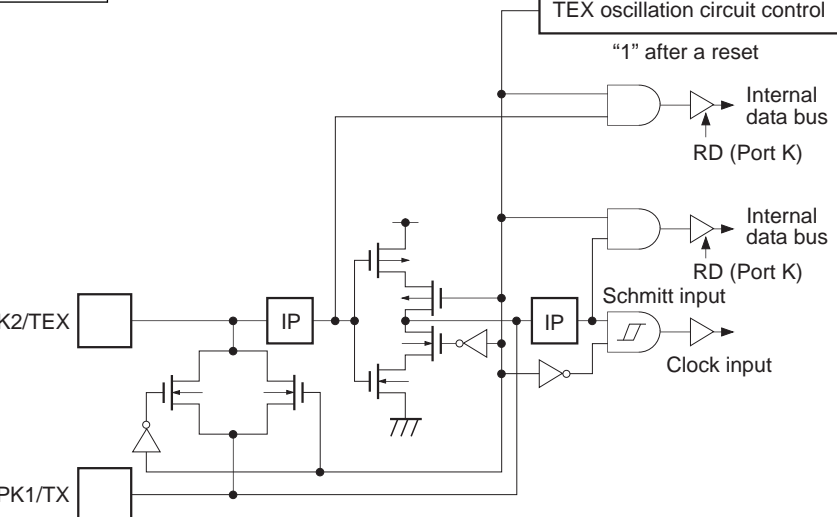


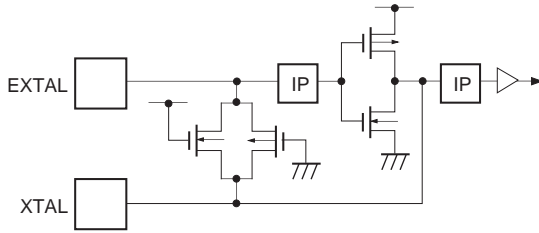
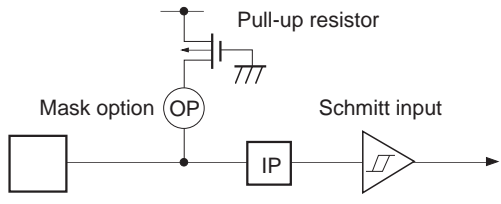
Pin	Circuit format	After a reset
<p>Port B</p> <p>Port I</p> <p>Port K</p> <p>PB5/SCK2 PI5/SCK1 PK3/SCK0</p> <p>3 pins</p>	<p>Pull-up resistor "0" after a reset</p> <p>Output buffer capability "0" after a reset Output enable</p> <p>SCK2, SCK1, SCK0</p> <p>Ports B, I, K function select "0" after a reset</p> <p>Ports B, I, K data</p> <p>Ports B, I, K direction "0" after a reset</p> <p>Internal data bus</p> <p>RD (Ports B, I, K)</p> <p>SCK2, SCK1, SCK0</p> <p>Schmitt input</p> <p>* Pull-up transistors approx. 100kΩ (V<sub>DD</sub> = 4.5 to 5.5V) approx. 150kΩ (V<sub>DD</sub> = 2.7 to 3.3V)</p>	<p>Hi-Z</p>
<p>Port B</p> <p>Port G</p> <p>Port I</p> <p>Port K</p> <p>PB6/SO2 PG0/TxD PI6/SO1 PK4/SO0</p> <p>4 pins</p>	<p>Pull-up resistor "0" after a reset</p> <p>Output buffer capability "0" after a reset Output enable</p> <p>TO2, SO2, TxD, SO1, SO0</p> <p>Ports B, G, I, K function select "0" after a reset</p> <p>Ports B, G, I, K data</p> <p>Ports B, G, I, K direction "0" after a reset</p> <p>Internal data bus</p> <p>RD (Ports B, G, I, K)</p> <p>* Pull-up transistors approx. 100kΩ (V<sub>DD</sub> = 4.5 to 5.5V) approx. 150kΩ (V<sub>DD</sub> = 2.7 to 3.3V)</p>	<p>Hi-Z</p>



Pin	Circuit format	After a reset
<p>PE2/PWM0 PE3/PWM1</p> <p>2 pins</p>	<p>Port E</p> <p>Hi-Z by writing to Port E data register or Port E function select register → Output active</p>	<p>Hi-Z</p>
<p>PE4 PE5</p> <p>2 pins</p>	<p>Port E</p> <p>Hi-Z by writing to Port E data register → Output active</p>	<p>Hi-Z</p>
<p>PE6</p> <p>1 pin</p>	<p>Port E</p> <p>High level</p>	<p>High level</p>
<p>PE7</p> <p>1 pin</p>	<p>Port E</p> <p>* Pull-up transistors approx. 150kΩ (VDD = 4.5 to 5.5V) approx. 200kΩ (VDD = 2.7 to 3.3V)</p>	<p>"H" level ("H" level at ON resistance of pull-up transistor during a reset.)</p>
<p>AN0 to AN3</p> <p>4 pins</p>		<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PF0/AN4 to PF3/AN7</p> <p>4 pins</p>	<p>Port F</p>  <p>Pull-up resistor "0" after a reset</p> <p>Port F data</p> <p>Port F direction "0" after a reset</p> <p>Internal data bus</p> <p>RD (Port F)</p> <p>Port F function select "0" after a reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>* Pull-up transistors approx. 100kΩ (V<sub>DD</sub> = 4.5 to 5.5V) approx. 150kΩ (V<sub>DD</sub> = 2.7 to 3.3V)</p>	<p>Hi-Z</p>
<p>PF4/AN8 to PF7/AN11</p> <p>4 pins</p>	<p>Port F</p>  <p>Pull-up resistor "0" after a reset</p> <p>Port F data</p> <p>Port F direction "0" after a reset</p> <p>Internal data bus</p> <p>RD (Port F)</p> <p>Port F function select "0" after a reset</p> <p>Standby release</p> <p>Edge detection</p> <p>Polarity select "0" after a reset</p> <p>Input multiplexer</p> <p>A/D converter</p> <p>* Pull-up transistors approx. 100kΩ (V<sub>DD</sub> = 4.5 to 5.5V) approx. 150kΩ (V<sub>DD</sub> = 2.7 to 3.3V)</p>	<p>Hi-Z</p>

Pin	Circuit format	After a reset
<p>PH0 to PH7</p> <p>8 pins</p>	<p>Port H</p>  <p>Port H data "1" after a reset</p> <p>Internal data bus</p> <p>RD (Port H)</p> <p>* High tension proof 12V Large current 12mA (<math>V_{DD} = 4.5</math> to <math>5.5V</math>) 4.5mA (<math>V_{DD} = 2.7</math> to <math>3.3V</math>)</p>	<p>Hi-Z</p>
<p>PJ0 to PJ7</p> <p>8 pins</p>	<p>Port J</p>  <p>Pull-up resistor "0" after a reset</p> <p>Port J data</p> <p>Port J direction "0" after a reset</p> <p>Internal data bus</p> <p>RD (Port J)</p> <p>Standby release</p> <p>Edge detection</p> <p>Polarity select "0" after a reset</p> <p>* Pull-up transistors approx. <math>100k\Omega</math> (<math>V_{DD} = 4.5</math> to <math>5.5V</math>) approx. <math>150k\Omega</math> (<math>V_{DD} = 2.7</math> to <math>3.3V</math>)</p>	<p>Hi-Z</p>
<p>PK1/TX PK2/TEX</p> <p>2 pins</p>	<p>Port K</p>  <p>TEX oscillation circuit control "1" after a reset</p> <p>Internal data bus</p> <p>RD (Port K)</p> <p>Internal data bus</p> <p>RD (Port K)</p> <p>Schmitt input</p> <p>Clock input</p> <p>PK2/TEX</p> <p>PK1/TX</p>	<p>Oscillation stop port input</p>

Pin	Circuit format	After a reset
<p>EXTAL XTAL</p> <p>2 pins</p>	 <ul style="list-style-type: none"> <li>• Diagram shows circuit configuration during oscillation.</li> <li>• When program stops the oscillation, the feedback register disconnects, and XTAL is driven at "H" level.</li> </ul>	<p>Oscillation</p>
<p><math>\overline{\text{RST}}</math></p> <p>1 pin</p>	 <p>Pull-up resistor</p> <p>Mask option (OP)</p> <p>Schmitt input</p>	<p>"L" level (during a reset)</p>

## Absolute Maximum Ratings

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V <sub>DD</sub>	-0.3 to +7.0	V	
	AV <sub>DD</sub>	AV <sub>SS</sub> to +7.0* <sup>1</sup>	V	
	AV <sub>SS</sub>	-0.3 to +0.3	V	
	AV <sub>REF</sub>	AV <sub>SS</sub> to +7.0	V	
Input voltage	V <sub>IN</sub>	-0.3 to +7.0* <sup>2</sup>	V	
Output voltage	V <sub>OUT</sub>	-0.3 to +7.0* <sup>2</sup>	V	
High level output current	I <sub>OH</sub>	-5	mA	Output (value per pin)
High level total output current	∑I <sub>OH</sub>	-50	mA	Total for all output pins
Low level output current	I <sub>OL</sub>	15	mA	All pins excluding large current outputs (value per pin)
	I <sub>OLC</sub>	20	mA	Large current outputs (value per pin) * <sup>3</sup>
Low level total output current	∑I <sub>OL</sub>	100	mA	Total for all output pins
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	
Allowable power dissipation	P <sub>D</sub>	600	mW	QFP package
		380		LQFP package

\*<sup>1</sup> AV<sub>DD</sub> and V<sub>DD</sub> must be set to the same voltage.

\*<sup>2</sup> V<sub>IN</sub> and V<sub>OUT</sub> must not exceed V<sub>DD</sub> + 0.3V.

\*<sup>3</sup> The large current output pins are Port D and H (PD, PH).

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V <sub>DD</sub>	4.5	5.5	V	fc = 24MHz or less
		2.7	5.5	V	fc = 12MHz or less
		2.7	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or sleep mode
		2.7	5.5	V	Guaranteed operation range for TEX
		2.5	5.5	V	Guaranteed data hold operation range during stop mode
Analog voltage	AV <sub>DD</sub>	2.7	5.5	V	*1
High level input voltage	V <sub>IH</sub>	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	*2, *6
		0.8V <sub>DD</sub>	V <sub>DD</sub>	V	*2, *7
	V <sub>IHS</sub>	0.8V <sub>DD</sub>	V <sub>DD</sub>	V	Hysteresis input*3
	V <sub>IHEX</sub>	V <sub>DD</sub> - 0.4	V <sub>DD</sub> + 0.3	V	EXTAL pin*4, *6, TEX pin*5, *6
		V <sub>DD</sub> - 0.2	V <sub>DD</sub> + 0.2	V	EXTAL pin*4, *7, TEX pin*5, *7
Low level input voltage	V <sub>IL</sub>	0	0.3V <sub>DD</sub>	V	*2, *6
		0	0.2V <sub>DD</sub>	V	*2, *7
	V <sub>ILS</sub>	0	0.2V <sub>DD</sub>	V	Hysteresis input*3
	V <sub>ILEX</sub>	-0.3	0.4	V	EXTAL pin*4, *6, TEX pin*5, *6
		-0.3	0.2	V	EXTAL pin*4, *7, TEX pin*5, *7
Operating temperature	Topr	-20	+75	°C	

\*1 AV<sub>DD</sub> and V<sub>DD</sub> must be set to the same voltage.

\*2 Normal input port (PA, PB0, PB2, PB4, PB6, PC, PD, PF, PG0, PI3, PI6, PJ, PK1, PK2, PK4, PK7)

\*3 RST, PB1, PB3, PB5/SCK2, PB7/SI2, PE0/INT0, PE1/INT2, PG1/RxD, PG2/EC0, PG3/EC1, PG4/EC2, PG5/INT3, PG6/INT4, PG7/CINT, PI1/RMC, PI2/NMI, PI4/INT1/CS1, PI5/SCK1, PI7/SI1, PK3/SCK0, PK5/SIO, PK6/CS0

\*4 Specifies only when the external clock is input.

\*5 Specifies only when the external event count is input.

\*6 This case applies to the range of 4.5 to 5.5V supply voltage (V<sub>DD</sub>).

\*7 This case applies to the range of 2.7 to 5.5V supply voltage (V<sub>DD</sub>).



## Electrical Characteristics

DC Characteristics ( $V_{DD} = 4.5$  to  $5.5V$ )( $T_a = -20$  to  $+75^\circ C$ ,  $V_{SS} = 0V$  reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit	
High level output voltage	$V_{OH}$	PA to PD, PE2 to PE7, PF to PG, PI to PJ, PK3 to PK7	$V_{DD} = 4.5V, I_{OH} = -0.5mA$	4.0			V	
			$V_{DD} = 4.5V, I_{OH} = -1.2mA$	3.5			V	
		PB5, PB6*1, PG0*1, PI5, PI6*1, PK3, PK4*1	$V_{DD} = 4.5V, I_{OH} = -1.0mA$	4.0			V	
			$V_{DD} = 4.5V, I_{OH} = -2.4mA$	3.5			V	
Low level output voltage	$V_{OL}$	PA to PD, PE2 to PE7, PF to PG, PI to PJ, PK3 to PK7	$V_{DD} = 4.5V, I_{OL} = 1.8mA$			0.4	V	
			$V_{DD} = 4.5V, I_{OL} = 3.6mA$			0.6	V	
		PD, PH	$V_{DD} = 4.5V, I_{OL} = 12.0mA$			1.5	V	
Input current	$I_{IHE}$	EXTAL	$V_{DD} = 5.5V, V_{IH} = 5.5V$	0.5		40	$\mu A$	
	$I_{ILE}$		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.5		-40	$\mu A$	
	$I_{IHT}$	TEX	$V_{DD} = 5.5V, V_{IL} = 5.5V$	0.1		10	$\mu A$	
	$I_{ILT}$		$V_{DD} = 5.5V, V_{IL} = 0.4V$	-0.1		-10	$\mu A$	
	$I_{ILR}$	$\overline{RST}^{*2}$	$V_{DD} = 5.5V, V_{IL} = 0.4V$			-1.5	-400	$\mu A$
	$I_{IL}$	PA to PD*3, PF to PG*3, PI to PK*3					-45	$\mu A$
I/O leakage current	$I_{IZ}$	PA to PD*3, PF to PG*3, PI to PK*3, PE, AN0 to AN3 $\overline{RST}^{*2}$	$V_{DD} = 5.5V$ $V_I = 0, 5.5V$			$\pm 10$	$\mu A$	
Open drain output leakage current (N-ch Tr off state)	$LLOH$	PH	$V_{DD} = 5.5V$ $V_{OH} = 12V$			50	$\mu A$	

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*4	I <sub>DD1</sub>	V <sub>DD</sub>	24MHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 15pF)		27	47	mA
			V <sub>DD</sub> = 5V ± 0.5V				
	I <sub>DDS1</sub>		Sleep mode		1.0	5.0	mA
			V <sub>DD</sub> = 5V ± 0.5V				
	I <sub>DD2</sub>		32kHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 47pF)		30	75	μA
			V <sub>DD</sub> = 3V ± 0.3V				
I <sub>DDS2</sub>	Sleep mode		12	40	μA		
	V <sub>DD</sub> = 3V ± 0.3V						
I <sub>DDS3</sub>	Stop mode (Termination of EXTAL and TEX pins crystal oscillation)			10	μA		
		V <sub>DD</sub> = 5V ± 0.5V					
Input capacity	C <sub>IN</sub>	PA to PD, PE0 to PE1, PF to PG, PI to PK, AN0 to AN3, EXTAL, RST	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

\*1 This case applies that Port B buffer capability switching register (BUFB: 010F4h, bits 6 and 5 = "1, 1") and Ports G/I/K buffer capability switching register (BUFG: 010F5h, bits 6, 5, 4, 3 and 0= "1, 1, 1, 1, 1") are ON.

\*2 RST pin specifies the input current when the pull-up resistor is selected, and specifies the leakage current when no resistor is selected.

\*3 PA to PD, PF to PG and PI to PK pins specify the input current when the pull-up resistor is selected, and specify the leakage current when no resistor is selected.

\*4 When all pins are open.

## Electrical Characteristics

DC Characteristics ( $V_{DD} = 2.7$  to  $3.3V$ )(Ta = -20 to +75°C,  $V_{SS} = 0V$  reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	$V_{OH}$	PA to PD, PE2 to PE7, PF to PG, PI to PJ, PK3 to PK7	$V_{DD} = 2.7V, I_{OH} = -0.12mA$	2.5			V
			$V_{DD} = 2.7V, I_{OH} = -0.45mA$	2.1			V
		PB5, PB6*1, PG0*1, PI5, PI6*1, PK3, PK4*1	$V_{DD} = 2.7V, I_{OH} = -0.24mA$	2.5			V
			$V_{DD} = 2.7V, I_{OH} = -0.9mA$	2.1			V
Low level output voltage	$V_{OL}$	PA to PD, PE2 to PE7, PF to PG, PI to PJ, PK3 to PK7	$V_{DD} = 2.7V, I_{OL} = 1.0mA$			0.25	V
			$V_{DD} = 2.7V, I_{OL} = 1.4mA$			0.4	V
		PD, PH	$V_{DD} = 2.7V, I_{OL} = 4.5mA$			0.9	V
Input current	$I_{IHE}$	EXTAL	$V_{DD} = 3.3V, V_{IH} = 3.3V$	0.3		20	$\mu A$
	$I_{ILE}$		$V_{DD} = 3.3V, V_{IL} = 0.3V$	-0.3		-20	$\mu A$
	$I_{IHT}$	TEX	$V_{DD} = 3.3V, V_{IL} = 3.3V$	0.1		10	$\mu A$
	$I_{ILT}$		$V_{DD} = 3.3V, V_{IL} = 0.4V$	-0.1		-10	$\mu A$
	$I_{ILR}$	$\overline{RST}^{*2}$	$V_{DD} = 3.3V, V_{IL} = 0.3V$	-0.9		-200	$\mu A$
	$I_{IL}$	PA to PD*3, PF to PG*3, PI to PK*3	$V_{DD} = 3.3V, V_{IL} = 0.3V$			-20	$\mu A$
		$V_{DD} = 3.3V, V_{IL} = 2.7V$	-1.0			$\mu A$	
I/O leakage current	$I_{IZ}$	PA to PD*3, PF to PG*3, PI to PK*3, PE, AN0 to AN3 $\overline{RST}^{*2}$	$V_{DD} = 3.3V$ $V_I = 0, 3.3V$			$\pm 10$	$\mu A$
Open drain output leakage current (N-ch Tr off state)	$LLOH$	PH	$V_{DD} = 3.3V$ $V_{OH} = 12V$			50	$\mu A$

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*4	I <sub>DD1</sub>	V <sub>DD</sub>	12MHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 15pF)		8	20	mA
			V <sub>DD</sub> = 3.0V ± 0.3V*3				
	I <sub>DDS1</sub>		Sleep mode		0.3	1.5	mA
	V <sub>DD</sub> = 3.0V ± 0.3V						
	I <sub>DDS3</sub>		Stop mode (Termination of EXTAL and TEX pins crystal oscillation)			10	μA
			V <sub>DD</sub> = 3.0V ± 0.3V				
Input capacity	C <sub>IN</sub>	PA to PD, PE0 to PE1, PF to PG, PI to PK, AN0 to AN3, EXTAL, RST	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

\*1 This case applies that Port B buffer capability switching register (BUFB: 010F4h, bits 6 and 5 = "1, 1") and Ports G/I/K buffer capability switching register (BUFG: 010F5h, bits 6, 5, 4, 3 and 0 = "1, 1, 1, 1, 1") are ON.

\*2  $\overline{\text{RST}}$  pin specifies the input current when the pull-up resistor is selected, and specifies the leakage current when no resistor is selected.

\*3 PA to PD, PF to PG and PI to PK pins specify the input current when the pull-up resistor is selected, and specify the leakage current when no resistor is selected.

\*4 When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 2.7 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	fc	XTAL EXTAL	Fig. 1, Fig. 2	VDD = 4.5 to 5.5V	1	24	MHz
					1	12	
System clock input pulse width	tXL, tXH	EXTAL	Fig. 1, Fig. 2	External clock drive	VDD = 4.5 to 5.5V	28	ns
						37.5	
System clock input rise time, fall time	tCR, tCF	EXTAL	Fig. 1, Fig. 2			200	ns
Event count input clock pulse width	tEH, tEL	EC	Fig. 3	tsys + 50*1			ns
Event count input clock rise time, fall time	tER, tEF	EC	Fig. 3			20	ms
System clock frequency	fc	TEX TX	VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock pulse width	tTL, tTH	TEX	Fig. 3	10			µs
Event count input clock rise time, fall time	tTR, tTF	TEX	Fig. 3			20	ms

\*1 tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 000FEh).

tsys [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

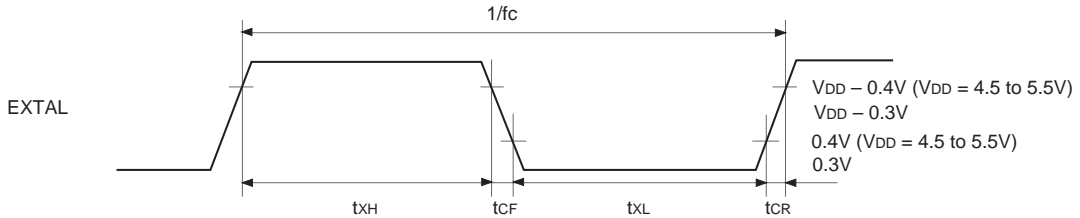


Fig. 1. Clock timing

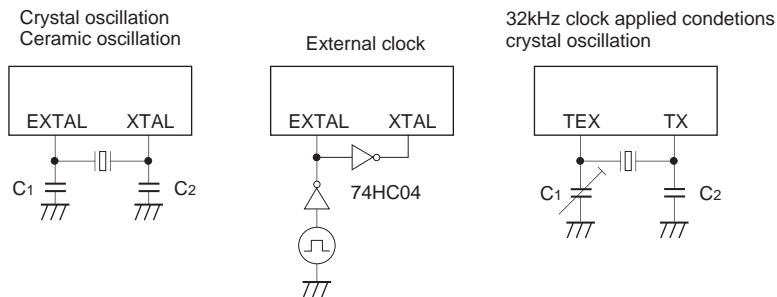


Fig. 2. Clock applied conditions

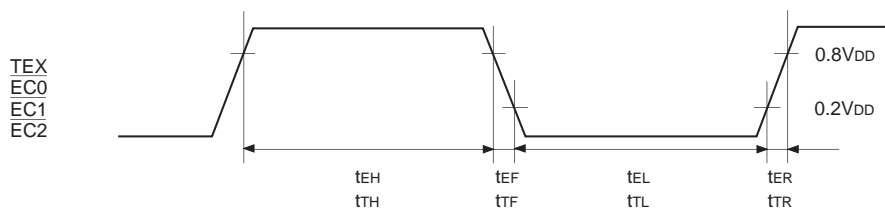


Fig. 3. Event count clock timing

(2) Serial transfer (CH0, CH1)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS}\downarrow \rightarrow \overline{SCK}$ delay time	t <sub>D<sub>CSK</sub></sub>	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ( $\overline{SCK}$ = output mode)		1.5t <sub>sys</sub> + 200	ns
$\overline{CS}\uparrow \rightarrow \overline{SCK}$ floating delay time	t <sub>D<sub>CSKF</sub></sub>	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ( $\overline{SCK}$ = output mode)		1.5t <sub>sys</sub> + 200	ns
$\overline{CS}\downarrow \rightarrow SO$ delay time	t <sub>D<sub>CSO</sub></sub>	SO0 SO1	Chip select transfer mode		1.5t <sub>sys</sub> + 200	ns
$\overline{CS}\uparrow \rightarrow SO$ floating delay time	t <sub>D<sub>CSOF</sub></sub>	SO0 SO1	Chip select transfer mode		1.5t <sub>sys</sub> + 200	ns
$\overline{CS}$ High level width	t <sub>WH<sub>CS</sub></sub>	$\overline{CS0}$ $\overline{CS1}$	Chip select transfer mode	t <sub>sys</sub> + 200		ns
$\overline{SCK}$ cycle time	t <sub>K<sub>CY</sub></sub>	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	2t <sub>sys</sub> + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level width	t <sub>K<sub>H</sub></sub> t <sub>K<sub>L</sub></sub>	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	t <sub>sys</sub> + 100		ns
			Output mode	4000/fc - 50		ns
SI input setup time (for $\overline{SCK}\uparrow$ )	t <sub>SI<sub>K</sub></sub>	SI0 SI1	$\overline{SCK}$ input mode	-t <sub>sys</sub> + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$ )	t <sub>K<sub>SI</sub></sub>	SI0 SI1	$\overline{SCK}$ input mode	2t <sub>sys</sub> + 200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow \rightarrow SO$ delay time	t <sub>K<sub>SO</sub></sub>	SO0 SO1	$\overline{SCK}$ input mode		2t <sub>sys</sub> + 200	ns
			$\overline{SCK}$ output mode		100	ns

**Note 1)** t<sub>sys</sub> indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (upper 2 bits = "00"), 4000/fc (upper 2 bits = "01"), 16000/fc (upper 2 bits = "11")

**Note 2)**  $\overline{CS}$ ,  $\overline{SCK}$ , SI and SO represent  $\overline{CS0}$ ,  $\overline{SCK0}$ , SI0 and SO0 for CH0; they represent  $\overline{CS1}$ ,  $\overline{SCK1}$ , SI1 and SO1 for CH1, respectively.

**Note 3)** The load of  $\overline{SCK}$  output mode and SO output delay time is 50pF + 1TTL.

**Note 4)** This case applies that Port I/K output buffer capability switching register (BUFG: 010F5h, bits 6, 5, 4 and 3 = "0, 0, 0, 0") is OFF.

**Serial transfer (CH0, CH1)**

(Ta = -20 to +75°C, VDD = 2.7 to 3.3V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS}\downarrow \rightarrow \overline{SCK}$ delay time	t <sub>DCSK</sub>	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ( $\overline{SCK}$ = output mode)		1.5t <sub>sys</sub> + 250	ns
$\overline{CS}\uparrow \rightarrow \overline{SCK}$ floating delay time	t <sub>DCSKF</sub>	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode ( $\overline{SCK}$ = output mode)		1.5t <sub>sys</sub> + 250	ns
$\overline{CS}\downarrow \rightarrow \overline{SO}$ delay time	t <sub>DCSO</sub>	SO0 SO1	Chip select transfer mode		1.5t <sub>sys</sub> + 250	ns
$\overline{CS}\uparrow \rightarrow \overline{SO}$ floating delay time	t <sub>DCSOF</sub>	SO0 SO1	Chip select transfer mode		1.5t <sub>sys</sub> + 250	ns
$\overline{CS}$ High level width	t <sub>WHCS</sub>	$\overline{CS0}$ $\overline{CS1}$	Chip select transfer mode	t <sub>sys</sub> + 200		ns
$\overline{SCK}$ cycle time	t <sub>KCY</sub>	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	2t <sub>sys</sub> + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ High and Low level widths	t <sub>KH</sub> t <sub>KL</sub>	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	t <sub>sys</sub> + 100		ns
			Output mode	4000/fc - 100		ns
SI input setup time (for $\overline{SCK}\uparrow$ )	t <sub>SIK</sub>	SI0 SI1	$\overline{SCK}$ input mode	-t <sub>sys</sub> + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$ )	t <sub>KSI</sub>	SI0 SI1	$\overline{SCK}$ input mode	2t <sub>sys</sub> + 200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow \rightarrow \overline{SO}$ delay time	t <sub>KSO</sub>	SO0 SO1	$\overline{SCK}$ input mode		2t <sub>sys</sub> + 250	ns
			$\overline{SCK}$ output mode		125	ns

**Note 1)** t<sub>sys</sub> indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).

t<sub>sys</sub> [ns] = 2000/fc (upper 2 bits = "00"), 4000/fc (upper 2 bits = "01"), 16000/fc (upper 2 bits = "11")

**Note 2)**  $\overline{CS}$ ,  $\overline{SCK}$ , SI and SO represent  $\overline{CS0}$ ,  $\overline{SCK0}$ , SI0 and SO0 for CH0; they represent  $\overline{CS1}$ ,  $\overline{SCK1}$ , SI1 and SO1 for CH1, respectively.

**Note 3)** The load of  $\overline{SCK}$  output mode and SO output delay time is 50pF.

**Note 4)** This case applies that Port G/I/K output buffer capability switching register (BUFG: 010F5h, bits 6, 5, 4 and 3 = "1, 1, 1, 1") is ON.

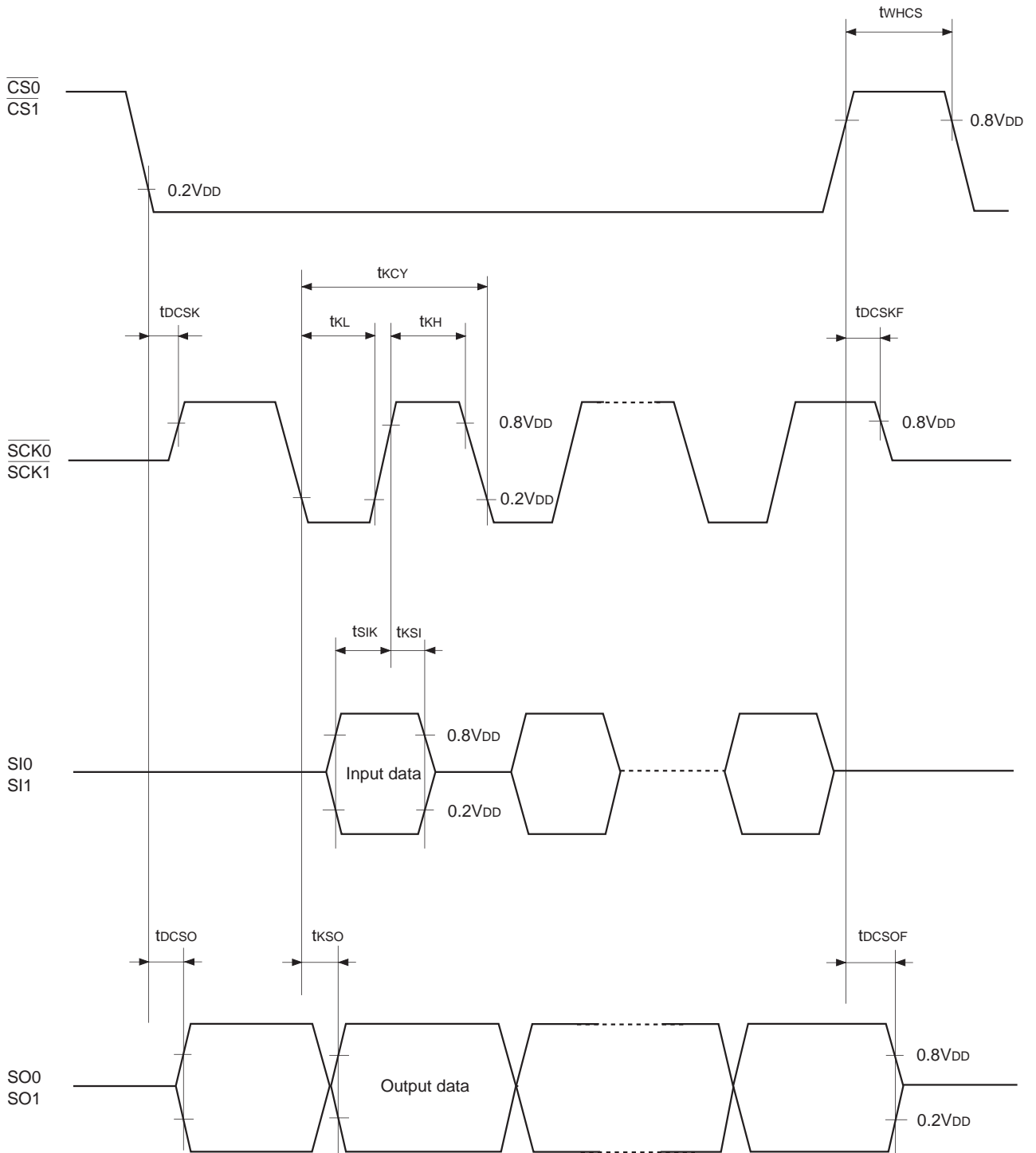


Fig. 4. Serial transfer CH0, CH1 timing



**Serial transfer (CH2)**

(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK2}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
SCK High and Low level widths	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK2}}$	Input mode	400		ns
			Output mode	4000/fc - 50		ns
SI input setup time (for $\overline{\text{SCK}}\uparrow$ )	$t_{\text{SIK}}$	SI2	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}}\uparrow$ )	$t_{\text{KSI}}$	SI2	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
SCK $\downarrow$ → SO delay time	$t_{\text{KSO}}$	SO2	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

**Note 1)**  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).

$$t_{\text{sys}} [\text{ns}] = 2000/\text{fc} \text{ (upper 2 bits = "00")}, 4000/\text{fc} \text{ (upper 2 bits = "01")}, 16000/\text{fc} \text{ (upper 2 bits = "11")}$$

**Note 2)**  $\overline{\text{SCK}}$ , SI and SO represent  $\overline{\text{SCK2}}$ , SI2 and SO2 for CH2, respectively.

**Note 3)** The load of SCK2 output mode and SO2 output delay time is 50pF+1TTL.

**Note 4)** This case applies that Port B output buffer capability switching register (BUFB: 010F4h, bits 6 and 5 = "0, 0") is OFF.

**Serial transfer (CH2)**

(Ta = -20 to +75°C, V<sub>DD</sub> = 2.7 to 3.3V, V<sub>SS</sub> = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	$t_{\text{KCY}}$	$\overline{\text{SCK2}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
SCK High and Low level widths	$t_{\text{KH}}$ $t_{\text{KL}}$	$\overline{\text{SCK2}}$	Input mode	400		ns
			Output mode	4000/fc - 100		ns
SI input setup time (for $\overline{\text{SCK}}\uparrow$ )	$t_{\text{SIK}}$	SI2	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI input hold time (for $\overline{\text{SCK}}\uparrow$ )	$t_{\text{KSI}}$	SI2	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
SCK $\downarrow$ → SO delay time	$t_{\text{KSO}}$	SO2	$\overline{\text{SCK}}$ input mode		250	ns
			$\overline{\text{SCK}}$ output mode		125	ns

**Note 1)**  $t_{\text{sys}}$  indicates three values according to the contents of the clock control register (CLC: 000FEh) upper 2 bits (CPU clock selection).

$$t_{\text{sys}} [\text{ns}] = 2000/\text{fc} \text{ (upper 2 bits = "00")}, 4000/\text{fc} \text{ (upper 2 bits = "01")}, 16000/\text{fc} \text{ (upper 2 bits = "11")}$$

**Note 2)**  $\overline{\text{SCK}}$ , SI and SO represent  $\overline{\text{SCK2}}$ , SI2 and SO2 for CH2, respectively.

**Note 3)** The load of SCK2 output mode and SO2 output delay time is 50pF.

**Note 4)** This case applies that Port B output buffer capability switching register (BUFB: 010F4h, bits 6 and 5 = "1, 1") is ON.

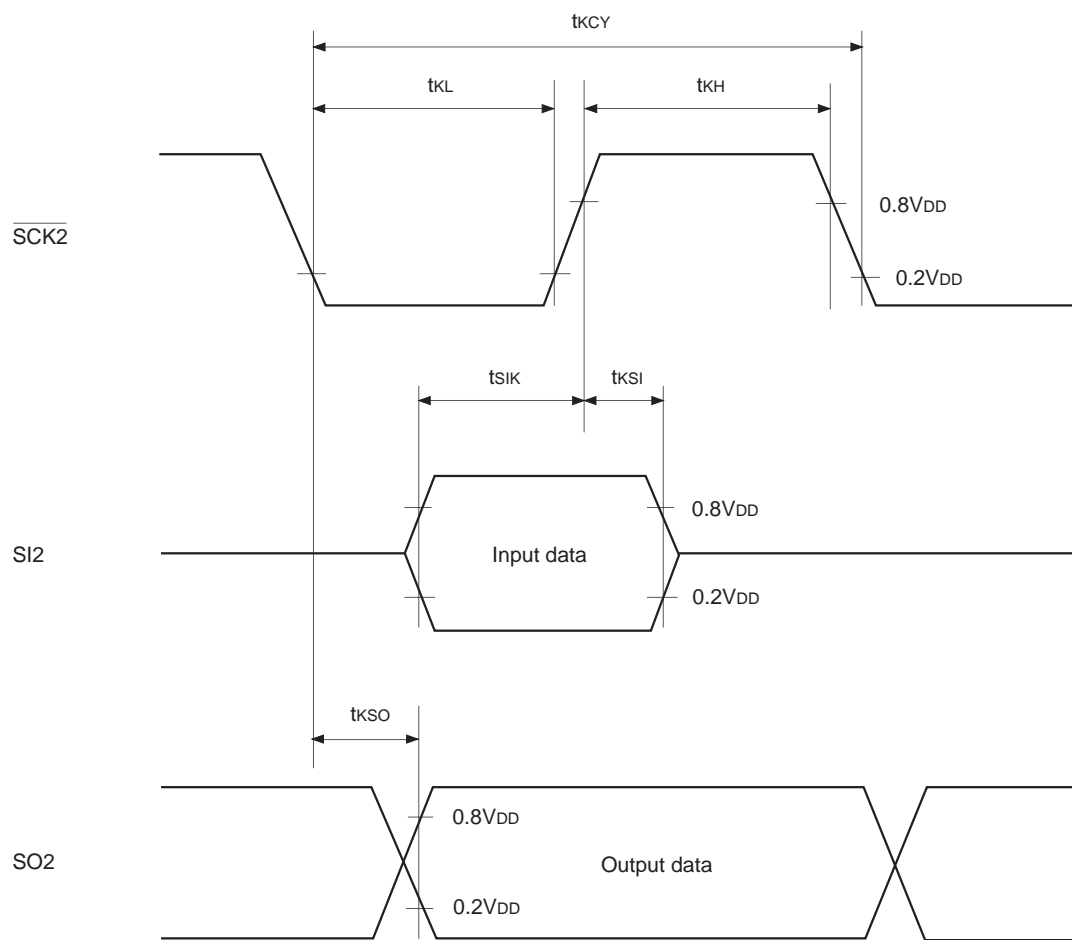


Fig. 5. Serial transfer CH2 timing

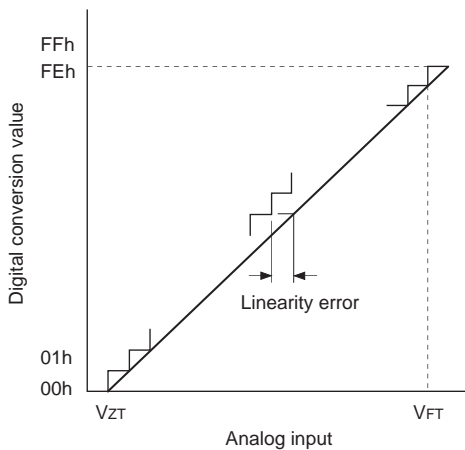
**(3) A/D converter characteristics**

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 4.5$  to  $5.5\text{V}$ ,  $AV_{REF} = 4.0$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 5.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			$\pm 2$	LSB
Absolute error						$\pm 3$	LSB
Conversion time	$t_{CONV}$			$31/f_{ADC}^{*3, *4}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$10/f_{ADC}^{*3, *4}$			$\mu\text{s}$
Reference input voltage	$V_{REF}$	$AV_{REF}$	$V_{DD} = AV_{DD} = 4.5$ to $5.5\text{V}$	$AV_{DD} - 0.5$			V
Analog input voltage	$V_{IAN}$	AN0 to AN11		0			V
AVREF current	$I_{REF}$	$AV_{REF}$	Operation mode		0.6	1.0	mA
	$I_{REFS}$		Sleep mode Stop mode 32kHz operation mode			10	$\mu\text{A}$

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = AV_{DD} = 2.7$  to  $3.3\text{V}$ ,  $AV_{REF} = 2.7$  to  $AV_{DD}$ ,  $V_{SS} = AV_{SS} = 0\text{V}$  reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^\circ\text{C}$ $V_{DD} = AV_{DD} = AV_{REF} = 3.0\text{V}$ $V_{SS} = AV_{SS} = 0\text{V}$			$\pm 2$	LSB
Absolute error						$\pm 3$	LSB
Conversion time	$t_{CONV}$			$31/f_{ADC}^{*3, *4}$			$\mu\text{s}$
Sampling time	$t_{SAMP}$			$10/f_{ADC}^{*3, *4}$			$\mu\text{s}$
Reference input voltage	$V_{REF}$	$AV_{REF}$	$V_{DD} = AV_{DD} = 2.7$ to $3.3\text{V}$	$AV_{DD} - 0.3$			V
Analog input voltage	$V_{IAN}$	AN0 to AN11		0			V
AVREF current	$I_{REF}$	$AV_{REF}$	Operation mode		0.4	0.7	mA
	$I_{REFS}$		Sleep mode Stop mode 32kHz operation mode			10	$\mu\text{A}$

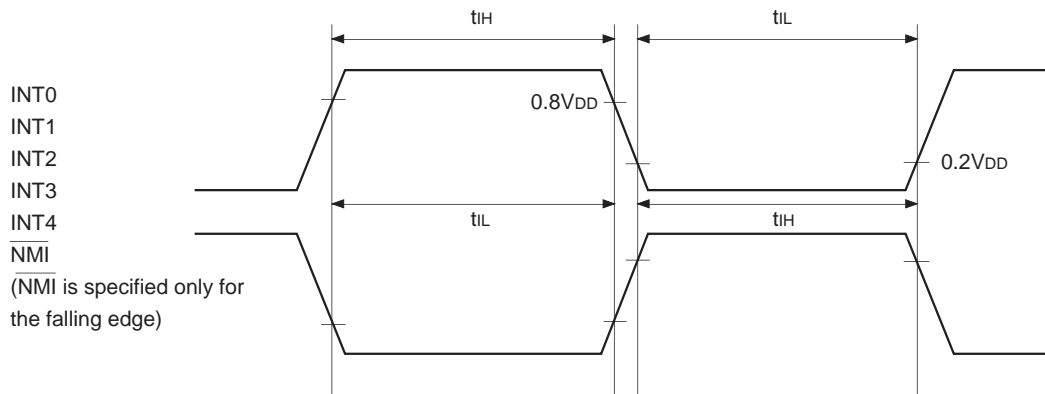


- \*1  $V_{ZT}$ : Value at which the digital conversion value changes from 00h to 01h and vice versa.
- \*2  $V_{FT}$ : Value at which the digital conversion value changes from FEh to FFh and vice versa.
- \*3  $f_{ADC}$  indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 000F9h).  
 PS3 selected  $f_{ADC} = f_c/4$   
 PS4 selected  $f_{ADC} = f_c/8$   
 However, when PS3 is selected,  $f_c$  is 12MHz or less.
- \*4 Sub clock operated  $t_{CONV} = 34/f_{TEX}$   
 $t_{SAMP} = 10/f_{TEX}$

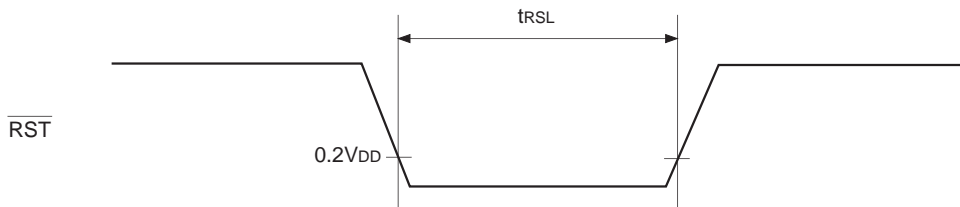
**Fig. 6. Definition of A/D converter terms**

**(4) Interruption, reset input** (Ta = -20 to +75°C, VDD = 2.7 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption High and Low level widths	t <sub>IH</sub> t <sub>IL</sub>	INT0 INT1 INT2 INT3 INT4 NMI		1		μs
Reset input Low level width	t <sub>RSL</sub>	$\overline{\text{RST}}$		32/f <sub>c</sub>		μs



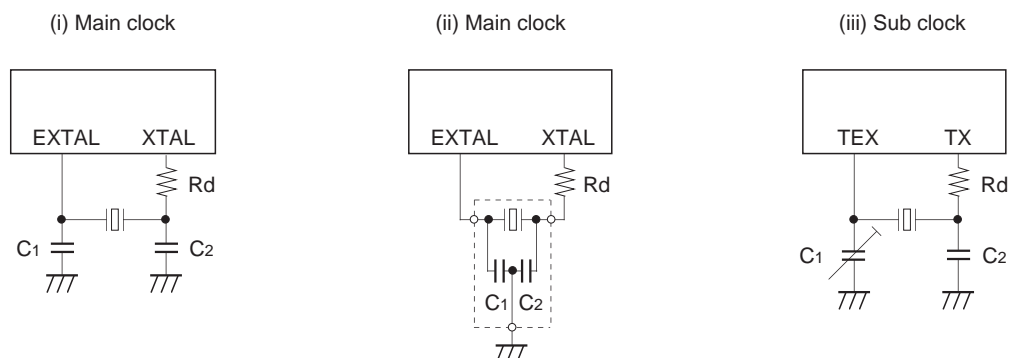
**Fig. 7. Interruption input timing**



**Fig. 8.  $\overline{\text{RST}}$  input timing**

Appendix

Fig. 9. Recommended oscillation circuit

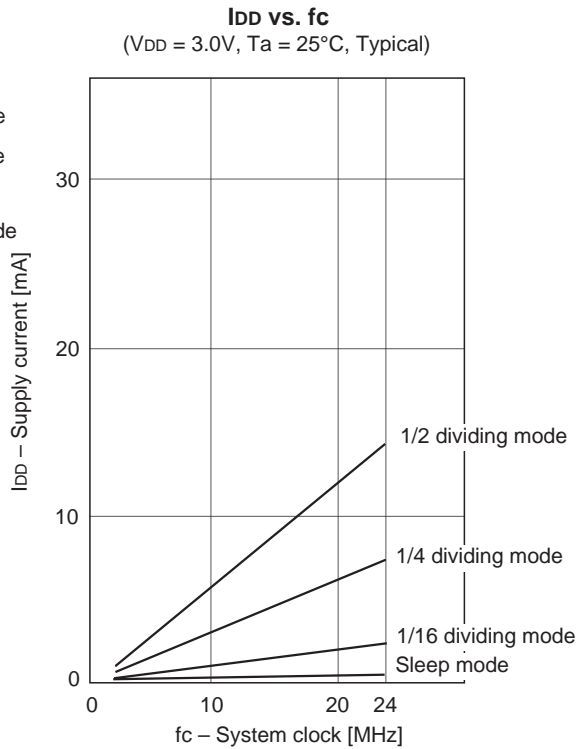
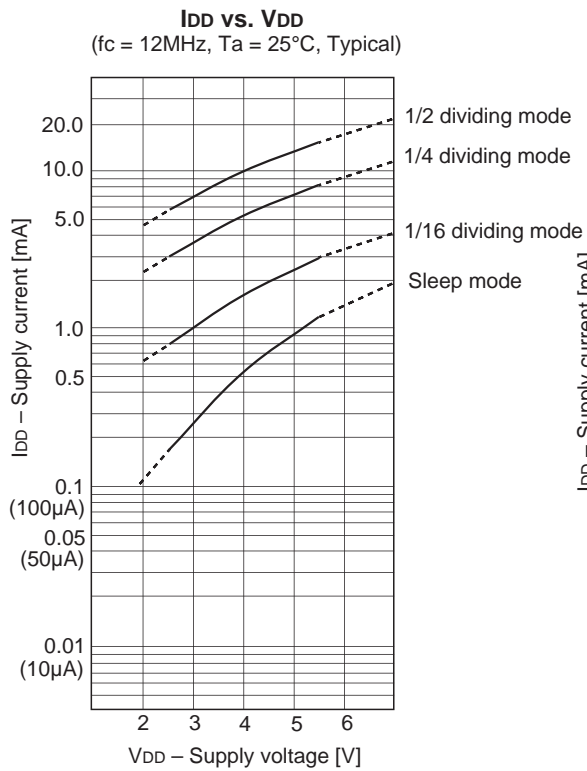
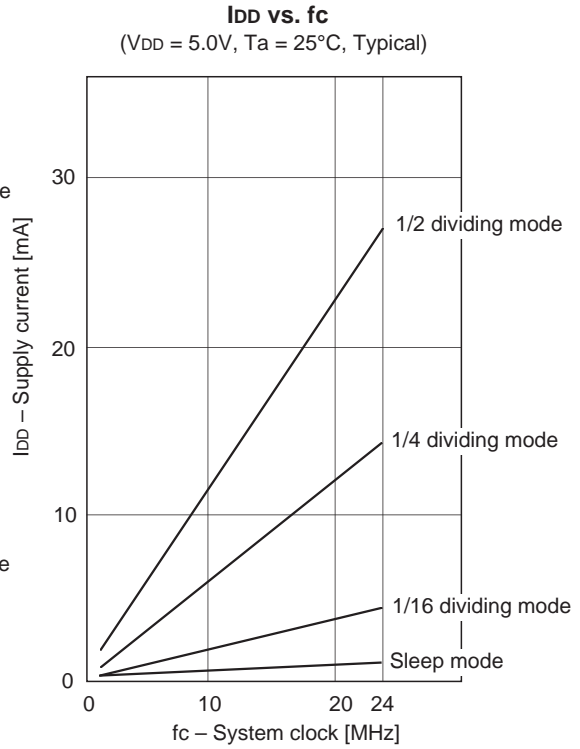
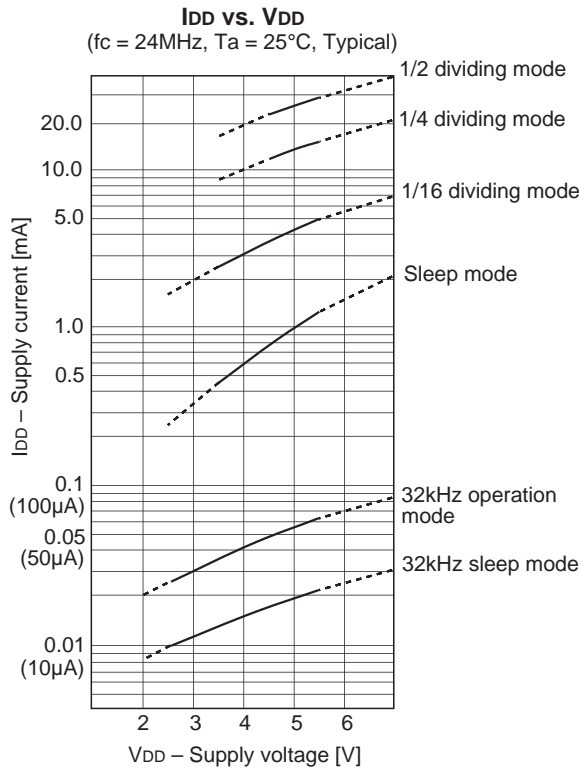


Manufacturer	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd ( $\Omega$ )	Circuit example	Remarks
MURATA MFG CO., LTD.	CSA10.0MTZ	10.0	30	30	0*1	(i)	
	CSA12.0MTZ	12.0					
	CSA16.00MXZ040	16.0	5	5			
	CST10.0MTW*	10.0	30	30		(ii)	
	CST12.0MTW*	12.0					
	CST16.00MXW0C1*	16.0	5	5			
RIVER ELETEC CO., LTD.	HC-49/U03	8.0	18	18	330*1	(i)	
		12.0	12	12			
		16.0	10	10			
KINSEKI LTD.	HC-49/U (-S)	8.0	10	10	0*1	(i)	
		12.0	5	5			
		16.0	Open	Open			
	P3	32.768kHz	30	33	120k	(iii)	
Seiko Instruments Inc.	VTC-200 SP-T	32.768kHz	18	18	330k	(iii)	CL = 12.5pF

\* Indicates types with on-chip grounding capacitor (C1, C2).

\*1 XTAL series resistor (Rd = 500 $\Omega$  or less) is hard to affect noise by ESD.

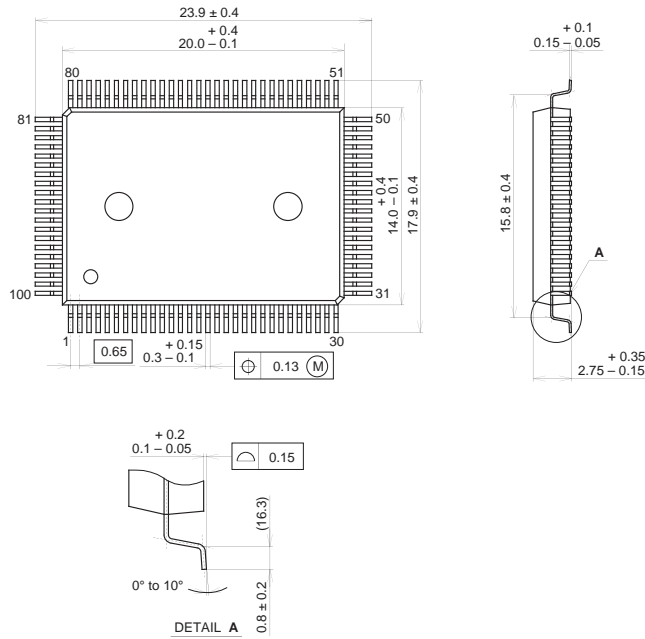
Characteristics Curve



Package Outline

Unit: mm

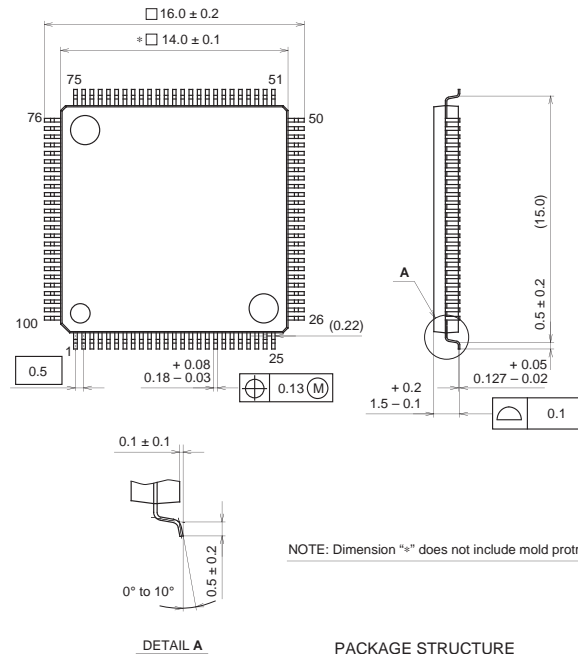
100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	

PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN LQFP (PLASTIC)



NOTE: Dimension "\*" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	LQFP100-P-1414
JEDEC CODE	

PACKAGE STRUCTURE	
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.8g