SONY

# CXD2597Q

## CD Digital Signal Processor with Built-in Digital Servo and DAC

### Description

The CXD2597Q is a digital signal processor LSI for CD players. This LSI incorporates a digital servo, digital filter, zero detection circuit, 1-bit DAC and analog low-pass filter on a single chip.

### Features

Digital Signal Processor (DSP) Block

- Playback mode supporting CAV (Constant Angular Velocity)
  - Frame jitter free
  - 0.5× to 4× continuous playback possible
  - Allows relative rotational velocity readout
- Wide capture range playback mode
  - Spindle rotational velocity following method
  - Supports normal-speed to 4× speed playback
- 16K RAM
- EFM data demodulation
- Enhanced EFM frame sync signal protection
- SEC strategy-based error correction
- Subcode demodulation and Sub Q data error detection
- Digital spindle servo
- 16-bit traverse counter
- Asymmetry correction circuit
- CPU interface on serial bus
- Error correction monitor signal, etc. output from a new CPU interface
- Servo auto sequencer
- Digital audio interface outputs
- Digital level meter, peak meter
- CD TEXT data demodulation

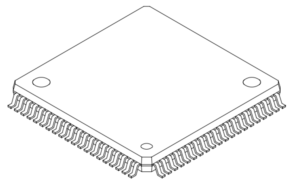
Digital Servo (DSSP) Block

- Microcomputer software-based flexible servo control
- Offset cancel function for servo error signal
- Auto gain control function for servo loop
- E:F balance, focus bias adjustment functions

Digital Filter, DAC and Analog Low-Pass Filter Blocks

- DBB (digital bass boost) function
- Double-speed playback supported
- Digital de-emphasis
- Digital attenuation
- Zero detection function
- 8Fs oversampling digital filter
- S/N: 100dB or more (master clock: 384Fs, typ.) Logical value: 109dB
- THD + N: 0.007% or less (master clock: 384Fs, typ.)
- Rejection band attenuation: –60dB or less

80 pin QFP (Plastic)



### Applications

CD players

### Structure

Silicon gate CMOS IC

### Absolute Maximum Ratings

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD}$ | –0.3 to +7.0 | V |
| • Input voltage | $V_I$ | –0.3 to +7.0 | V |
| | | ($V_{SS}$ – 0.3V to $V_{DD}$ + 0.3) | |
| • Output voltage | $V_O$ | –0.3 to +7.0 | V |
| • Storage temperature | Tstg | –40 to +125 | °C |
| • Supply voltage difference | | | |
| | $V_{SS}$ – $AV_{SS}$ | –0.3 to +0.3 | V |
| | $V_{DD}$ – $AV_{DD}$ | –0.3 to +0.3 | V |

**Note)** $AV_{DD}$ includes $XV_{DD}$ and $AV_{SS}$ includes $XV_{SS}$.

### Recommended Operating Conditions

| | | | |
|---|---|---|---|
| • Supply voltage | $V_{DD}$ | +2.7 to +5.5 | V |
| • Operating temperature | Topr | –20 to +75 | °C |

**Note)** The $V_{DD}$ for the CXD2597Q varies according to the playback speed selection.

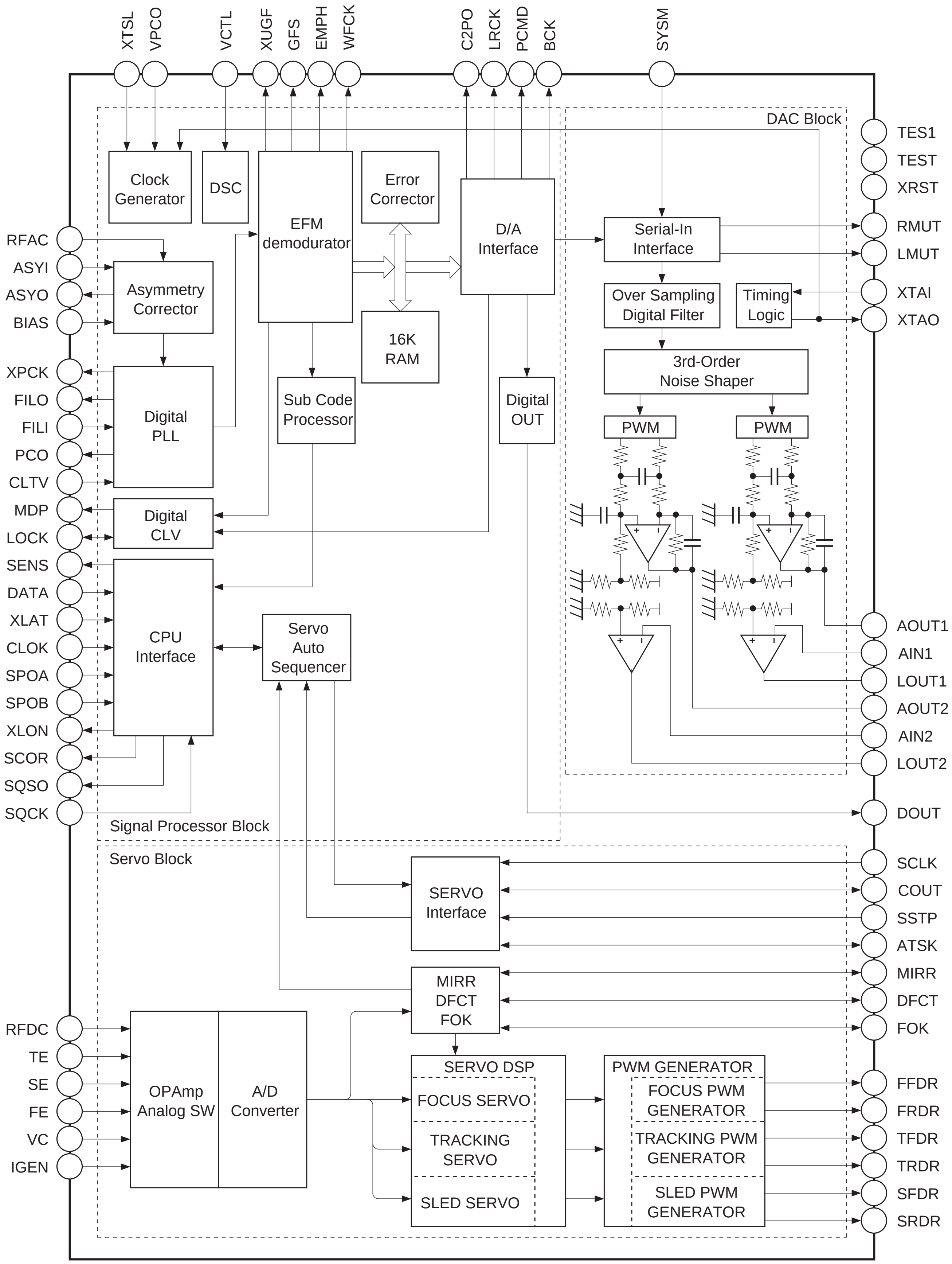
| Playback speed | $V_{DD}$ [V] | |
|---|---|---|
| | CD-DSP block | DAC block |
| 4× | 4.75 to 5.25 | |
| 2× | 3.0 to 5.5 | 4.5 to 5.5 |
| 1× | 2.7 to 5.5 | 2.7 to 5.5 |

### I/O Capacitance

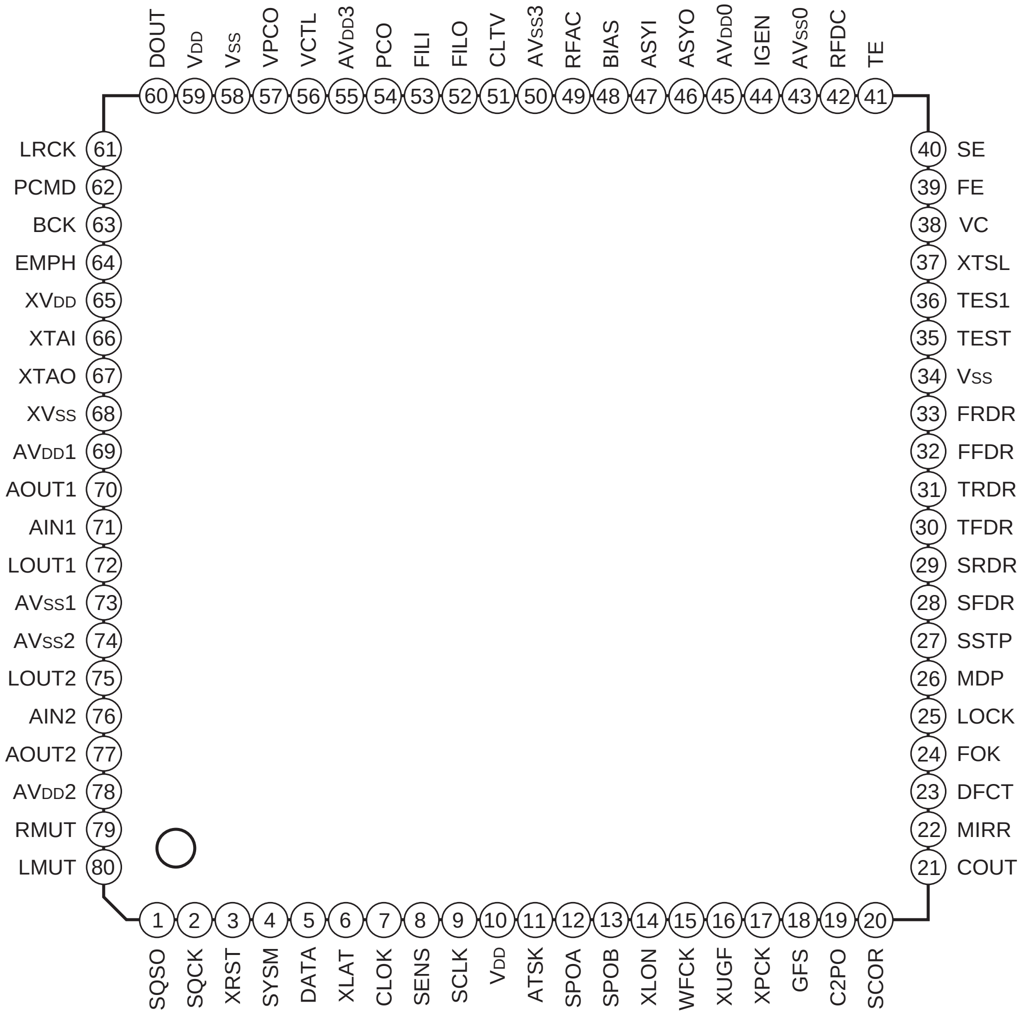
| | | | |
|---|---|---|---|
| • Input capacitance | $C_I$ | 11 (Max.) | pF |
| • Output capacitance | $C_O$ | 11 (Max.) | pF |
| • I/O capacitance | $C_{I/O}$ | 11 (Max.) | pF |

**Note)** Measurement conditions $V_{DD}$ = $V_I$ = 0V
$f_M$ = 1MHz

## Block Diagram



**Pin Configuration**



### Pin Description

| Pin No. | Symbol | I/O | | Description |
|---|---|---|---|---|
| 1 | SQSO | O | 1, 0 | Sub Q 80-bit, PCM peak and level data outputs. CD TEXT data output. |
| 2 | SQCK | I | | SQSO readout clock input. |
| 3 | XRST | I | | System reset. Reset when low. |
| 4 | SYSM | I | | Mute input. Muted when high. |
| 5 | DATA | I | | Serial data input from CPU. |
| 6 | XLAT | I | | Latch input from CPU. Serial data is latched at the falling edge. |
| 7 | CLOK | I | | Serial data transfer clock input from CPU. |
| 8 | SENS | O | 1, 0 | SENS output to CPU. |
| 9 | SCLK | I | | SENS serial data readout clock input. |
| 10 | $V_{DD}$ | — | — | Digital power supply. |
| 11 | ATSK | I/O | 1, 0 | Anti-shock input/output. |
| 12 | SPOA | I | | Microcomputer extension interface (input A) |
| 13 | SPOB | I | | Microcomputer extension interface (input B) |
| 14 | XLON | O | 1, 0 | Microcomputer extension interface (output) |
| 15 | WFCK | O | 1, 0 | WFCK output. |
| 16 | XUGF | O | 1, 0 | XUGF output. MINT1 or RFCK is output by switching with the command. |
| 17 | XPCK | O | 1, 0 | XPCK output. MNT0 is output by switching with the command. |
| 18 | GFS | O | 1, 0 | GFS output. MNT3 or XROF is output by switching with the command. |
| 19 | C2PO | O | 1, 0 | C2PO output. GTOP is output by switching with the command. |
| 20 | SCOR | O | 1, 0 | Outputs a high signal when either subcode sync S0 or S1 is detected. |
| 21 | COUT | I/O | 1, 0 | Track count signal input/output. |
| 22 | MIRR | I/O | 1, 0 | Mirror signal input/output. |
| 23 | DFCT | I/O | 1, 0 | Defect signal input/output. |
| 24 | FOK | I/O | 1, 0 | Focus OK signal input/output. |
| 25 | LOCK | I/O | 1, 0 | GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low. Or input when LKIN = 1. |
| 26 | MDP | O | 1, Z, 0 | Spindle motor servo control output. |
| 27 | SSTP | I | | Disc innermost track detection signal input. |
| 28 | SFDR | O | 1, 0 | Sled drive output. |
| 29 | SRDR | O | 1, 0 | Sled drive output. |
| 30 | TFDR | O | 1, 0 | Tracking drive output. |
| 31 | TRDR | O | 1, 0 | Tracking drive output. |
| 32 | FFDR | O | 1, 0 | Focus drive output. |
| 33 | FRDR | O | 1, 0 | Focus drive output. |
| 34 | $V_{SS}$ | — | — | Digital GND. |
| 35 | TEST | I | | Test pin. Normally, GND. |

| Pin No. | Symbol | I/O | | Description |
|---|---|---|---|---|
| 36 | TES1 | I | | Test pin. Normally, GND. |
| 37 | XTSL | I | | Crystal selection input. Low when the crystal is 16.9344MHz; high when the crystal is 33.8688MHz. |
| 38 | VC | I | | Center voltage input. |
| 39 | FE | I | | Focus error signal input. |
| 40 | SE | I | | Sled error signal input. |
| 41 | TE | I | | Tracking error signal input. |
| 42 | RFDC | I | | RF signal input. |
| 43 | AV$_{SS}$0 | — | — | Analog GND. |
| 44 | IGEN | I | | Operational amplifier constant current input. |
| 45 | AV$_{DD}$0 | — | — | Analog power supply. |
| 46 | ASYO | O | 1, 0 | EFM full-swing output. (low = Vss, high = V$_{DD}$) |
| 47 | ASYI | I | | Asymmetry comparator voltage input. |
| 48 | BIAS | I | | Asymmetry circuit constant current input. |
| 49 | RFAC | I | | EFM signal input. |
| 50 | AV$_{SS}$3 | — | — | Analog GND. |
| 51 | CLTV | I | | Multiplier VCO1 control voltage input. |
| 52 | FILO | O | Analog | Master PLL filter output. (slave = digital PLL) |
| 53 | FILI | I | | Master PLL filter input. |
| 54 | PCO | O | 1, Z, 0 | Master PLL charge pump output. |
| 55 | AV$_{DD}$3 | — | — | Analog power supply. |
| 56 | VCTL | I | | Wide-band EFM PLL VCO2 control voltage input. |
| 57 | VPCO | O | 1, Z, 0 | Wide-band EFM PLL charge pump output. |
| 58 | V$_{SS}$ | — | — | Digital GND. |
| 59 | V$_{DD}$ | — | — | Digital power supply. |
| 60 | DOUT | O | 1, 0 | Digital Out output. |
| 61 | LRCK | O | 1, 0 | D/A interface. LR clock output f = Fs. |
| 62 | PCMD | O | 1, 0 | D/A interface. Serial data output. (two's complement, MSB first) |
| 63 | BCK | O | 1, 0 | D/A interface. Bit clock output. |
| 64 | EMPH | O | 1, 0 | Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis. |
| 65 | XV$_{DD}$ | — | — | Master clock power supply. |
| 66 | XTAI | I | | Crystal oscillation circuit input. Master clock is externally input from this pin. |
| 67 | XTAO | O | | Crystal oscillation circuit output. |
| 68 | XV$_{SS}$ | — | — | Master clock GND. |
| 69 | AV$_{DD}$1 | — | — | Analog power supply. |
| 70 | AOUT1 | O | | L ch analog output. |
| 71 | AIN1 | I | | L ch operational amplifier input. |

| Pin No. | Symbol | I/O | | Description |
|---|---|---|---|---|
| 72 | LOUT1 | O | | L ch LINE output. |
| 73 | $AV_{SS}1$ | — | — | Analog GND. |
| 74 | $AV_{SS}2$ | — | — | Analog GND. |
| 75 | LOUT2 | O | | R ch LINE output. |
| 76 | AIN2 | I | | R ch operational amplifier output. |
| 77 | AOUT2 | O | | R ch analog output. |
| 78 | $AV_{DD}2$ | — | — | Analog power supply. |
| 79 | RMUT | O | 1, 0 | R ch zero detection flag. |
| 80 | LMUT | O | 1, 0 | L ch zero detection flag. |

**Notes)**
- PCMD is a MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window opens.)
- XUGF is the frame sync obtained from the EFM signal, and is negative pulse. It is the signal before sync protection.
- XPCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- The GFS signal goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136µs.
- C2PO represents the data error status.
- XROF is generated when the 16K RAM exceeds the ±4F jitter margin.

**Monitor Pin Output Combinations**

| Command bit | | Output data | | | |
|---|---|---|---|---|---|
| MTSL1 | MTSL0 | | | | |
| 0 | 0 | XUGF | XPCK | GFS | C2PO |
| 0 | 1 | MNT1 | MNT0 | MNT3 | C2PO |
| 1 | 0 | RFCK | XPCK | XROF | GTOP |

## Electrical Characteristics

### 1. DC Characteristics

($V_{DD} = AV_{DD} = 5.0V \pm 5\%$, $V_{SS} = AV_{SS} = 0V$, Topr = –20 to +75°C)

| Item | | | Conditions | Min. | Typ. | Max. | Unit | Applicable pins |
|---|---|---|---|---|---|---|---|---|
| Input voltage (1) | High level input voltage | $V_{IH}$ (1) | | $0.7V_{DD}$ | | | V | *1, *9 |
| | Low level input voltage | $V_{IL}$ (1) | | | | $0.3V_{DD}$ | V | |
| Input voltage (2) | High level input voltage | $V_{IH}$ (2) | Schmitt input | $0.8V_{DD}$ | | | V | *2, *10 |
| | Low level input voltage | $V_{IL}$ (2) | | | | $0.2V_{DD}$ | V | |
| Input voltage (3) | Input voltage | $V_{IN}$ (3) | Analog input | Vss | | $V_{DD}$ | V | *3, *7, *8 |
| Output voltage (1) | High level output voltage | $V_{OH}$ (1) | $I_{OH}$ = –2mA | $V_{DD}$ – 0.8 | | $V_{DD}$ | V | *4 |
| | Low level output voltage | $V_{OL}$ (1) | $I_{OL}$ = 4mA | Vss | | 0.4 | V | |
| Output voltage (2) | High level output voltage | $V_{OH}$ (2) | $I_{OH}$ = –6mA | $V_{DD}$ – 0.8 | | $V_{DD}$ | V | *5 |
| | Low level output voltage | $V_{OL}$ (2) | $I_{OL}$ = 4mA | Vss | | 0.4 | V | |
| Output voltage (3) | High level output voltage | $V_{OH}$ (3) | $I_{OH}$ = –0.28mA | $V_{DD}$ – 0.5 | | $V_{DD}$ | V | *6 |
| | Low level output voltage | $V_{OL}$ (3) | $I_{OL}$ = 0.36mA | Vss | | 0.4 | V | |
| Input leak current (1) | | $I_{LI}$ (1) | $V_{IN}$ = $V_{SS}$ or $V_{DD}$ | –10 | | 10 | µA | *1, *2 |
| Input leak current (2) | | $I_{LI}$ (2) | $V_{IN}$ = $V_{SS}$ or $V_{DD}$ | –40 | | 40 | µA | *9, *10 |
| Input leak current (3) | | $I_{LI}$ (3) | $V_I$ = 1.5 to 3.5V | –20 | | 20 | µA | *7 |
| Input leak current (4) | | $I_{LI}$ (4) | $V_I$ = 0 to 5.0V | –40 | | 600 | µA | *8 |

**Applicable pins**

*1 SYSM, DATA, XLAT, SSTP, XTSL, TEST, TES1
*2 SQCK, XRST, CLOK
*3 ASYI, RFAC, CLTV, FILI, VCTL
*4 SQSO, SENS, ATSK, XLON, WFCK, XUGF, XPCK, GFS, C2PO, SCOR, COUT, MIRR, DFCT, FOK, LOCK, SFDR, SRDR, TFDR, TRDR, FFDR, FRDR, ASYO, DOUT, LRCK, PCMD, BCK, EMPH, RMUT, LMUT
*5 MDP, PCO, VPCO
*6 FILO
*7 VC, FE, SE, TE
*8 RFDC
*9 ATSK, COUT, MIRR, DFCT, FOK, LOCK
*10 SCLK, SPOA, SPOB

## 2. AC Characteristics

### (1) XTAI pin

(a) When using self-excited oscillation

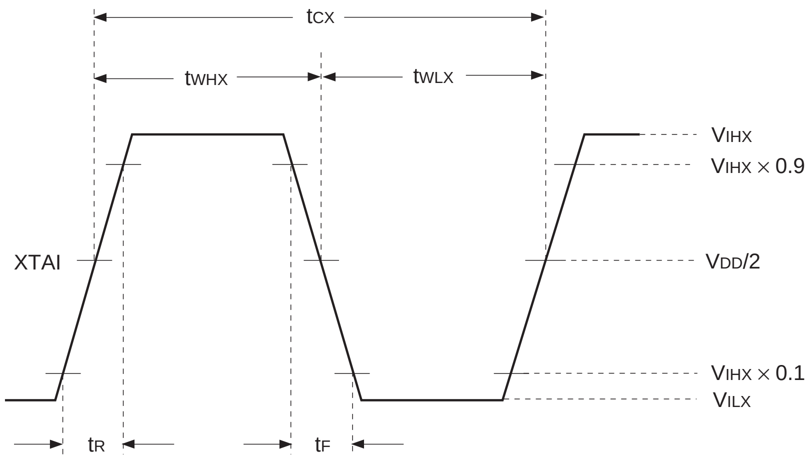
(Topr = –20 to +75°C, $V_{DD}$ = $AV_{DD}$ = 5.0V ± 5%)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Oscillation frequency | $f_{MAX}$ | 7 | | 34 | MHz |

(b) When inputting pulses to XTAI pin

(Topr = –20 to +75°C, $V_{DD}$ = $AV_{DD}$ = 5.0V ± 5%)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| High level pulse width | $t_{WHX}$ | 13 | | 500 | ns |
| Low level pulse width | $t_{WLX}$ | 13 | | 500 | ns |
| Pulse cycle | $t_{CK}$ | 26 | | 1,000 | ns |
| Input high level | $V_{IHX}$ | $V_{DD}$ – 1.0 | | | V |
| Input low level | $V_{ILX}$ | | | 0.8 | V |
| Rise time, fall time | $t_R$, $t_F$ | | | 10 | ns |




(c) When inputting sine waves to XTAI pin via a capacitor

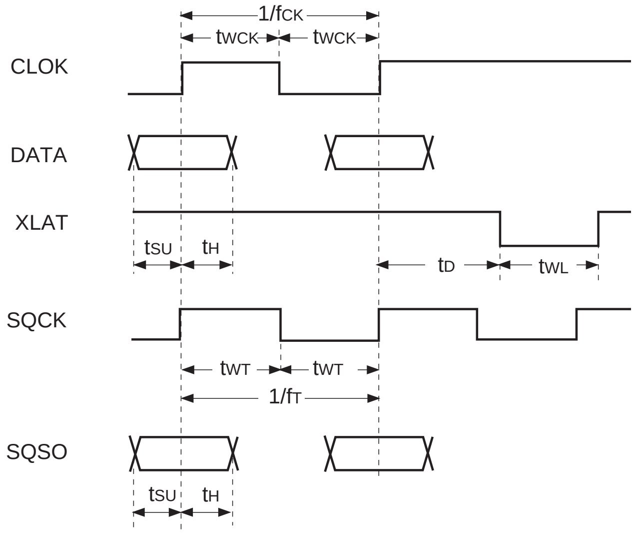
(Topr = –20 to +75°C, $V_{DD}$ = $AV_{DD}$ = 5.0V ± 5%)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input amplitude | $V_I$ | 2.0 | | $V_{DD}$ + 0.3 | Vp-p |

(2) CLOK, DATA, XLAT and SQCK pin

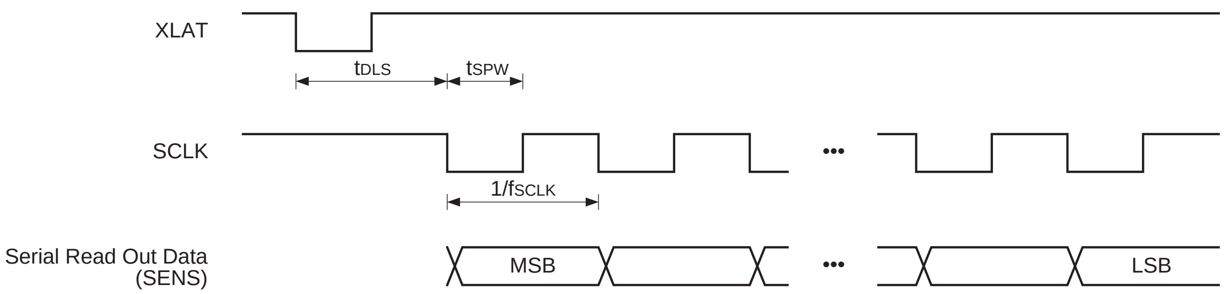
($V_{DD}$ = $AV_{DD}$ = 5.0V ± 5%, $V_{SS}$ = $AV_{SS}$ = 0V, Topr = –20 to +75°C)

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Clock frequency | $f_{CK}$ | | | 0.65 | MHz |
| Clock pulse width | $t_{WCK}$ | 750 | | | ns |
| Setup time | $t_{SU}$ | 300 | | | ns |
| Hold time | $t_H$ | 300 | | | ns |
| Delay time | $t_D$ | 300 | | | ns |
| Latch pulse width | $t_{WL}$ | 750 | | | ns |
| SQCK frequency | $f_T$ | | | 0.65 **Note)** | MHz |
| SQCK pulse width | $t_{WT}$ | 750 **Note)** | | | ns |




**Note)** In quasi double-speed playback mode, except when SQSO is Sub Q Read, the SQCK maximum operating frequency is 300kHz and its minimum pulse width is 1.5µs.

(3) SCLK pin




| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| SCLK frequency | $f_{SCLK}$ | | | 16 | MHz |
| SCLK pulse width | $t_{SPW}$ | 31.3 | | | ns |
| Delay time | $t_{DLS}$ | 15 | | | µs |

(4) COUT, MIRR and DFCT pins

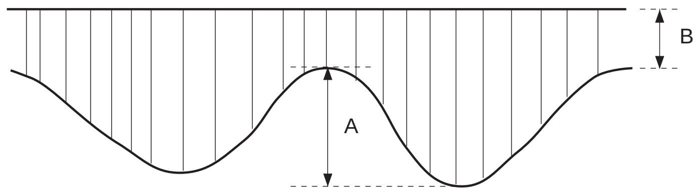
**Operating frequency**

($V_{DD} = AV_{DD} = 5.0V \pm 5\%$, $V_{SS} = AV_{SS} = 0V$, Topr = –20 to +75°C)

| Item | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| COUT maximum operating frequency | $f_{COUT}$ | 40 | | | kHz | *1 |
| MIRR maximum operating frequency | $f_{MIRR}$ | 40 | | | kHz | *2 |
| DFCT maximum operating frequency | $f_{DFCTH}$ | 5 | | | kHz | *3 |

*1 When using a high-speed traverse TZC.

*2




When the RF signal continuously satisfies the following conditions during the above traverse.

- $A = 0.12V_{DD}$ to $0.26V_{DD}$
- $\dfrac{B}{A + B} \leq 25\%$

*3 During complete RF signal omission.
When settings related to DFCT signal generation are Typ.

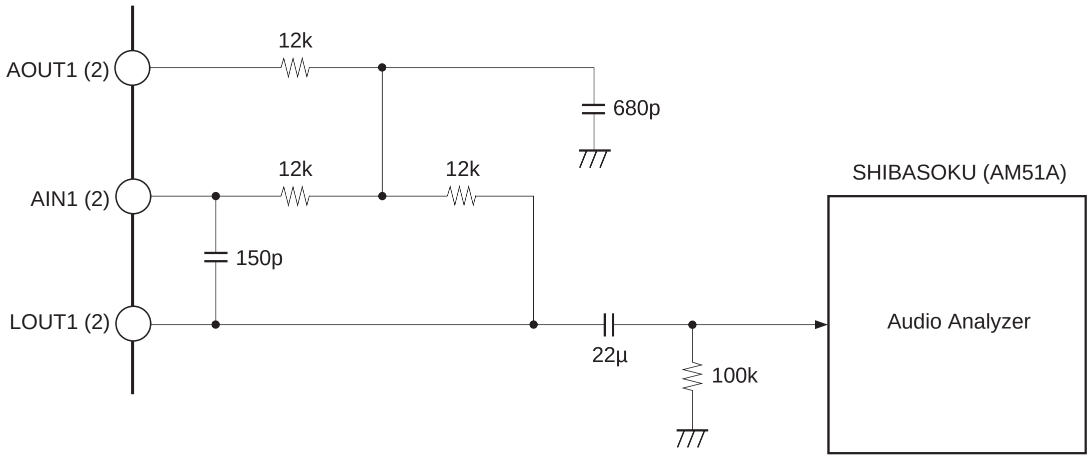
### 1-bit DAC and LPF Block Analog Characteristics

Analog characteristics ($V_{DD} = AV_{DD} = 5.0V$, $V_{SS} = AV_{SS} = 0V$, Ta = 25°C)

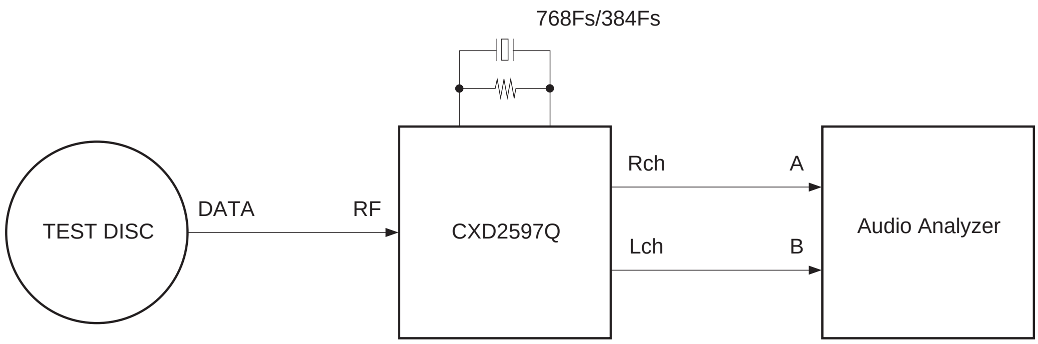
| Item | Symbol | Conditions | Crystal | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Total harmonic distortion | THD | 1kHz, 0dB data | 384Fs | | 0.0050 | 0.0070 | % |
| | | | 768Fs | | 0.0045 | 0.0065 | |
| Signal-to-noise ratio | S/N | 1kHz, 0dB data (Using A-weighting filter) | 384Fs | 96 | 100 | | dB |
| | | | 768Fs | 96 | 100 | | |

Fs = 44.1kHz in all cases.

The total harmonic distortion and signal-to-noise ratio measurement circuits are shown below.




**LPF external circuit diagram**




**Block diagram of analog characteristics measurement**

($V_{DD} = AV_{DD} = 5.0V$, $V_{SS} = AV_{SS} = 0V$, Topr = –20 to +75°C)

| Item | Symbol | Min. | Typ. | Max. | Unit | Applicable pins |
|---|---|---|---|---|---|---|
| Output voltage | $V_{OUT}$ | | 1.12 | | Vrms | *1 |
| Load resistance | $R_L$ | 8 | | | kΩ | *1 |

* Measurement is conducted for the LPF external circuit diagram with the sine wave output of 1kHz and 0dB.

**Applicable pins**

*1 LOUT1, LOUT2

## Contents



Explanation of abbreviations

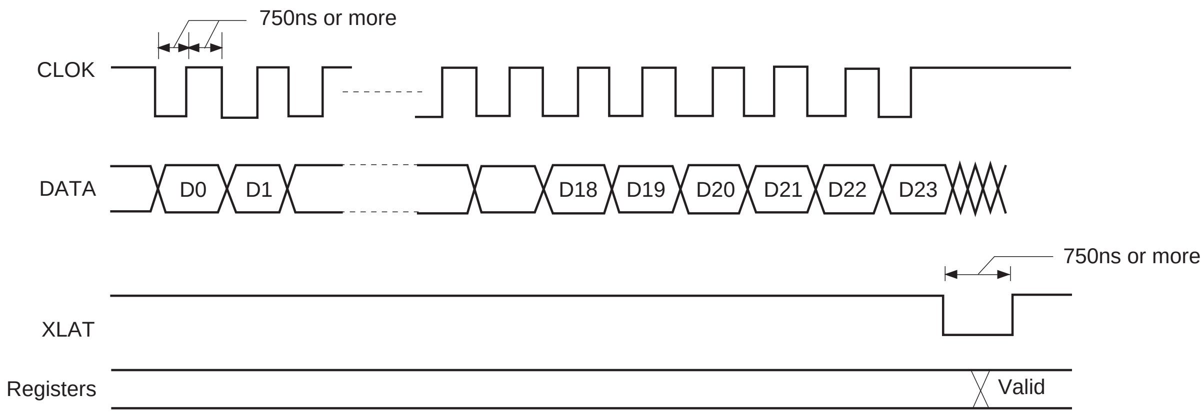
| | |
|---|---|
| AVRG: | Average |
| AGCNTL: | Auto gain control |
| FCS: | Focus |
| TRK: | Tracking |
| SLD: | Sled |
| DFCT: | Defect |

## §1. CPU Interface

### §1-1. CPU Interface Timing

• CPU interface

This interface uses DATA, CLOK and XLAT to set the modes.
The interface timing chart is shown below.




• The internal registers are initialized by a reset when XRST = 0.

**Note)** Be sure to set SQCK to high when XLAT is low.

### §1-2. CPU Interface Command Table

Total bit length for each register

| Register | Total bit length |
|---|---|
| 0 to 2 | 8 bits |
| 3 | 8 to 24 bits |
| 4 to 6 | 8 bits |
| 7 | 20 bits |
| 8 | 28 bits |
| 9 | 24 bits |
| A | 28 bits |
| B | 16 bits |
| C | 8 bits |
| D | 16 bits |
| E | 20 bits |

## Command Table ($0X to 1X)

| Register | Command | Address | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | FOCUS CONTROL | 0 0 0 0 | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SERVO ON (FOCUS GAIN NORMAL) |
| | | | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SERVO ON (FOCUS GAIN DOWN) |
| | | | 0 | — | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SERVO OFF, 0V OUT |
| | | | 0 | — | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT |
| | | | 0 | — | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SEARCH VOLTAGE DOWN |
| | | | 0 | — | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SEACH VOLTAGE UP |
| 1 | TRACKING CONTROL | 0 0 0 1 | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ANTI SHOCK ON |
| | | | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ANTI SHOCK OFF |
| | | | — | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | BRAKE ON |
| | | | — | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | BRAKE OFF |
| | | | — | — | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING GAIN NORMAL |
| | | | — | — | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING GAIN UP |
| | | | — | — | — | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING GAIN UP FILTER SELECT 1 |
| | | | — | — | — | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING GAIN UP FILTER SELECT 2 |

—: Don't care

**Command Table ($2X to 3X)**

| Register | Command | Address | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 2 | TRACKING MODE | 0 0 1 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING SERVO OFF |
| | | | 0 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING SERVO ON |
| | | | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FORWARD TRACK JUMP |
| | | | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | REVERSE TRACK JUMP |
| | | | — | — | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED SERVO OFF |
| | | | — | — | 0 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED SERVO ON |
| | | | — | — | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FORWARD SLED MOVE |
| | | | — | — | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | REVERSE SLED MOVE |

| Register | Command | Address | | | Data 1 | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED KICK LEVEL (±1 × basic value) (Default) |
| | | | 0 | 0 | 0 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED KICK LEVEL (±2 × basic value) |
| | | | 0 | 0 | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED KICK LEVEL (±3 × basic value) |
| | | | 0 | 0 | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED KICK LEVEL (±4 × basic value) |

—: Don't care

**Command Table ($340X)**

| Register | Command | Address 1 | Address 2 | Address 3 | Address 4 | | | | Data 1 | | | | Data 2 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D23 to D20 | D19 to D16 | D15 to D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 0 0 0 0 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K00) SLED INPUT GAIN |
| | | | | | 0 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K01) SLED LOW BOOST FILTER A-H |
| | | | | | 0 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K02) SLED LOW BOOST FILTER A-L |
| | | | | | 0 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K03) SLED LOW BOOST FILTER B-H |
| | | | | | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K04) SLED LOW BOOST FILTER B-L |
| | | | | | 0 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K05) SLED OUTPUT GAIN |
| | | | | | 0 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K06) FOCUS INPUT GAIN |
| | | | | | 0 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K07) SLED AUTO GAIN |
| | | | | | 1 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K08) FOCUS HIGH CUT FILTER A |
| | | | | | 1 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K09) FOCUS HIGH CUT FILTER B |
| | | | | | 1 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0A) FOCUS LOW BOOST FILTER A-H |
| | | | | | 1 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0B) FOCUS LOW BOOST FILTER A-L |
| | | | | | 1 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0C) FOCUS LOW BOOST FILTER B-H |
| | | | | | 1 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0D) FOCUS LOW BOOST FILTER B-L |
| | | | | | 1 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0E) FOCUS PHASE COMPENSATE FILTER A |
| | | | | | 1 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K0F) FOCUS DEFECT HOLD GAIN |

## Command Table ($341X)

| Register | Command | Address 1 | Address 2 | Address 3 | Address 4 | | | | Data 1 | | | | Data 2 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D23 to D20 | D19 to D16 | D15 to D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 0 0 0 1 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K10)<br>FOCUS PHASE COMPENSATE FILTER B |
| | | | | | 0 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K11)<br>FOCUS OUTPUT GAIN |
| | | | | | 0 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K12)<br>ANTI SHOCK INPUT GAIN |
| | | | | | 0 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K13)<br>FOCUS AUTO GAIN |
| | | | | | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K14)<br>HPTZC / AUTO GAIN HIGH PASS FILTER A |
| | | | | | 0 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K15)<br>HPTZC / AUTO GAIN HIGH PASS FILTER B |
| | | | | | 0 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K16)<br>ANTI SHOCK HIGH PASS FILTER A |
| | | | | | 0 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K17)<br>HPTZC / AUTO GAIN LOW PASS FILTER B |
| | | | | | 1 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K18)<br>FIX |
| | | | | | 1 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K19)<br>TRACKING INPUT GAIN |
| | | | | | 1 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K1A)<br>TRACKING HIGH CUT FILTER A |
| | | | | | 1 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K1B)<br>TRACKING HIGH CUT FILTER B |
| | | | | | 1 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K1C)<br>TRACKING LOW BOOST FILTER A-H |
| | | | | | 1 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K1D)<br>TRACKING LOW BOOST FILTER A-L |
| | | | | | 1 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K1E)<br>TRACKING LOW BOOST FILTER B-H |
| | | | | | 1 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K1F)<br>TRACKING LOW BOOST FILTER B-L |

## Command Table ($342X)

| Register | Command | Address 1 | Address 2 | Address 3 | Address 4 | | | | Data 1 | | | | Data 2 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D23 to D20 | D19 to D16 | D15 to D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 0 0 1 0 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K20)<br>TRACKING PHASE COMPENSATE FILTER A |
| | | | | | 0 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K21)<br>TRACKING PHASE COMPENSATE FILTER B |
| | | | | | 0 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K22)<br>TRACKING OUTPUT GAIN |
| | | | | | 0 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K23)<br>TRACKING AUTO GAIN |
| | | | | | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K24)<br>FOCUS GAIN DOWN HIGH CUT FILTER A |
| | | | | | 0 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K25)<br>FOCUS GAIN DOWN HIGH CUT FILTER B |
| | | | | | 0 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K26)<br>FOCUS GAIN DOWN LOW BOOST FILTER A-H |
| | | | | | 0 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K27)<br>FOCUS GAIN DOWN LOW BOOST FILTER A-L |
| | | | | | 1 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K28)<br>FOCUS GAIN DOWN LOW BOOST FILTER B-H |
| | | | | | 1 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K29)<br>FOCUS GAIN DOWN LOW BOOST FILTER B-L |
| | | | | | 1 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K2A)<br>FOCUS GAIN DOWN PHASE COMPENSATE FILTER A |
| | | | | | 1 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K2B)<br>FOCUS GAIN DOWN DEFECT HOLD GAIN |
| | | | | | 1 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K2C)<br>FOCUS GAIN DOWN PHASE COMPENSATE FILTER B |
| | | | | | 1 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K2D)<br>FOCUS GAIN DOWN OUTPUT GAIN |
| | | | | | 1 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K2E)<br>NOT USED |
| | | | | | 1 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K2F)<br>NOT USED |

**Command Table ($343X)**

| Register | Command | Address 1 | Address 2 | Address 3 | Address 4 | | | | Data 1 | | | | Data 2 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D23 to D20 | D19 to D16 | D15 to D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 0 0 1 1 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K30)<br>SLED INPUT GAIN (when SFSK = 1 TG up2) |
| | | | | | 0 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K31)<br>ANTI SHOCK LOW PASS FILTER B |
| | | | | | 0 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K32)<br>NOT USED |
| | | | | | 0 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K33)<br>ANTI SHOCK HIGH PASS FILTER B-H |
| | | | | | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K34)<br>ANTI SHOCK HIGH PASS FILTER B-L |
| | | | | | 0 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K35)<br>ANTI SHOCK FILTER COMPARATE GAIN |
| | | | | | 0 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K36)<br>TRACKING GAIN UP2 HIGH CUT FILTER A |
| | | | | | 0 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K37)<br>TRACKING GAIN UP2 HIGH CUT FILTER B |
| | | | | | 1 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K38)<br>TRACKING GAIN UP2 LOW BOOST FILTER A-H |
| | | | | | 1 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K39)<br>TRACKING GAIN UP2 LOW BOOST FILTER A-L |
| | | | | | 1 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K3A)<br>TRACKING GAIN UP2 LOW BOOST FILTER B-H |
| | | | | | 1 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K3B)<br>TRACKING GAIN UP2 LOW BOOST FILTER B-L |
| | | | | | 1 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K3C)<br>TRACKING GAIN UP PHASE COMPENSATE FILTER A |
| | | | | | 1 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K3D)<br>TRACKING GAIN UP PHASE COMPENSATE FILTER B |
| | | | | | 1 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K3E)<br>TRACKING GAIN UP OUTPUT GAIN |
| | | | | | 1 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K3F)<br>NOT USED |

**Command Table ($344X)**

| Register | Command | Address 1 | Address 2 | Address 3 | Address 4 | | | | Data 1 | | | | Data 2 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D23 to D20 | D19 to D16 | D15 to D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 1 0 0 | 0 1 0 0 | 0 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K40)<br>TRACKING HOLD FILTER INPUT GAIN |
| | | | | | 0 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K41)<br>TRACKING HOLD FILTER A-H |
| | | | | | 0 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K42)<br>TRACKING HOLD FILTER A-L |
| | | | | | 0 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K43)<br>TRACKING HOLD FILTER B-H |
| | | | | | 0 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K44)<br>TRACKING HOLD FILTER B-L |
| | | | | | 0 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K45)<br>TRACKING HOLD FILTER OUTPUT GAIN |
| | | | | | 0 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K46)<br>TRACKING HOLD INPUT GAIN (when THSK = 1 TG up2) |
| | | | | | 0 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K47)<br>NOT USED |
| | | | | | 1 | 0 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K48)<br>FOCUS HOLD FILTER INPUT GAIN |
| | | | | | 1 | 0 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K49)<br>FOCUS HOLD FILTER A-H |
| | | | | | 1 | 0 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K4A)<br>FOCUS HOLD FILTER A-L |
| | | | | | 1 | 0 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K4B)<br>FOCUS HOLD FILTER B-H |
| | | | | | 1 | 1 | 0 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K4C)<br>FOCUS HOLD FILTER B-L |
| | | | | | 1 | 1 | 0 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K4D)<br>FOCUS HOLD FILTER OUTPUT GAIN |
| | | | | | 1 | 1 | 1 | 0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K4E)<br>NOT USED |
| | | | | | 1 | 1 | 1 | 1 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 | KRAM DATA (K4F)<br>NOT USED |

## Command Table ($34FX to 3FX)

| Register | Command | Address 1 | | | | | Address 2 | | | | | | Data 1 | | Data 2 | | | | Data 3 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | FBL9 | FBL8 | FBL7 | FBL6 | FBL5 | FBL4 | FBL3 | FBL2 | FBL1 | — | FOCUS BIAS LIMIT |
| | | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | FB9 | FB8 | FB7 | FB6 | FB5 | FB4 | FB3 | FB2 | FB1 | — | FOCUS BIAS DATA |
| | | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | TV9 | TV8 | TV7 | TV6 | TV5 | TV4 | TV3 | TV2 | TV1 | TV0 | TRVSC DATA |
| | | Address | | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | |
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | | 0 0 1 1 | 0 | 1 | 0 | 1 | FT1 | FT0 | FS5 | FS4 | FS3 | FS2 | FS1 | FS0 | FTZ | FG6 | FG5 | FG4 | FG3 | FG2 | FG1 | FG0 | FOCUS SEARCH SPEED/ VOLTAGE/AUTO GAIN |
| | | | 0 | 1 | 1 | 0 | TDZC | DTZC | TJ5 | TJ4 | TJ3 | TJ2 | TJ1 | TJ0 | SFJP | TG6 | TG5 | TG4 | TG3 | TG2 | TG1 | TG0 | DTZC/TRACK JUMP VOLTAGE/AUTO GAIN |
| | | | 0 | 1 | 1 | 1 | FZSH | FZSL | SM5 | SM4 | SM3 | SM2 | SM1 | SM0 | AGS | AGJ | AGGF | AGGT | AGV1 | AGV2 | AGHS | AGHT | FZSL/SLED MOVE/ Voltage/AUTO GAIN |
| | | | 1 | 0 | 0 | 0 | VCLM | VCLC | FLM | FLC0 | RFLM | RFLC | AGF | AGT | DFSW | LKSW | TBLM | TCLM | FLC1 | TLC2 | TLC1 | TLC0 | LEVEL/AUTO GAIN/ DFSW/ (Initialize) |
| | | | 1 | 0 | 0 | 1 | DAC | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SERIAL DATA READ MODE/SELECT |
| | | | 1 | 0 | 1 | 0 | 0 | FBON | FBSS | FBUP | FBV1 | FBV0 | 0 | TJD0 | FPS1 | FPS0 | TPS1 | TPS0 | 0 | SJHD | INBK | MTI0 | FOCUS BIAS |
| | | | 1 | 0 | 1 | 1 | SFO2 | SFO1 | SDF2 | SDF1 | MAX2 | MAX1 | SFOX | BTF | D2V2 | D2V1 | D1V2 | D1V1 | RINT | 0 | 0 | 0 | Operation for MIRR/ DFCT/FOK |
| | | | 1 | 1 | 0 | 0 | COSS | COTS | 0 | 0 | COT2 | COT1 | MOT2 | 0 | BTS1 | BTS0 | MRC1 | MRC0 | 0 | 0 | 0 | 0 | TZC/COUT BOTTOM/MIRR |
| | | | 1 | 1 | 0 | 1 | SFID | SFSK | THID | THSK | 0 | TLD2 | TLD1 | TLD0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLED FILTER |
| | | | 1 | 1 | 1 | 0 | F1NM | F1DM | F3NM | F3DM | T1NM | T1UM | T3NM | T3UM | DFIS | TLCD | 0 | LKIN | COIN | MDFI | MIRI | XT1D | Filter |
| | | | 1 | 1 | 1 | 1 | 0 | AGG4 | XT4D | XT2D | 0 | DRR2 | DRR1 | DRR0 | 0 | ASFG | FTQ | LPAS | SRO1 | 0 | AGHF | ASOT | Others |

—: Don't care

## Instruction Table

| Register | Command | Address D3 | Address D2 | Address D1 | Address D0 | Data 1 D3 | Data 1 D2 | Data 1 D1 | Data 1 D0 | Data 2 D3 | Data 2 D2 | Data 2 D1 | Data 2 D0 | Data 3 D3 | Data 3 D2 | Data 3 D1 | Data 3 D0 | Data 4 D3 | Data 4 D2 | Data 4 D1 | Data 4 D0 | Data 5 D3 | Data 5 D2 | Data 5 D1 | Data 5 D0 | Data 6 D3 | Data 6 D2 | Data 6 D1 | Data 6 D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 | Auto sequence | 0 | 1 | 0 | 0 | AS3 | AS2 | AS1 | AS0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 5 | Blind (A, E), Overflow (C) | 0 | 1 | 0 | 1 | 0.18ms | 0.09ms | 0.05ms | 0.02ms | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| | Brake (B) | | | | | 0.36ms | 0.18ms | 0.09ms | 0.05ms | | | | | | | | | | | | | | | | | | | | |
| 6 | KICK (D) | 0 | 1 | 1 | 0 | 11.6ms | 5.8ms | 2.9ms | 1.45ms | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 7 | Auto sequence (N) track jump count setting | 0 | 1 | 1 | 1 | 32768 | 16384 | 8192 | 4096 | 2048 | 1024 | 512 | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | — | — | — | — | — | — | — | — |
| 8 | MODE specification | 1 | 0 | 0 | 0 | CDROM | DOUT Mute | DOUT ON/OFF | WSEL | VCO SEL1 | 0 | SOCT | VCO SEL2 | KSL3 | KSL2 | KSL1 | KSL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TXON | TXOUT | OUTL1 | OUTL0 |
| 9 | Function specification | 1 | 0 | 0 | 1 | 0 | DSPB ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | OPSL1 0 | MCSL | 0 | 0 | ZDPL | ZMUT | — | — | — | — | — | — | — | — | — | — |
| | | 1 | 0 | 0 | 1 | 0 | DSPB ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | OPSL1 1 | MCSL | 0 | 0 | ZDPL | ZMUT | 0 | 0 | 0 | DCOF | 0 | 0 | — | — | — | — |
| A | Audio CTRL | 1 | 0 | 1 | 0 | 0 | 0 | Mute | ATT | 0 | 0 | OPSL2 0 | EMPH | SMUT | 0 | AD9 | AD8 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 | — | — | — | — |
| | | 1 | 0 | 1 | 0 | 0 | 0 | Mute | ATT | 0 | 0 | OPSL2 1 | EMPH | SMUT | 0 | AD9 | AD8 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 | FMUT | LRWO | BSBST | BBSL |
| B | Serial bus CTRL | 1 | 0 | 1 | 1 | SL1 | SL0 | CPUSR | 0 | TRMI | TRMO | MTSL1 | MTSL0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — |
| C | Spindle servo coefficient setting | 1 | 1 | 0 | 0 | Gain MDP1 | Gain MDP0 | Gain MDS1 | Gain MDS0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| D | CLV CTRL | 1 | 1 | 0 | 1 | 0 | TB | TP | Gain CLVS | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 | — | — | — | — | — | — | — | — | — | — | — | — |
| E | CLV mode | 1 | 1 | 1 | 0 | CM3 | CM2 | CM1 | CM0 | EPWM | SPDC | ICAP | SFSL | VC2C | HIFC | LPWR | VPON | Gain CAV1 | Gain CAV0 | 0 | 0 | — | — | — | — | — | — | — | — |

## §1-3. CPU Command Presets

### Command Preset Table ($0X to 34X)

| Register | Command | Address | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | FOCUS CONTROL | 0 0 0 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | FOCUS SERVO OFF, 0V OUT |
| 1 | TRACKING CONTROL | 0 0 0 1 | 0 | 0 | 0 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING GAIN UP FILTER SELECT 1 |
| 2 | TRACKING MODE | 0 0 1 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRACKING SERVO OFF SLED SERVO OFF |
| Register | Command | Address | | | Data 1 | | Data 2 | | | | Data 3 | | | | Data 4 | | | | Data 5 | | | | |
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D0 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SLED KICK LEVEL (±1 × basic value) (Default) |
| | | Address 1 | | | | | Address 2 | | | | Address 3 | | | | Data 1 | | | | Data 2 | | | | |
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D0 | D0 | |
| | | 0 0 1 1 | 0 | 1 | 0 | 0 | 0 | See "Coefficient ROM Preset Values Table". | | | | | | | | | | | | | | | KRAM DATA ($3400XX to $344fXX) |

—: Don't care

## Command Preset Table ($34FX to 3FX)

| Register | Command | Address 1 | | | | | Address 2 | | | | | | Data 1 | | Data 2 | | | | Data 3 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 3 | SELECT | 0 0 1 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FOCUS BIAS LIMIT |
| | | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FOCUS BIAS DATA |
| | | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TRVSC DATA |
| | | Address | | | | | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | | |
| | | D23 to D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | | 0 0 1 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | FOCUS SEARCH SPEED/ VOLTAGE AUTO GAIN |
| | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | DTZC/TRACK JUMP VOLTAGE AUTO GAIN |
| | | | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | FZSL/SLED MOVE/ Voltage/AUTO GAIN |
| | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LEVEL/AUTO GAIN/ DFSW/ (Initialize) |
| | | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SERIAL DATA READ MODE/SELECT |
| | | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FOCUS BIAS |
| | | | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | Operation for MIRR/ DFCT/FOK |
| | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TZC/COUT BOTTOM/MIRR |
| | | | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SLED FILTER |
| | | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Filter |
| | | | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Others |

—: Don't care

## Reset Initialization

| Register | Command | Address D3 | Address D2 | Address D1 | Address D0 | Data 1 D3 | Data 1 D2 | Data 1 D1 | Data 1 D0 | Data 2 D3 | Data 2 D2 | Data 2 D1 | Data 2 D0 | Data 3 D3 | Data 3 D2 | Data 3 D1 | Data 3 D0 | Data 4 D3 | Data 4 D2 | Data 4 D1 | Data 4 D0 | Data 5 D3 | Data 5 D2 | Data 5 D1 | Data 5 D0 | Data 6 D3 | Data 6 D2 | Data 6 D1 | Data 6 D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 | Auto sequence | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 5 | Blind (A, E), Overflow (C) / Brake (B) | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 6 | KICK (D) | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| 7 | Auto sequence (N) track jump count setting | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — |
| 8 | MODE specification | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | Function specification | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — |
| A | Audio CTRL | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| B | Serial bus CTRL | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — |
| C | Spindle servo coefficient setting | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| D | CLV CTRL | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — | — | — | — | — |
| E | CLV mode | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | — | — | — | — | — | — | — | — |

**<Coefficient ROM Preset Values Table (1)>**

| ADDRESS | DATA | CONTENTS |
|---|---|---|
| K00 | E0 | SLED INPUT GAIN |
| K01 | 81 | SLED LOW BOOST FILTER A-H |
| K02 | 23 | SLED LOW BOOST FILTER A-L |
| K03 | 7F | SLED LOW BOOST FILTER B-H |
| K04 | 6A | SLED LOW BOOST FILTER B-L |
| K05 | 10 | SLED OUTPUT GAIN |
| K06 | 14 | FOCUS INPUT GAIN |
| K07 | 30 | SLED AUTO GAIN |
| K08 | 7F | FOCUS HIGH CUT FILTER A |
| K09 | 46 | FOCUS HIGH CUT FILTER B |
| K0A | 81 | FOCUS LOW BOOST FILTER A-H |
| K0B | 1C | FOCUS LOW BOOST FILTER A-L |
| K0C | 7F | FOCUS LOW BOOST FILTER B-H |
| K0D | 58 | FOCUS LOW BOOST FILTER B-L |
| K0E | 82 | FOCUS PHASE COMPENSATE FILTER A |
| K0F | 7F | FOCUS DEFECT HOLD GAIN |
| K10 | 4E | FOCUS PHASE COMPENSATE FILTER B |
| K11 | 32 | FOCUS OUTPUT GAIN |
| K12 | 20 | ANTI SHOCK INPUT GAIN |
| K13 | 30 | FOCUS AUTO GAIN |
| K14 | 80 | HPTZC / Auto Gain HIGH PASS FILTER A |
| K15 | 77 | HPTZC / Auto Gain HIGH PASS FILTER B |
| K16 | 80 | ANTI SHOCK HIGH PASS FILTER A |
| K17 | 77 | HPTZC / Auto Gain LOW PASS FILTER B |
| K18 | 00 | Fix* |
| K19 | F1 | TRACKING INPUT GAIN |
| K1A | 7F | TRACKING HIGH CUT FILTER A |
| K1B | 3B | TRACKING HIGH CUT FILTER B |
| K1C | 81 | TRACKING LOW BOOST FILTER A-H |
| K1D | 44 | TRACKING LOW BOOST FILTER A-L |
| K1E | 7F | TRACKING LOW BOOST FILTER B-H |
| K1F | 5E | TRACKING LOW BOOST FILTER B-L |
| K20 | 82 | TRACKING PHASE COMPENSATE FILTER A |
| K21 | 44 | TRACKING PHASE COMPENSATE FILTER B |
| K22 | 18 | TRACKING OUTPUT GAIN |
| K23 | 30 | TRACKING AUTO GAIN |
| K24 | 7F | FOCUS GAIN DOWN HIGH CUT FILTER A |
| K25 | 46 | FOCUS GAIN DOWN HIGH CUT FILTER B |
| K26 | 81 | FOCUS GAIN DOWN LOW BOOST FILTER A-H |
| K27 | 3A | FOCUS GAIN DOWN LOW BOOST FILTER A-L |
| K28 | 7F | FOCUS GAIN DOWN LOW BOOST FILTER B-H |
| K29 | 66 | FOCUS GAIN DOWN LOW BOOST FILTER B-L |
| K2A | 82 | FOCUS GAIN DOWN PHASE COMPENSATE FILTER A |
| K2B | 44 | FOCUS GAIN DOWN DEFECT HOLD GAIN |
| K2C | 4E | FOCUS GAIN DOWN PHASE COMPENSATE FILTER B |
| K2D | 1B | FOCUS GAIN DOWN OUTPUT GAIN |
| K2E | 00 | NOT USED |
| K2F | 00 | NOT USED |

* Fix indicates that normal preset values should be used.

**<Coefficient ROM Preset Values Table (2)>**

| ADDRESS | DATA | CONTENTS |
|---|---|---|
| K30 | 80 | SLED INPUT GAIN (Only when TRK Gain Up2 is accessed with SFSK = 1.) |
| K31 | 66 | ANTI SHOCK LOW PASS FILTER B |
| K32 | 00 | NOT USED |
| K33 | 7F | ANTI SHOCK HIGH PASS FILTER B-H |
| K34 | 6E | ANTI SHOCK HIGH PASS FILTER B-L |
| K35 | 20 | ANTI SHOCK FILTER COMPARATE GAIN |
| K36 | 7F | TRACKING GAIN UP2 HIGH CUT FILTER A |
| K37 | 3B | TRACKING GAIN UP2 HIGH CUT FILTER B |
| K38 | 80 | TRACKING GAIN UP2 LOW BOOST FILTER A-H |
| K39 | 44 | TRACKING GAIN UP2 LOW BOOST FILTER A-L |
| K3A | 7F | TRACKING GAIN UP2 LOW BOOST FILTER B-H |
| K3B | 77 | TRACKING GAIN UP2 LOW BOOST FILTER B-L |
| K3C | 86 | TRACKING GAIN UP PHASE COMPENSATE FILTER A |
| K3D | 0D | TRACKING GAIN UP PHASE COMPENSATE FILTER B |
| K3E | 57 | TRACKING GAIN UP OUTPUT GAIN |
| K3F | 00 | NOT USED |
| K40 | 04 | TRACKING HOLD FILTER INPUT GAIN |
| K41 | 7F | TRACKING HOLD FILTER A-H |
| K42 | 7F | TRACKING HOLD FILTER A-L |
| K43 | 79 | TRACKING HOLD FILTER B-H |
| K44 | 17 | TRACKING HOLD FILTER B-L |
| K45 | 6D | TRACKING HOLD FILTER OUTPUT GAIN |
| K46 | 00 | TRACKING HOLD FILTER INPUT GAIN (Only when TRK Gain Up2 is a accessed with THSK = 1.) |
| K47 | 00 | NOT USED |
| K48 | 02 | FOCUS HOLD FILTER INPUT GAIN |
| K49 | 7F | FOCUS HOLD FILTER A-H |
| K4A | 7F | FOCUS HOLD FILTER A-L |
| K4B | 79 | FOCUS HOLD FILTER B-H |
| K4C | 17 | FOCUS HOLD FILTER B-L |
| K4D | 54 | FOCUS HOLD FILTER OUTPUT GAIN |
| K4E | 00 | NOT USED |
| K4F | 00 | NOT USED |

## §1-4. Description of SENS Signals and Commands

### SENS output

| Microcomputer serial register (latching not required) | SENS output | Output data length |
|---|---|---|
| $0X | FZC | — |
| $1X | As (Anti Shock) | — |
| $2X | TZC | — |
| $30 to 37 | SSTP | — |
| $38 | AGOK | — |
| $38 | XA VEBSY | — |
| $3904 | TE Avrg Reg. | 9 bits |
| $3908 | FE Avrg Reg. | 9 bits |
| $390C | VC Avrg Reg. | 9 bits |
| $391C | TRVSC Reg. | 9 bits |
| $391D | FB Reg. | 9 bits |
| $391F | RFDC Avrg. Reg. | 8 bits |
| $3A | FBIAS count STOP | — |
| $3B to 3F | SSTP | — |
| $4X | XBUSY | — |
| $5X | FOK | — |
| $6X, 7X, 8X, 9X | 0 | — |
| $AX | GFS | — |
| $BX | 0 | — |
| $CX | COUT frequency division | — |
| $DX | 0 | — |
| $EX | OV64 | — |
| $FX | 0 | — |

The SENS output can be read from the SQSO pin when SOCT = 0, SL1 = 1 and SL0 = 0. (See $BX commands.)
$38 outputs AGOK during AGT and AGF command settings, and XAVEBSY during AVRG measurement.
SSTP is output in all other cases.

### Description of SENS Signals

| SENS output | Contents |
|---|---|
| XBUSY | Low while the auto sequencer is in operation, high when operation terminates. |
| FOK | Outputs the same signal as the FOK pin.<br>High for "focus OK". |
| GFS | High when the regenerated frame sync is obtained with the correct timing. |
| COUT frequency division | Counts the number of tracks with frequency division ratio set by $B.<br>High when $C is latched, and toggles each time COUT is counted just for the frequency division ratio set by $B. |
| OV64 | Low when the EFM signal is lengthened by 64 channel clock pulses or more after passing through the sync detection filter. |

The meaning of the data for each address is explained below.

**$4X commands**

| Command | AS3 | AS2 | AS1 | AS0 |
|---|---|---|---|---|
| CANCEL | 0 | 0 | 0 | 0 |
| FOCUS-ON | 0 | 1 | 1 | 1 |
| 1 TRACK JUMP | 1 | 0 | 0 | RXF |
| 10 TRACK JUMP | 1 | 0 | 1 | RXF |
| 2 NTRACK JUMP | 1 | 1 | 0 | RXF |
| N TRACK MOVE | 1 | 1 | 1 | RXF |

RXF = 0 FORWARD
RXF = 1 REVERSE

- When the Focus-on command ($47) is canceled, $02 is sent and the auto sequence is interrupted.
- When the Track jump/Move commands ($48 to $4F) are canceled, $25 is sent and the auto sequence is interrupted.

**$5X commands**

Auto sequence timer setting
Set timers: A, E, C, B

| Command | D3 | D2 | D1 | D0 |
|---|---|---|---|---|
| Blind (A, E), Over flow (C) | 0.18ms | 0.09ms | 0.05ms | 0.02ms |
| Brake (B) | 0.36ms | 0.18ms | 0.09ms | 0.05ms |

**e.g.)** D2 = D0 = 1, D3 = D1 = 0 (Initial Reset)
A = E = C = 0.11ms
B = 0.23ms

**$6X commands**

Auto sequence timer setting
Set timer: D

| Command | D3 | D2 | D1 | D0 |
|---|---|---|---|---|
| KICK (D) | 11.6ms | 5.8ms | 2.9ms | 1.45ms |

**e.g.)** D3 = 0, D2 = D1 = D0 = 1 (Initial Reset)
D = 10.15ms

**$7X commands**

Auto sequence track jump/move count setting (N)

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | | Data 4 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Auto sequence track jump count setting | $2^{15}$ | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^{9}$ | $2^{8}$ | $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |

This command is used to set N when a 2N-track jump or N-track move is executed for auto sequence.

- The maximum track count is 65,535, but note that with a 2N-track jump the maximum track jump count depends on the mechanical limitations of the optical system.
- The number of tracks jumped is counted according to the COUT signals.

**$8X commands**

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Mode specification | CDROM | DOUT Mute | DOUT ON/OFF | WSEL | VCO SEL1 | 0 | SOCT | VCO SEL2 | KSL3 | KSL2 | KSL1 | KSL0 |

See "$BX Commands".

| Data 4 | | | | Data 5 | | | | Data 6 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TXON | TXOUT | OUTL1 | OUTL0 |

| Command bit | C2PO timing | Processing |
|---|---|---|
| CDROM = 1 | See Timing Chart 1-1. | CDROM mode; average value interpolation and pre-value hold are not performed. |
| CDROM = 0 | See Timing Chart 1-1. | Audio mode; average value interpolation and pre-value hold are performed. |

| Command bit | Processing |
|---|---|
| DOUT Mute = 1 | Digital Out output is muted. (DA output is not muted.) |
| DOUT Mute = 0 | If other mute conditions are not set, Digital Out is not muted. |

| Command bit | Processing |
|---|---|
| DOUT ON/OFF = 1 | Digital Out is output from the DOUT pin. |
| DOUT ON/OFF = 0 | Digital Out is not output from the DOUT pin. |

| Command bit | Sync protection window width | Application |
|---|---|---|
| WSEL = 1 | ±26 channel clock*1 | Anti-rolling is enhanced. |
| WSEL = 0 | ±6 channel clock | Sync window protection is enhanced. |

*1 In normal-speed playback, channel clock = 4.3218MHz.

| Command bit | | | Processing |
|---|---|---|---|
| VCOSEL1 | KSL3 | KSL2 | |
| 0 | 0 | 0 | Multiplier PLL VCO1 is set to normal speed, and the output is 1/1 frequency-divided. |
| 0 | 0 | 1 | Multiplier PLL VCO1 is set to normal speed, and the output is 1/2 frequency-divided. |
| 0 | 1 | 0 | Multiplier PLL VCO1 is set to normal speed, and the output is 1/4 frequency-divided. |
| 0 | 1 | 1 | Multiplier PLL VCO1 is set to normal speed, and the output is 1/8 frequency-divided. |
| 1 | 0 | 0 | Multiplier PLL VCO1 is set to high speed*1, and the output is 1/1 frequency-divided. |
| 1 | 0 | 1 | Multiplier PLL VCO1 is set to high speed*1, and the output is 1/2 frequency-divided. |
| 1 | 1 | 0 | Multiplier PLL VCO1 is set to high speed*1, and the output is 1/4 frequency-divided. |
| 1 | 1 | 1 | Multiplier PLL VCO1 is set to high speed*1, and the output is 1/8 frequency-divided. |

*1 Approximately twice the normal speed

| Command bit | | | Processing |
|---|---|---|---|
| VCOSEL2 | KSL1 | KSL0 | |
| 0 | 0 | 0 | Wide-band PLL VCO2 is set to normal speed, and the output is 1/1 frequency-divided. |
| 0 | 0 | 1 | Wide-band PLL VCO2 is set to normal speed, and the output is 1/2 frequency-divided. |
| 0 | 1 | 0 | Wide-band PLL VCO2 is set to normal speed, and the output is 1/4 frequency-divided. |
| 0 | 1 | 1 | Wide-band PLL VCO2 is set to normal speed, and the output is 1/8 frequency-divided. |
| 1 | 0 | 0 | Wide-band PLL VCO2 is set to high speed*2, and the output is 1/1 frequency-divided. |
| 1 | 0 | 1 | Wide-band PLL VCO2 is set to high speed*2, and the output is 1/2 frequency-divided. |
| 1 | 1 | 0 | Wide-band PLL VCO2 is set to high speed*2, and the output is 1/4 frequency-divided. |
| 1 | 1 | 1 | Wide-band PLL VCO2 is set to high speed*2, and the output is 1/8 frequency-divided. |

*2 Approximately twice the normal speed

| Command bit | Processing |
|---|---|
| TXON = 0 | When CD TEXT data is not demodulated, set TXON to 0. |
| TXON = 1 | When CD TEXT data is demodulated, set TXON to 1. |

* See "$4-13. CD TEXT Data Demodulation"

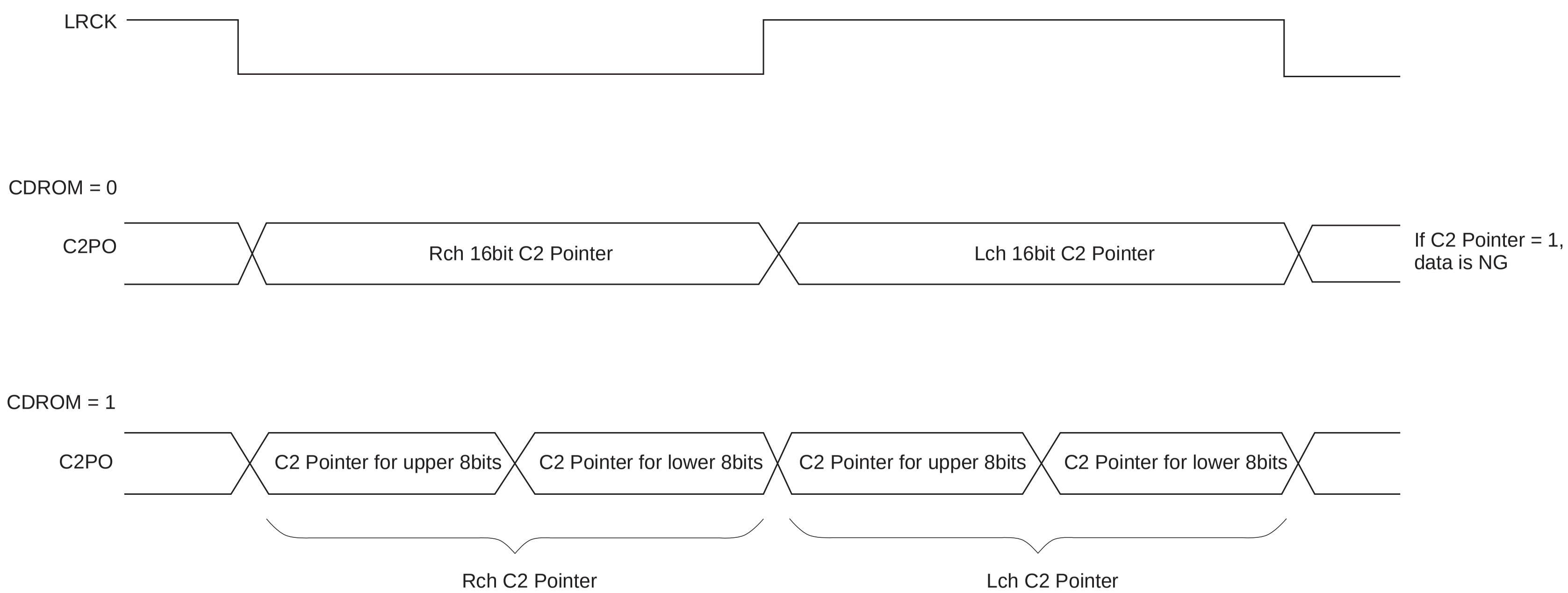
| Command bit | Processing |
|---|---|
| TXOUT = 0 | Various signals except for CD TEXT is output from the SQSO pin. |
| TXOUT = 1 | CD TEXT data is output from the SQSO pin. |

* See "$4-13. CD TEXT Data Demodulation"

| Command bit | Processing |
|---|---|
| OUTL1 = 0 | WFCK and XPCK are output. |
| OUTL1 = 1 | WFCK and XPCK outputs are set to low. |

| Command bit | Processing |
|---|---|
| OUTL0 = 0 | PCMD, BCK, LRCK and EMPH are output. |
| OUTL0 = 1 | PCMD, BCK, LRCK and EMPH outputs are low. |

**Timing Chart 1-1**



**$9X commands (OPSL1= 0)** * Data 2 D0 and subsequent data are for DF/DAC function settings.

| Command | Data 1 | | | | Data 2 | | Data 3 | | | | Data 4 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D3 | D2 | D1 | D0 | D3 to D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Function specification | 0 | DSPB ON/OFF | 0 | 0 | 000 | 0 | 0 | MCSL | 0 | 0 | ZDPL | ZMUT | — | — |

OPSL1

| Data 5 | | | |
|---|---|---|---|
| D3 | D2 | D1 | D0 |
| — | — | — | — |

**$9X commands (OPSL1= 1)** * Data 2 D0 and subsequent data are for DF/DAC function settings.

| Command | Data 1 | | | | Data 2 | | Data 3 | | | | Data 4 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D3 | D2 | D1 | D0 | D3 to D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Function specification | 0 | DSPB ON/OFF | 0 | 0 | 000 | 0 | 1 | MCSL | 0 | 0 | ZDPL | ZMUT | 0 | 0 |

OPSL1

| Data 5 | | | |
|---|---|---|---|
| D3 | D2 | D1 | D0 |
| 0 | DCOF | 0 | 0 |

| Command bit | Processing |
|---|---|
| DSPB = 1 | Double-speed playback (CD-DSP block) |
| DSPB = 0 | Normal-speed playback (CD-DSP block) |

| Command bit | Processing |
|---|---|
| OPSL1 = 1 | DCOF can be set. |
| OPSL1 = 0 | DCOF cannot be set. |

| Command bit | Processing |
|---|---|
| MCSL = 1 | DF/DAC block master clock selection. Crystal = 768Fs (33.8688MHz) |
| MCSL = 0 | DF/DAC block master clock selection. Crystal = 384Fs (16.9344MHz) |

| Command bit | Processing |
|---|---|
| ZDPL = 1 | LMUT and RMUT pins are high when muted. |
| ZDPL = 0 | LMUT and RMUT pins are low when muted. |

* See "Mute flag output" for the mute flag output conditions.

| Command bit | Processing |
| --- | --- |
| ZMUT = 1 | Zero detection mute is on. |
| ZMUT = 0 | Zero detection mute is off. |

| Command bit | Processing |
| --- | --- |
| DCOF = 1 | DC offset is off. |
| DCOF = 0 | DC offset is on. |

* DCOF can be set when OPSL1 = 1.
* Set DC offset to off when zero detection mute is on.

**$AX commands (OPSL2 = 0)**

* Data 2 and subsequent data are for DF/DAC function settings.

| Command | Data 1 | | | | Data 2 | | | | Data 3 | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 |
| Audio CTRL | 0 | 0 | Mute | ATT | 0 | 0 | 0 | EMPH | SMUT | AD10 |

OPSL2

| Data 3 | | Data 4 | | | | Data 5 | | | | Data 6 | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| AD9 | AD8 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 | — | — | — | — |

**$AX commands (OPSL2 = 1)**

* Data 2 and subsequent data are for DF/DAC function settings.

| Command | Data 1 | | | | Data 2 | | | | Data 3 | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 |
| Audio CTRL | 0 | 0 | Mute | ATT | 0 | 0 | 1 | EMPH | SMUT | 0 |

OPSL2

| Data 3 | | Data 4 | | | | Data 5 | | | | Data 6 | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| AD9 | AD8 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 | FMUT | LRWO | BSBST | BBSL |

| Command bit | Processing |
| --- | --- |
| Mute = 1 | CD-DSP block mute is on. 0 data is output from the CD-DSP block. |
| Mute = 0 | CD-DSP block mute is off. |

| Command bit | Processing |
|---|---|
| ATT = 1 | CD-DSP block output is attenuated (–12dB). |
| ATT = 0 | CD-DSP block output attenuation is off. |

| Command bit | Meaning |
|---|---|
| OPSL2 = 1 | FMUT, LRWO, BSBST and BBSL can be set. |
| OPSL2 = 0 | FMUT, LRWO, BSBST and BBSL cannot be set. |

| Command bit | Processing |
|---|---|
| EMPH = 1 | De-emphasis is on. |
| EMPH = 0 | De-emphasis is off. |

* If either the EMPHI pin or EMPH is high, de-emphasis is on.

| Command bit | Processing |
|---|---|
| SMUT = 1 | Soft mute is on. |
| SMUT = 0 | Soft mute is off. |

* If either the SMUT pin or SMUT is high, soft mute is on.

| Command bit | Meaning |
|---|---|
| AD10 to 0 | Attenuation data. |

The attenuation data consists of 11 bits, and is set as follows.

| Attenuation data | Audio output |
|---|---|
| 400h | 0dB |
| 3FEh<br>3FDh<br>:<br>001h | –0.0085dB<br>–0.0170dB<br><br>–60.206dB |
| 000h | $-\infty$ |

The attenuation data (AD10 to AD0) consists of 11 bits, and can be set in 1024 different ways in the range of 000h to 400h.
The audio output from 001h to 400h is obtained using the following equation.

$$\text{Audio output} = 20\log \frac{\text{Attenuation data}}{1024} \text{ [dB]}$$

| Command bit | Meaning |
|---|---|
| FMUT = 1 | Forced mute is on. |
| FMUT = 0 | Forced mute is off. |

* FMUT can be set when OPSL2 = 1.

| Command bit | Meaning |
|---|---|
| LRWO = 1 | Forced synchronization mode **Note)** |
| LRWO = 0 | Normal operation. |

* LRWO can be set when OPSL2 = 1.

**Note)** Synchronization is performed at the first falling edge of LRCK during reset, so there is normally no need to set this mode. However, synchronization can be forcibly performed by setting LRWO = 1.

| Command bit | Processing |
|---|---|
| BSBST = 1 | Bass boost is on. |
| BSBST = 0 | Bass boost is off. |

* BSBST can be set when OPSL2 = 1.

| Command bit | Processing |
|---|---|
| BBSL = 1 | Bass boost is Max. |
| BBSL = 0 | Bass boost is Mid. |

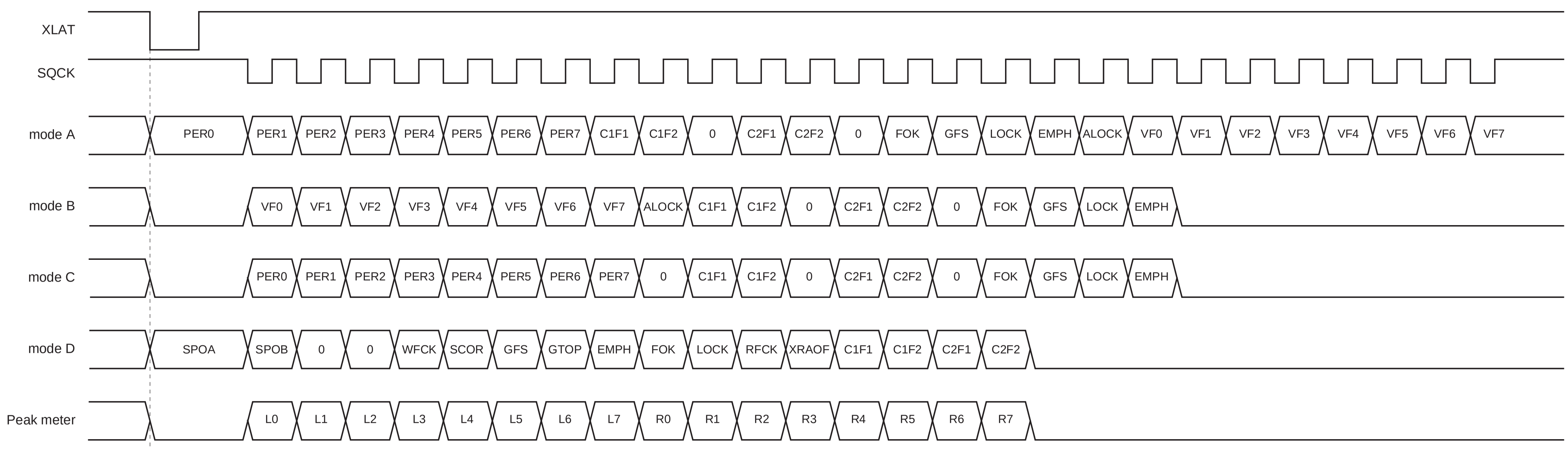
* BBSL can be set when OPSL2 = 1.

### $BX commands

| Command | Data 1 | | | | Data 2 | | | |
|---|---|---|---|---|---|---|---|---|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| Serial bus CTRL | SL1 | SL0 | CPUSR | 0 | TRM1 | TRM0 | MTSL1 | MTSL0 |

| SOCT | SL1 | SL0 | mode |
|---|---|---|---|
| 0 | 0 | 0 | SubQ |
| 0 | 0 | 1 | Peak meter |
| 0 | 1 | 0 | SENS |
| 0 | 1 | 1 | D |
| 1 | 0 | 0 | SubQ |
| 1 | 0 | 1 | A |
| 1 | 1 | 0 | B |
| 1 | 1 | 1 | C |

The SQSO pin output can be switched to the various signals by setting the SOCT command of $8X and the SL1 and SL0 commands of $BX. Set SQCK to high at the falling edge of XLAT.
Except for Sub Q and peak meter, the signals are loaded to the register when they are set at the falling edge of XLAT. Sub Q is loaded to the register with each SCOR, and Peak meter is loaded when a peak is detected.



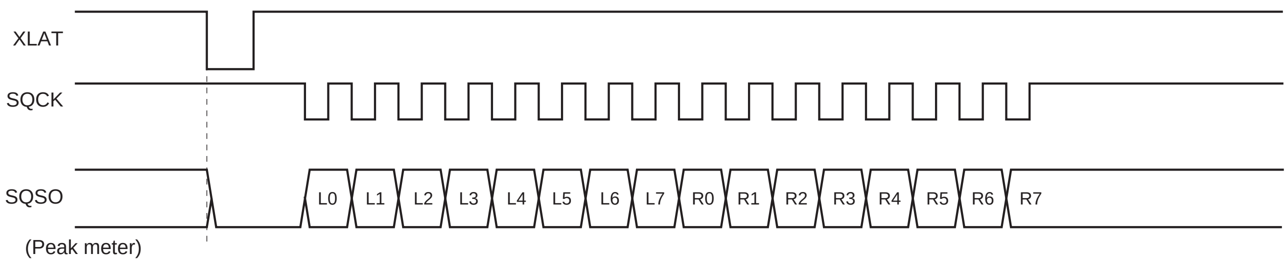
| Signal | Description |
|---|---|
| PER0 to 7 | RF jitter amount (used to adjust the focus bias). 8-bit binary data in PER0 = LSB, PER7 = MSB. |
| FOK | Focus OK |
| GFS | High when the frame sync and the insertion protection timing match. |
| LOCK | GFS is sampled at 460Hz; when GFS is high, a high signal is output. If GFS is low eight consecutive samples, a low signal is output. |
| EMPH | High when the playback disc has emphasis. |
| ALOCK | GFS is sampled at 460Hz; when GFS is high eight consecutive samples, a high signal is output. If GFS is low eight consecutive samples, a low signal is output. |
| VF0 to 7 | Used in CAV-W mode. Results of measuring the disc rotational velocity. (See Timing Chart 2-3.) VF0 = LSB, VF7 = MSB. |
| SPOA, B | SPOA and B pin inputs. |
| WFCK | Write frame clock output. |
| SCOR | High when either subcode sync S0 or S1 is detected. |
| GTOP | High when the sync protection window is open. |
| RFCK | Read frame clock output. |
| XRAOF | Low when the built-in 16K RAM exceeds the ±4 frame jitter margin. |
| L0 to L7, R0 to R7 | Peak meter register output. L0 to L7 are the left-channel and R0 to R7 are the right-channel peak data. L0 and R0 are LSB. |

| C1F1 | C1F2 | C1 correction status |
|---|---|---|
| 0 | 0 | No Error |
| 1 | 0 | Single Error Correction |
| 1 | 1 | Irretrievable Error |

| C2F1 | C2F2 | C2 correction status |
|---|---|---|
| 0 | 0 | No Error |
| 1 | 0 | Single Error Correction |
| 1 | 1 | Irretrievable Error |

| Command bit | Processing |
|---|---|
| CPUSR = 1 | XLON pin is high. |
| CPUSR = 0 | XLON pin is low. |

**Peak meter**




Setting the SOCT command of $8X to 0 and the SL1 and SL0 commands of $BX to 0 and 1, respectively, results in peak detection mode. The SQSO output is connected to the peak register. The maximum PCM data values (absolute value, upper 8 bits) for the left and right channels can be read from SQSO by inputting 16 clocks to SQCK. Peak detection is not performed during SQCK input, and the peak register does not change during readout. This SQCK input judgment uses a retriggerable monostable multivibrator with a time constant of 270µs to 400µs. The time during which SQCK input is high should be 270µs or less. Also, peak detection is restarted 270µs to 400µs after SQCK input.

The peak register is reset with each readout (16 clocks input to SQCK).
The maximum value in peak detection mode is detected and held in this status until the next readout. When switching to peak detection mode, readout should be performed one time initially to reset the peak register.

Peak detection can also be performed for previous value hold and average value interpolation data.

**Traverse monitor count value setting**
These bits are set when monitoring the traverse condition of the SENS output according to the COUT frequency division.

| Command bit | | Processing |
|---|---|---|
| TRM1 | TRM0 | |
| 0 | 0 | 1/64 frequency division |
| 0 | 1 | 1/128 frequency division |
| 1 | 0 | 1/256 frequency division |
| 1 | 1 | 1/512 frequency division |

**Monitor output switching**
The monitor output can be switched to the various signals by setting the MTSL1 and MTSL0 commands of $B.

| | | Output data | | | |
|---|---|---|---|---|---|
| Command bit \ Symbol | | XUGF | XPCK | GFS | C2PO |
| MTSL1 | MTSL0 | | | | |
| 0 | 0 | XUGF | XPCK | GFS | C2PO |
| 0 | 1 | MNT1 | MNT0 | MNT3 | C2PO |
| 1 | 0 | RFCK | XPCK | XROF | GTOP |

**$CX commands**

| Command | D3 | D2 | D1 | D0 |
|---|---|---|---|---|
| Servo coefficient setting | Gain MDP1 | Gain MDP0 | Gain MDS1 | Gain MDS0 |
| CLV CTRL ($DX) | | | | Gain CLVS |

• CLV mode gain setting: GCLVS

| Gain MDS1 | Gain MDS0 | Gain CLVS | GCLVS |
|---|---|---|---|
| 0 | 0 | 0 | –12dB |
| 0 | 0 | 1 | –6dB |
| 0 | 1 | 0 | –6dB |
| 0 | 1 | 1 | 0dB |
| 1 | 0 | 0 | 0dB |
| 1 | 0 | 1 | +6dB |

• CLVP mode gain setting: GMDP: GMDS

| Gain MDP1 | Gain MDP0 | GMDP |
|---|---|---|
| 0 | 0 | –6dB |
| 0 | 1 | 0dB |
| 1 | 0 | +6dB |

| Gain MDS1 | Gain MDS0 | GMDS |
|---|---|---|
| 0 | 0 | –6dB |
| 0 | 1 | 0dB |
| 1 | 0 | +6dB |

**$DX commands**

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| CLV CTRL | 0 | TB | TP | Gain CLVS | VP7 | VP6 | VP5 | VP4 | VP3 | VP2 | VP1 | VP0 |

See the $CX commands.

| Command bit | Description |
|---|---|
| TB = 0 | Bottom hold at a cycle of RFCK/32 in CLVS mode. |
| TB = 1 | Bottom hold at a cycle of RFCK/16 in CLVS mode. |
| TP = 0 | Peak hold at a cycle of RFCK/4 in CLVS mode. |
| TP = 1 | Peak hold at a cycle of RFCK/2 in CLVS mode. |

| Command bit | Description |
|---|---|
| VP0 to VP7 = F0 (H) | Playback at half (normal) speed |
| : | to |
| VP0 to VP7 = E0 (H) | Playback at normal (double) speed |
| : | to |
| VP0 to VP7 = C0 (H) | Playback at (quadruple) speed |

The rotational velocity R of the spindle can be expressed with the following equation.

$$R = \frac{256 - n}{32}$$

R: Relative velocity at normal speed = 1
n: VP0 to VP7 setting value

**Note)** • Values in parentheses are for when DSPB is 1.
• Values when crystal is 16.9344MHz and XTSL is low or when crystal is 33.8688MHz and XTSL is high.
• VP0 to VP7 setting values are valid in CAV-W mode.

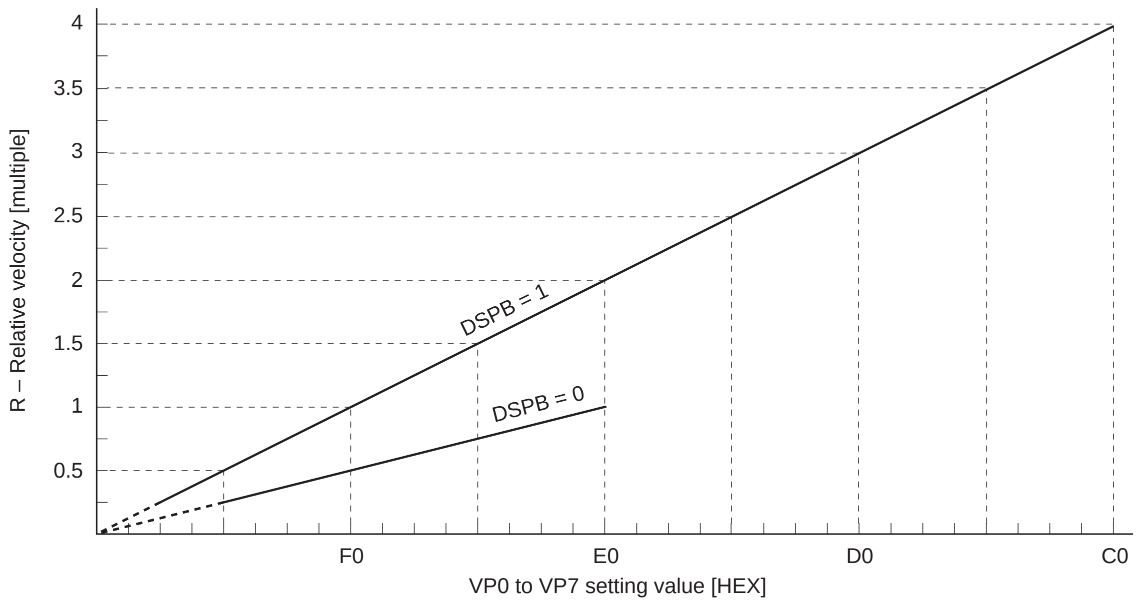



**Fig. 1-1**

**$EX commands**

| Command | Data 1 | | | | Data 2 | | | | Data 3 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| CLV mode | CM3 | CM2 | CM1 | CM0 | EPWM | SPDC | ICAP | SFSL | VC2C | HIFC | LPWR | VPON |

| Command bit | | | | Mode | Description |
|---|---|---|---|---|---|
| CM3 | CM2 | CM1 | CM0 | | |
| 0 | 0 | 0 | 0 | STOP | Spindle stop mode.*1 |
| 1 | 0 | 0 | 0 | KICK | Spindle forward rotation mode.*1 |
| 1 | 0 | 1 | 0 | BRAKE | Spindle reverse rotation mode. Valid only when LPWR = 0 in any mode.*1 |
| 1 | 1 | 1 | 0 | CLVS | Rough servo mode. When the RF-PLL circuit isn't locked, this mode is used to pull the disc rotations within the RF-PLL capture range. |
| 1 | 1 | 1 | 1 | CLVP | PLL servo mode. |
| 0 | 1 | 1 | 0 | CLVA | Automatic CLVS/CLVP switching mode.<br>Used for normal playback. |

*1 See Timing Charts 1-2 to 1-6.

| Command bit | | | | | | | | Mode | Description |
|---|---|---|---|---|---|---|---|---|---|
| EPWM | SPDC | ICAP | SFSL | VC2C | HIFC | LPWR | VPON | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CLV-N | Crystal reference CLV servo. |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | CLV-W | Used for normal-speed playback in CLV-W mode.*2 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | CAV-W | Spindle control with VP0 to VP7. |

*2 Figs. 3-1 and 3-2 show the control flow with the microcomputer software in CLV-W mode.

| Command | Data 4 | | | |
|---|---|---|---|---|
| | D3 | D2 | D1 | D0 |
| SPD mode | Gain CAV1 | Gain CAV0 | 0 | 0 |

| Gain CAV1 | Gain CAV0 | Gain |
|---|---|---|
| 0 | 0 | 0dB |
| 0 | 1 | –6dB |
| 1 | 0 | –12dB |
| 1 | 1 | –18dB |

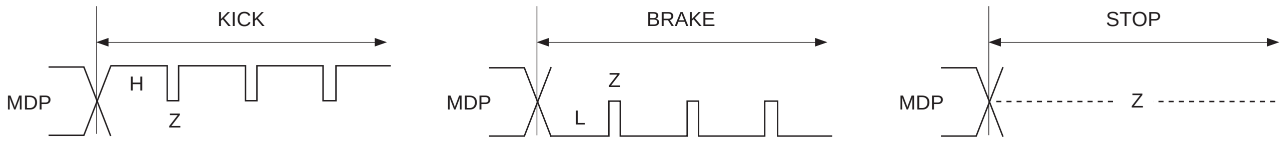
• This sets the gain when controlling the spindle with the phase comparator in CAV-W mode.

| Mode | LPWR | Command | Timing chart |
|---|---|---|---|
| CLV-N | 0 | KICK | 1-2 (a) |
| | | BRAKE | 1-2 (b) |
| | | STOP | 1-2 (c) |
| CLV-W | 0 | KICK | 1-3 (a) |
| | | BRAKE | 1-3 (b) |
| | | STOP | 1-3 (c) |
| | 1 | KICK | 1-4 (a) |
| | | BRAKE | 1-4 (b) |
| | | STOP | 1-4 (c) |
| CAV-W | 0 | KICK | 1-5 (a) |
| | | BRAKE | 1-5 (b) |
| | | STOP | 1-5 (c) |
| | 1 | KICK | 1-6 (a) |
| | | BRAKE | 1-6 (b) |
| | | STOP | 1-6 (c) |

| Mode | LPWR | Timing chart |
|---|---|---|
| CLV-N | 0 | 1-7 |
| CLV-W | 0 | 1-8 |
| | 1 | 1-9 |
| CAV-W | 0 | 1-10 (EPWM = 0) |
| | 1 | 1-11 (EPWM = 0) |
| | 0 | 1-12 (EPWM = 1) |
| | 1 | 1-13 (EPWM = 1) |

**Timing Chart 1-2**

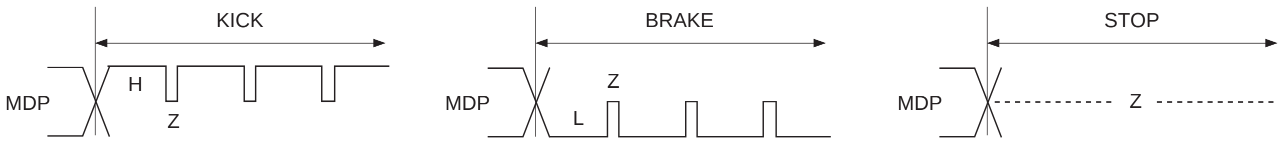
**CLV-N mode** LPWR = 0




(a) KICK (b) BRAKE (c) STOP

**Timing Chart 1-3**

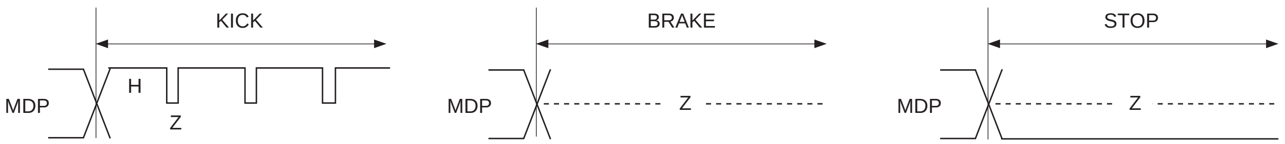
**CLV-W mode (when following the spindle rotational velocity)** LPWR = 0




(a) KICK (b) BRAKE (c) STOP

**Timing Chart 1-4**

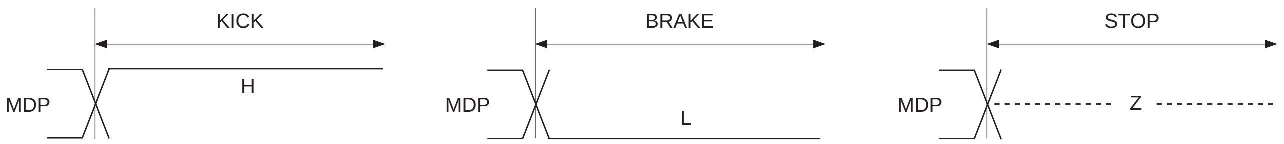
**CLV-W mode (when following the spindle rotational velocity)** LPWR = 1




(a) KICK (b) BRAKE (c) STOP

**Timing Chart 1-5**

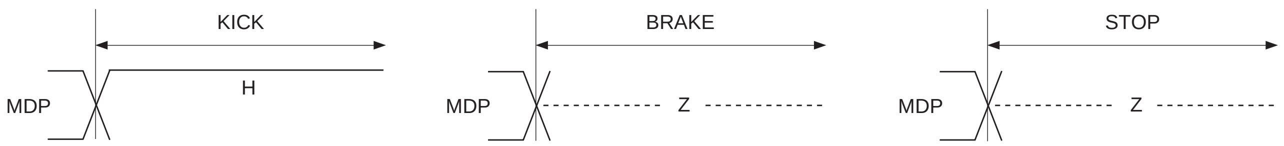
**CAV-W mode** LPWR = 0




(a) KICK (b) BRAKE (c) STOP

**Timing Chart 1-6**

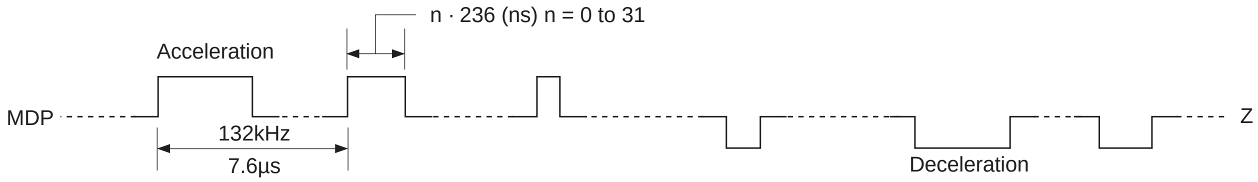
**CAV-W mode** LPWR = 1




(a) KICK (b) BRAKE (c) STOP

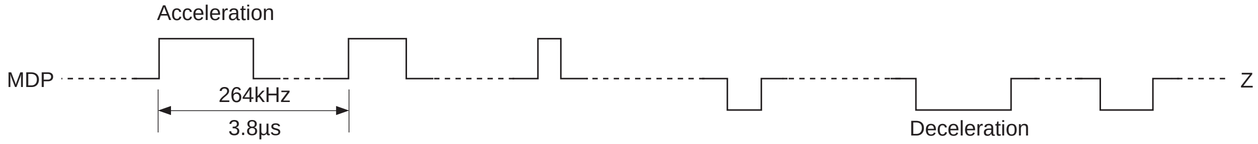
**Timing Chart 1-7**

**CLV-N mode** LPWR = 0



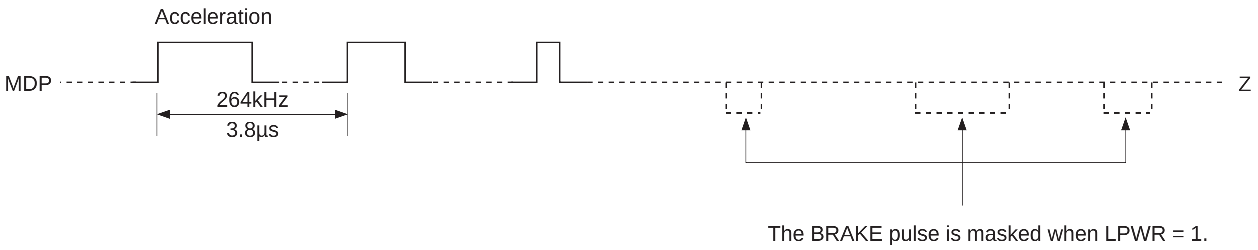

**Timing Chart 1-8**

**CLV-W mode** LPWR = 0



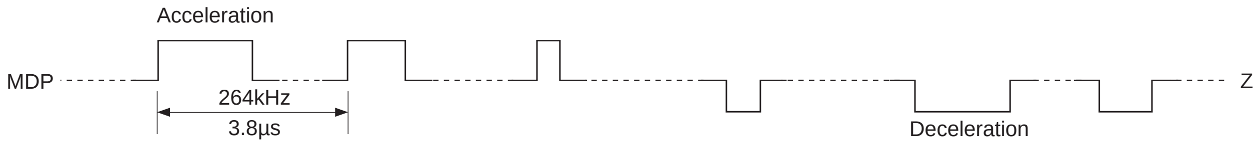

**Timing Chart 1-9**

**CLV-W mode** LPWR = 1



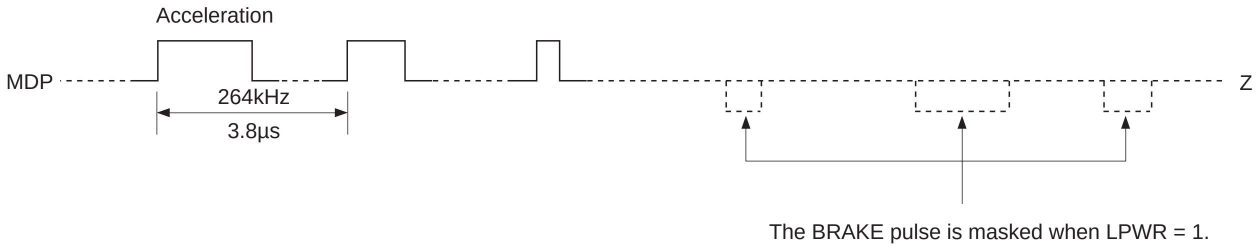

**Timing Chart 1-10**

**CAV-W mode** EPWM = LPWR = 0




**Timing Chart 1-11**

**CAV-W mode** EPWM = LPWR = 1



## §2. Subcode Interface

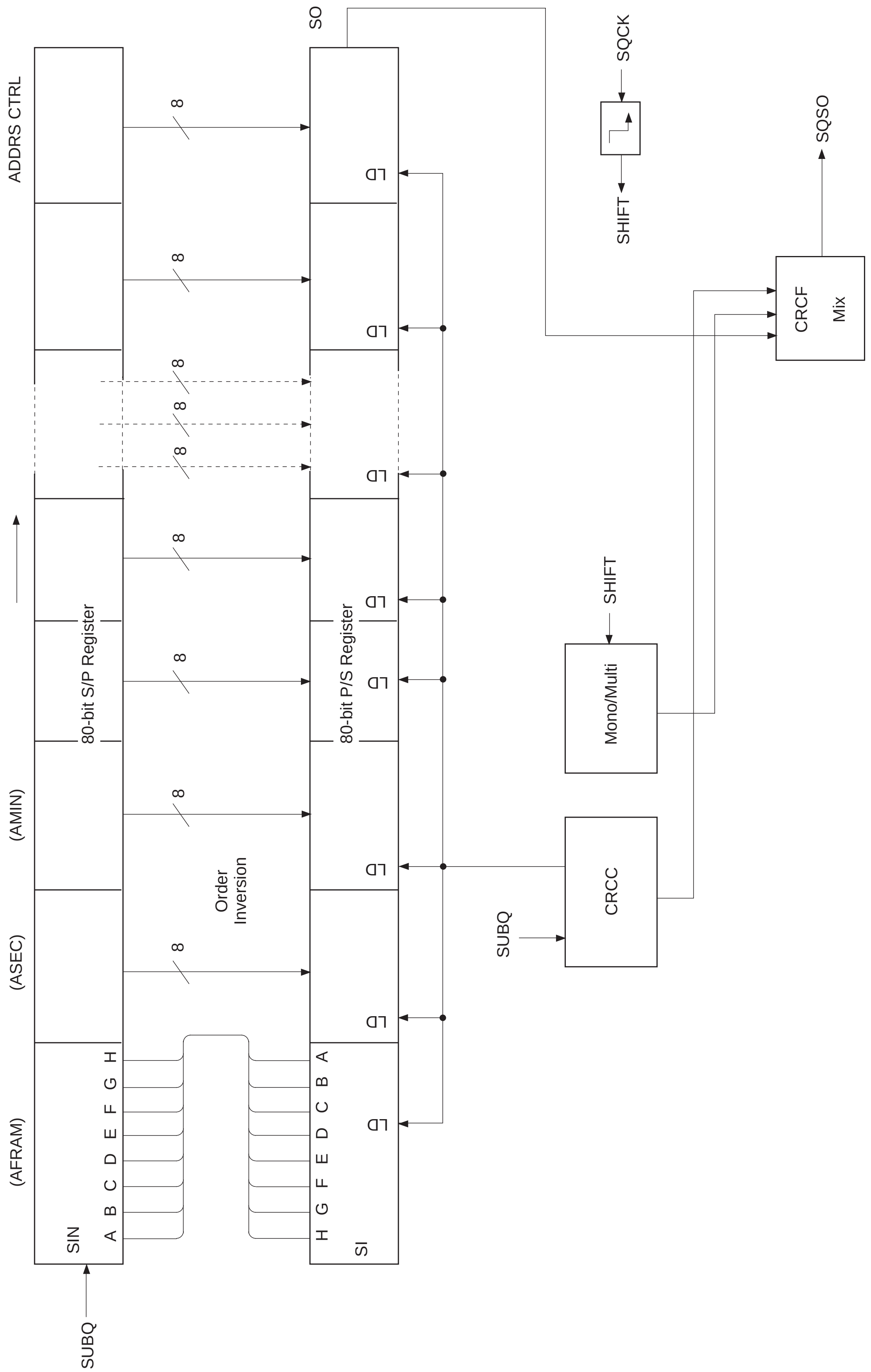
In the CXD2597Q, only SubQ can be readout.
The subcodes P and R to W cannot be readout.
Sub Q can be read out after checking CRC of the 80 bits in the subcode frame.
Sub Q can be read out from the SQSO pin by inputting 80 clock pulses to the SQCK pin when SCOR comes correctly and CRCF is high.

### §2-1. 80-bit Sub Q Readout

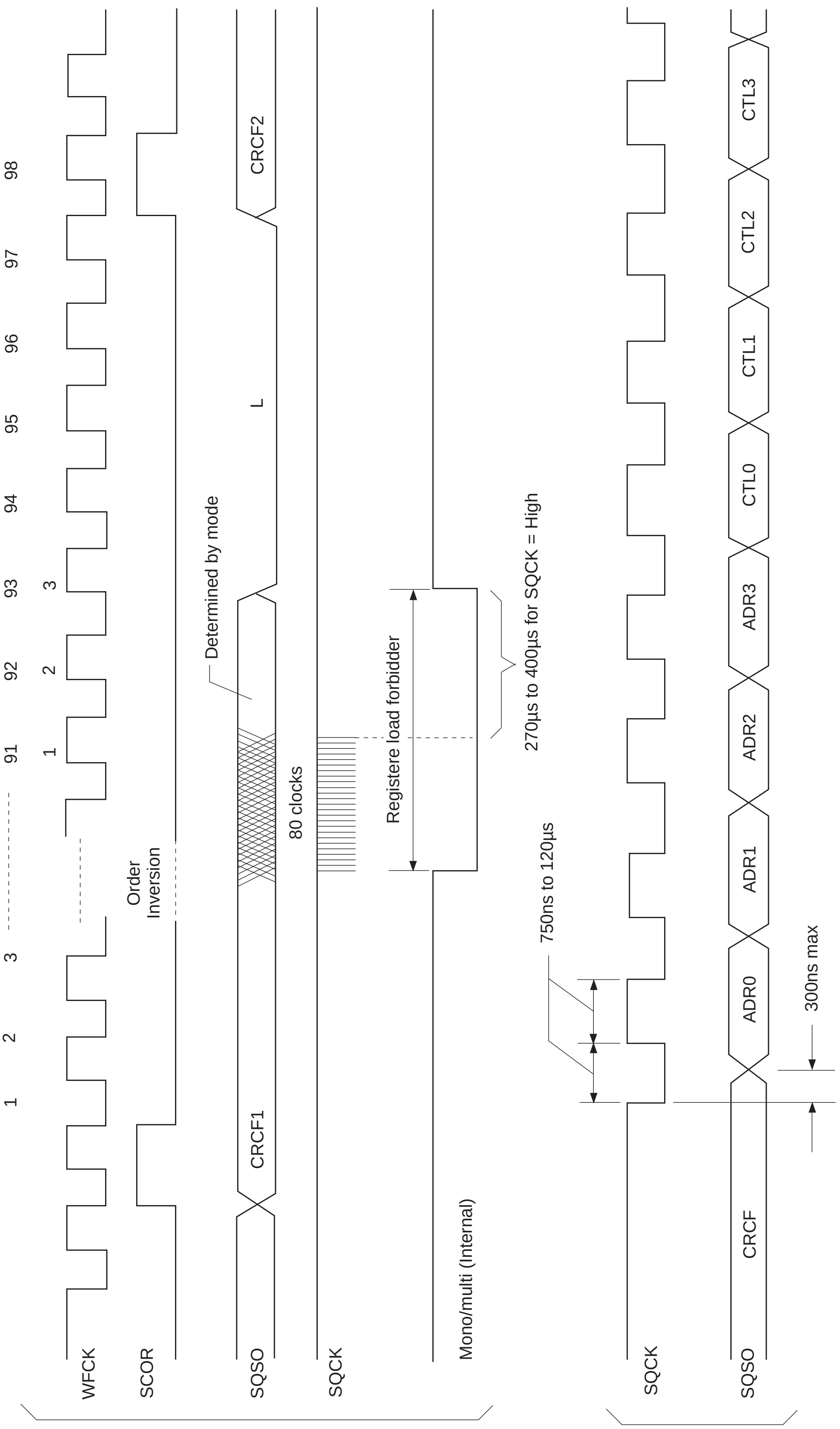
Fig. 2-1 shows the peripheral block of the 80-bit Sub Q register.

- First, Sub Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.
- 96-bit Sub Q is input, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, 80 bits are loaded into the parallel/serial register.
  When SQSO goes high 400µs (monostable multivibrator time constant) or more after subcode readout, the CPU determines that the new data (which passed the CRC check) has been loaded.
- The CRCF reset is performed by inputting SQCK. When the subcode data is discontinuous after track jump, etc. CRCF is reset by inputting SQCK. Then, if CRCF =1, the CPU determines that the new data has been loaded.
- When the 80-bit data is loaded, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.
- Once the 80-bit data load is confirmed, SQCK is input so that the data can be read.
  The SQCK input is detected, and the retriggerable monostable multivibrator is reset while the input is low.
- The retriggerable monostable multivibrator has a time constant from 270 to 400µs. When the duration when SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the serial/parallel register is not loaded into the parallel/serial register.
- While the monostable multivibrator is being reset, data cannot be loaded in the 80-bit parallel/serial register.
  In other words, while reading out with a clock cycle shorter than this time constant, the register will not be rewritten by CRCOK and others. (See Timing Chart 2-2.)
- The high and low intervals for SQCK should be between 750ns and 120µs.

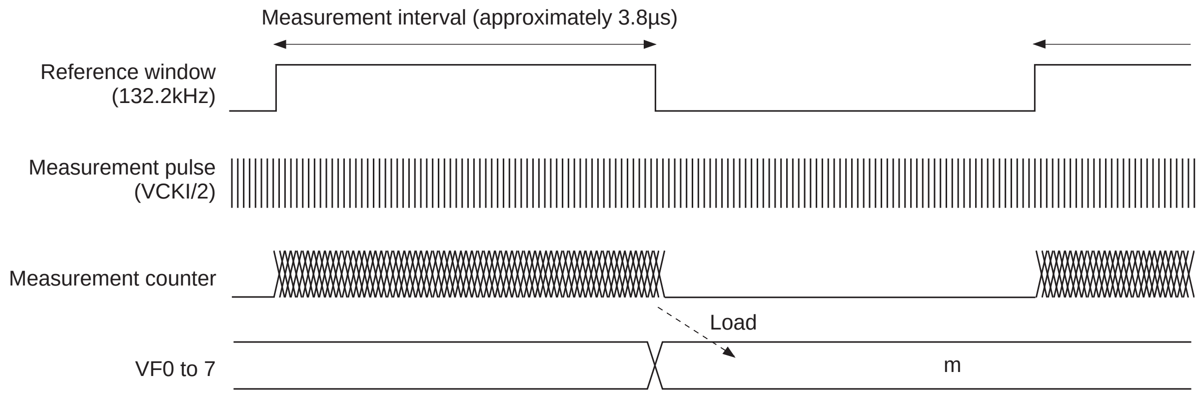
**Fig. 2-1. Block Diagram**



## Timing Chart 2-2



**Timing Chart 2-3**




The relative velocity R of the disc can be expressed with the following equation.

$$R = \frac{m + 1}{32} \quad \text{(R: Relative velocity, m: Measurement results)}$$

VF0 to VF7 is the result obtained by counting VCKI/2 pulses while the reference signal (132.2kHz) generated from the crystal (384Fs) is high. This count is 31 when the disc is rotating at normal speed and 63 when it is rotating at double speed (when DSPB is low).

## §3. Description of Modes

This LSI has three basic operating modes using a combination of spindle control and the PLL. The operations for each mode are described below.

### §3-1. CLV-N Mode

This mode is compatible with the CXD2507AQ, and operation is the same as for the conventional control. The PLL capture range is ±150kHz.

### §3-2. CLV-W Mode

This is the wide capture range mode. This mode allows the PLL to follow the rotational velocity of the disc. This rotational following control has two types: using the built-in VCO2 or providing an external VCO. The spindle is the same CLV servo as for the conventional series. Operation using the built-in VCO2 is described below. (When using an external VCO, input the signal from the VPCO pin to the low-pass filter, use the output from the low-pass filter as the control voltage for the external VCO, and input the oscillation output from the VCO to the VCKI pin.)
When starting to rotate the disc and/or speeding up to the lock range from the condition where the disc is stopped, CAV-W mode should be used. Specifically, first send $E6650 to set CAV-W mode and kick the disc, then send $E60C0 to set CLV-W mode if ALOCK is high, which can be readout serially from the SQSO pin. CLV mode can be used while ALOCK is high. The microcomputer monitors the serial data output, and must return the operation to the speed adjusting state (CAV-W mode) when ALOCK becomes low. The control flow according to the microcomputer software is shown in Fig. 3-2.
In CLV-W mode (normal), low power consumption is achieved by setting LPWR to high. Control was formerly performed by applying acceleration and deceleration pulses to the spindle motor. However, when LPWR is set to high, deceleration pulses are not output, thereby achieving low power consumption mode.

**Note)** The capture range for CLV-W mode has theoretically the range up to the signal processing limit.

### §3-3. CAV-W Mode

This is CAV mode. In this mode, the external clock is fixed and it is possible to control the spindle to variable rotational velocity. The rotational velocity is determined by the VP0 to VP7 setting values. When controlling the spindle with VP0 to VP7, setting CAV-W mode with the $E6650 command and controlling VP0 to VP7 with the $DX commands allows the rotational velocity to be varied from low speed to double speed. (See the $DX commands.)
The microcomputer can know the rotational velocity using V16M. The reference for the velocity measurement is a signal of 132.3kHz obtained by 1/128-frequency dividing the crystal (384Fs). The velocity is obtained by counting the half of V16M pulses while the reference is high, and the result is output from the new CPU interface as 8 bits (VF0 to VF7). These measurement results are 31 when the disc is rotating at normal speed or 63 when it is rotating at double speed. These values match those of the 256-n for control with VP0 to VP7.
In CAV-W mode, the spindle is set to the desired rotational velocity and the operation speed for the entire system follows this rotational velocity. Therefore, the cycles for the Fs system clock, PCM data and all other output signals from this LSI change according to the rotational velocity of the disc.

**Note)** The capture range for this mode is theoretically up to the signal processing limit.

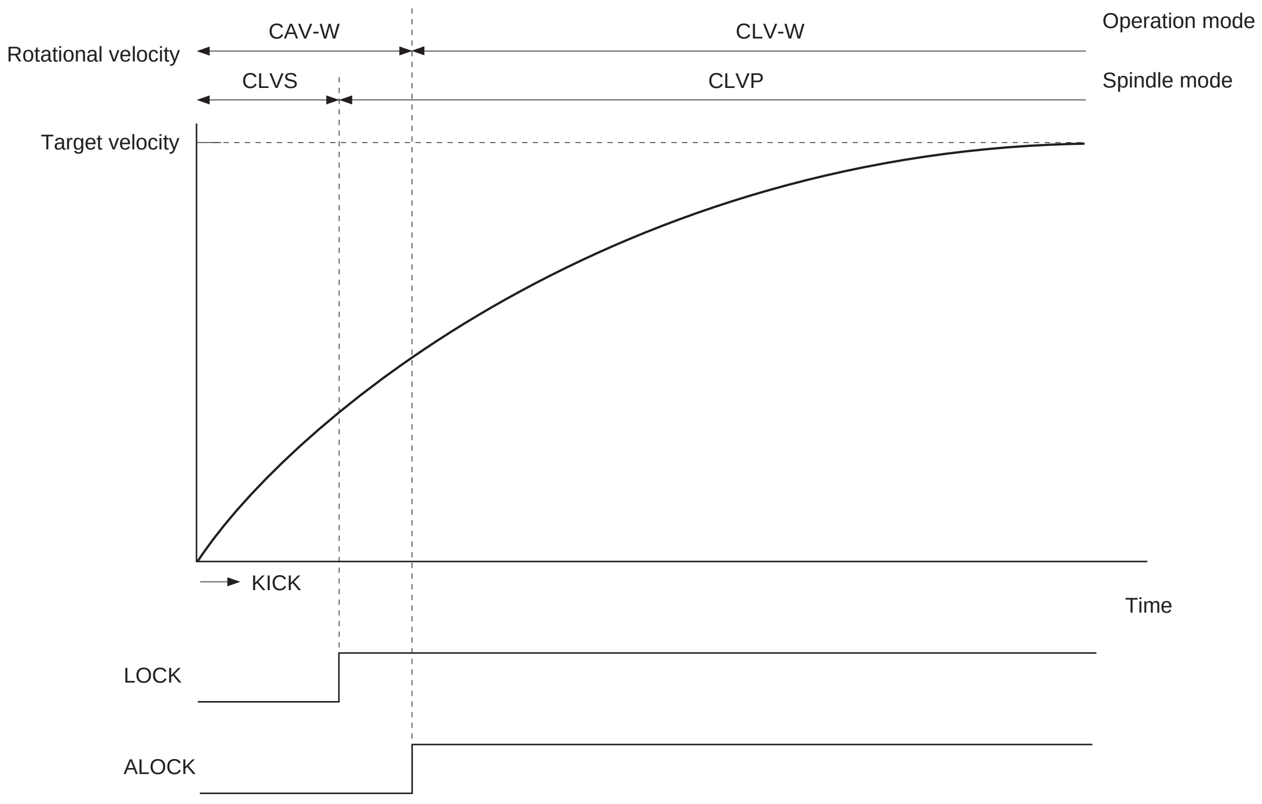



**Fig. 3-1. Disc Stop to Normal Condition in CLV-W Mode**

**CLV-W Mode**

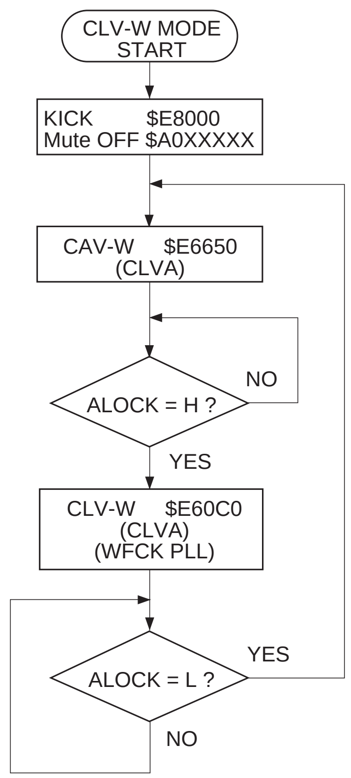



**Fig. 3-2. CLV-W Mode Flow Chart**

## §4. Description of Other Functions

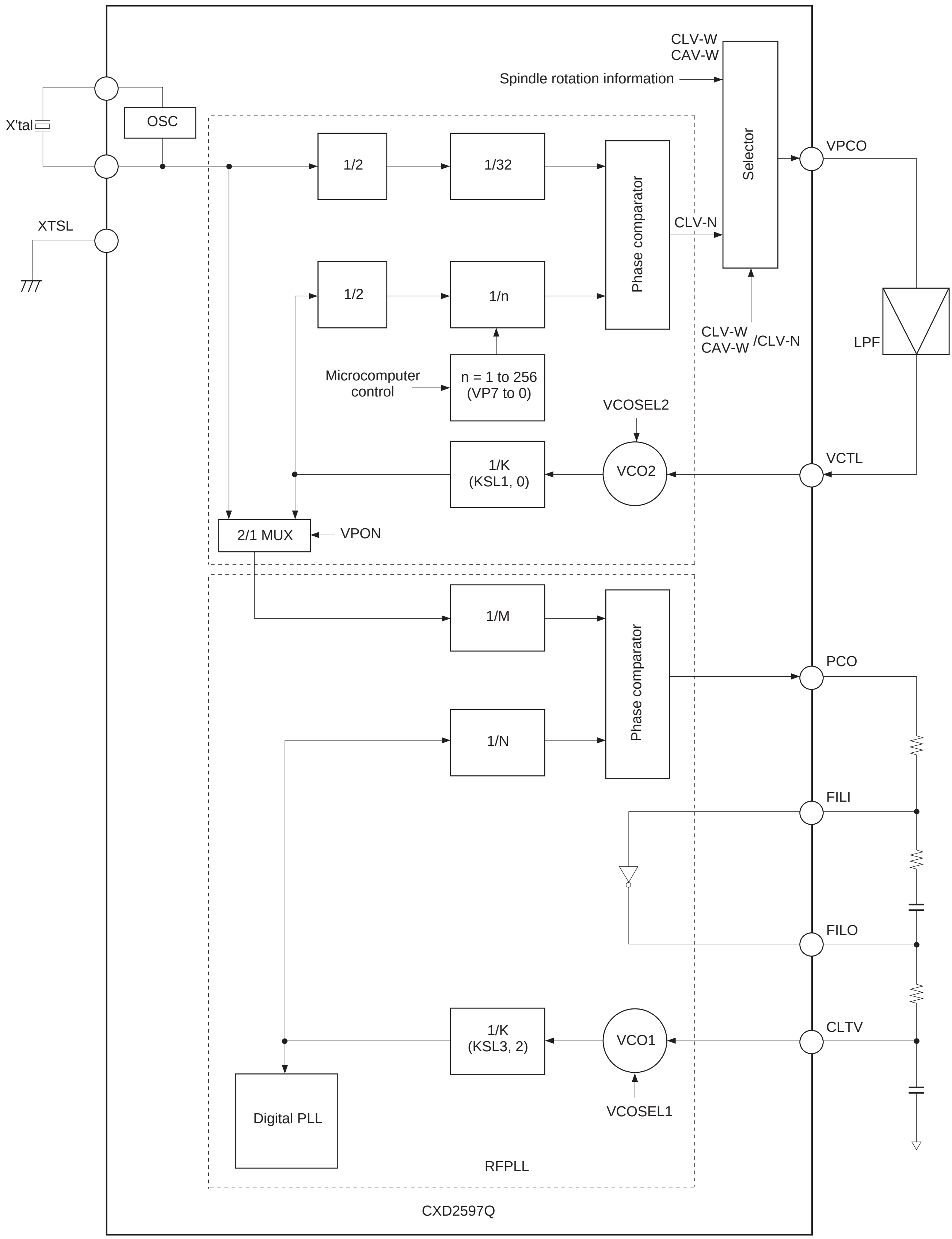
### §4-1. Channel Clock Recovery by Digital PLL Circuit

- The channel clock is necessary for demodulating the EFM signal regenerated by the optical system.
  Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from 3T to 11T. In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T, that is the channel clock, is necessary.
  In an actual player, the PLL is necessary to recover the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.

The block diagram of this PLL is shown in Fig. 4-1.
The CXD2597Q has a built-in three-stage PLL.

- The first-stage PLL is for the wide-band PLL. When the internal VCO2 is used, an external LPF is necessary; when not using the internal VCO2, external LPF and VCO are required.
  The output of this first-stage PLL is used as a reference for all clocks within the LSI.
- The second-stage PLL generates the high-frequency clock needed by the third-stage digital PLL.
- The third-stage PLL is a digital PLL that recovers the actual channel clock.
- A new digital PLL has been provided for CLV-W mode to follow the rotational velocity of the disc in addition to the conventional secondary loop.

## Block Diagram 4-1



### §4-2. Frame Sync Protection

- In normal-speed playback, a frame sync is recorded approximately every 136µs (7.35kHz). This signal is used as a reference to recognize the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because the data cannot be recognized. As a result, recognizing the frame sync properly is extremely important for improving playability.

- In the CXD2597Q, window protection and forward protection/backward protection have been adopted for frame sync protection. These functions achieve very powerful frame sync protection. There are two window widths: one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is fixed to 13, and the backward protection counter to 3. Concretely, when the disc is being played back normally and then the frame sync cannot be detected due to scratches etc., a maximum of 13 frames are inserted. If the frame sync cannot be detected for 13 frames or more, the window opens to resynchronize the frame sync.
  In addition, immediately after the window opens and the resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window opens immediately.

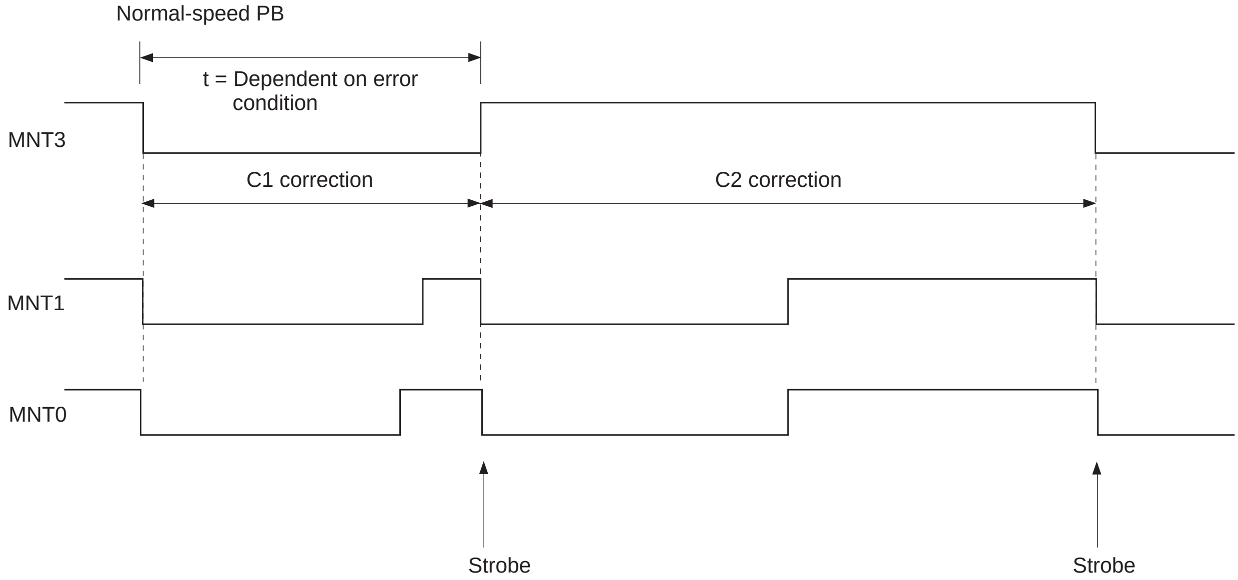
### §4-3. Error Correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.
  For C2 correction, the code is created with 24-byte information and 4-byte parity.
  Both C1 and C2 are Reed-Solomon codes with a minimum distance of 5.
- The CXD2597Q's SEC strategy uses powerful frame sync protection and C1 and C2 error correction to achieve high playability.
- The correction status can be monitored externally.
  See Table 4-2.
- When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held or an average value interpolation was made for the data.

| MNT3 | MNT1 | MNT0 | Description |
|---|---|---|---|
| 0 | 0 | 0 | No C1 errors |
| 0 | 0 | 1 | One C1 error corrected |
| 0 | 1 | 1 | C1 correction impossible |
| 1 | 0 | 0 | No C2 errors |
| 1 | 0 | 1 | One C2 error corrected |
| 1 | 1 | 0 | C2 correction impossible |

**Table 4-2.**

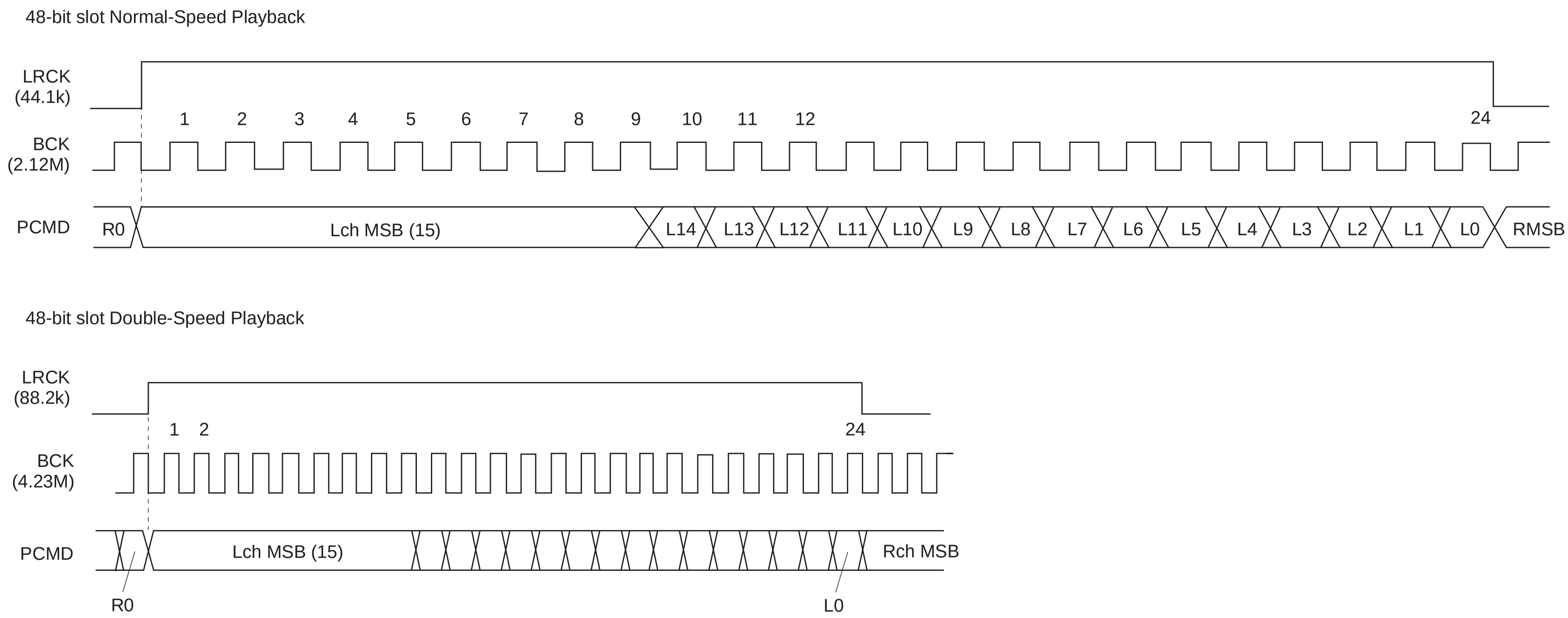
**Timing Chart 4-3**




**§4-4. DA Interface**

- The CXD2597Q DA interface is as described below.
  This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first. When LRCK is high, the data is for the left channel.

## Timing Chart 4-4



**§4-5. Digital Out**

There are three Digital Out: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.

The CXD2597Q supports type 2 form 1.

Sub Q data which are matched twice in succession after a CRC check are input to the first four bits (bits 0 to 3) of the channel status.

Digital Out C bit

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | From sub Q: ID0 | ID1 | COPY | Emph | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/1 | 0 | 0 |
| 32 to 176 | 0 | | | | | | | | | | | | | | | |

Bits 0 to 3 Sub Q control bits that matched twice with CRCOK
Bit 29 1 when VPON = 1

**Table 4-5.**

**§4-6. Servo Auto Sequence**

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1-track jump, 2N-track jump and N-track move are executed automatically.

The commands which enable transfer to the CXD2597Q during the execution of auto sequence are $4X to $EX.

When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point.

(a) Auto focus ($47)

Focus search-up is performed, FOK and FZC are checked, and the focus servo is turned on.

If $47 is received from the CPU, the focus servo is turned on according to Fig. 4-3. The auto focus starts with focus search-up, and note that the pickup should be lowered beforehand (focus search down). In addition, blind E of register 5 is used to eliminate FZC chattering. Concretely, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

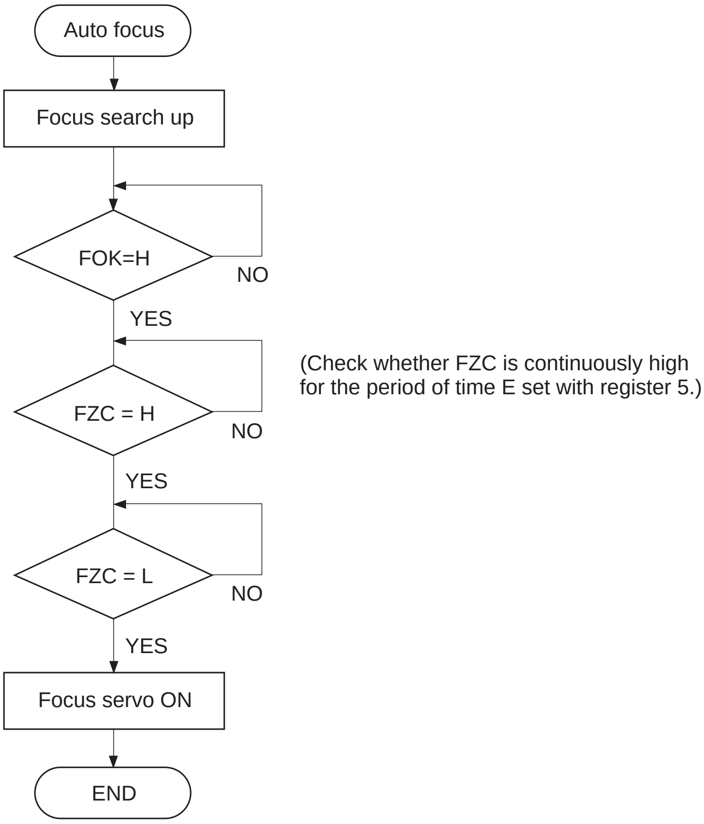



**Fig. 4-6-(a). Auto Focus Flow Chart**

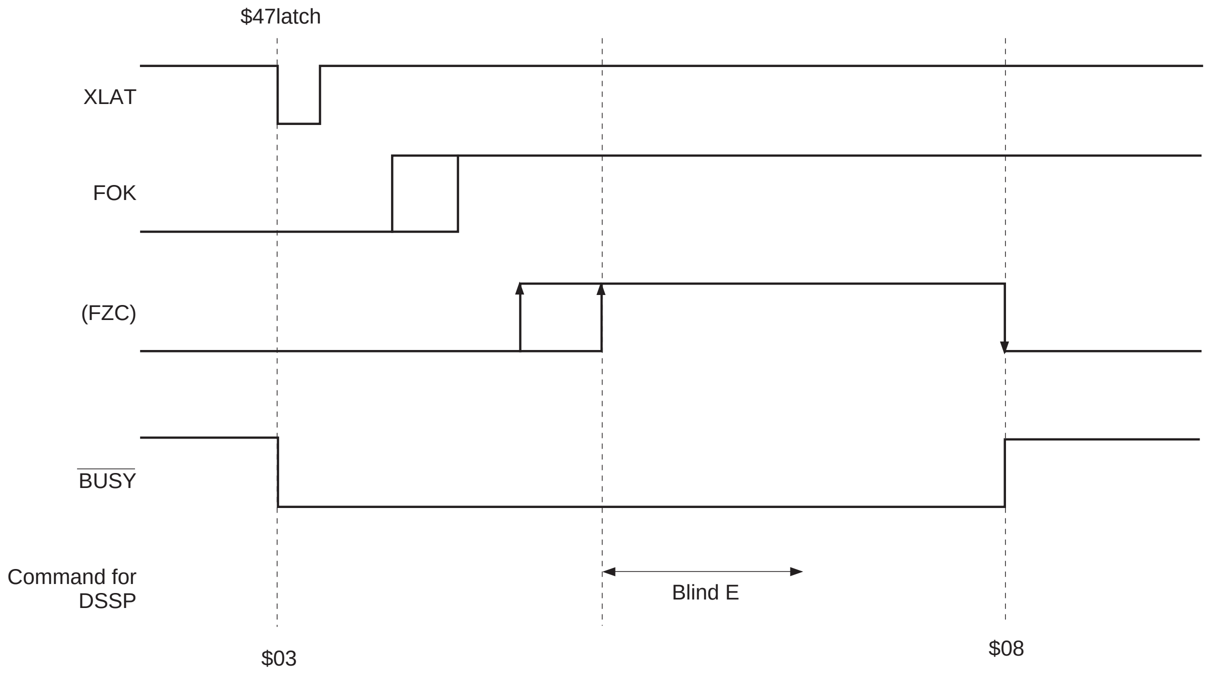



**Fig. 4-6-(b). Auto Focus Timing Chart**

(b) Track jump

1, 10 and 2N-track jumps are performed respectively. Always use this when the focus, tracking, and sled servos are on. Note that tracking gain-up and braking-on should be sent beforehand because they are not involved in this sequence.

• 1-track jump

When $48 ($49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 4-7. Set blind A and brake B with register 5.

• 10-track jump

When $4A ($4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed in accordance with Fig. 4-8. The principal difference from the 1-track jump is to kick the sled. In addition, after kicking the actuator, when 5 tracks have been counted through COUT, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the COUT cycle becoming longer than the overflow C set with register 5), the tracking and sled servos are turned on.

• 2N-track jump

When $4C ($4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 4-9. The track jump count N is set with register 7. Although N can be set to $2^{16}$ tracks, note that the setting is actually limited by the actuator. COUT is used for counting the number of jumps.

Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set with register 6.

• N-track move

When $4E ($4F for REV) is received from the CPU, a FWD (REV) N-track move is performed in accordance with Fig. 4-10. N can be set to $2^{16}$ tracks. COUT is used for counting the number of jumps. The N-track move is executed only by moving the sled, and is therefore suited for moving across several thousand to several ten-thousand tracks.

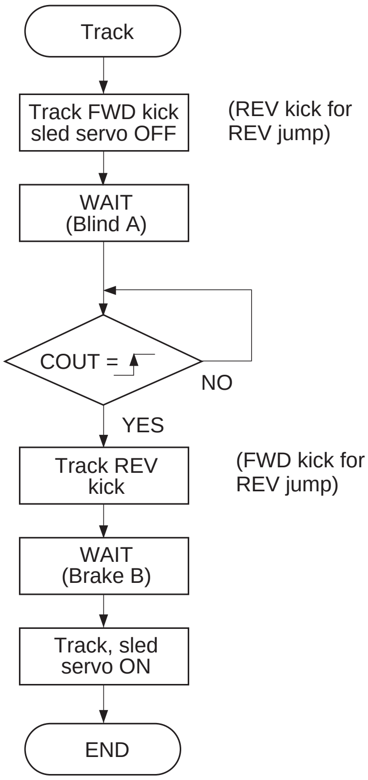



**Fig. 4-7-(a). 1-Track Jump Flow Chart**

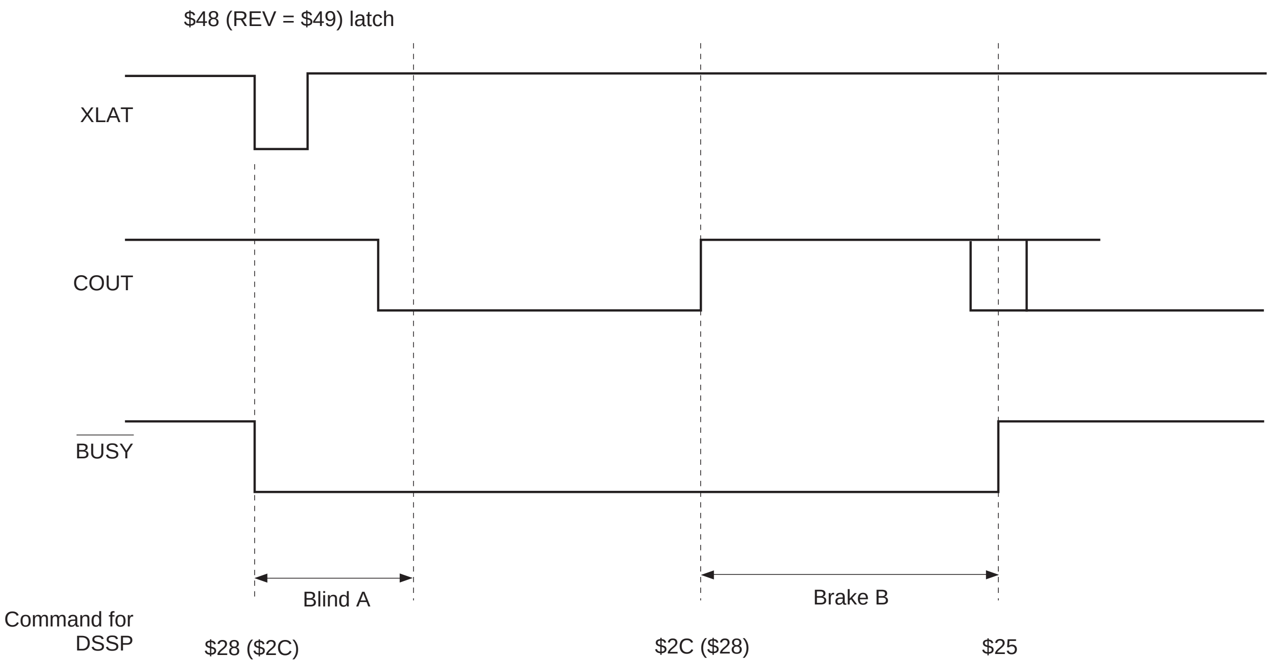



**Fig. 4-7-(b). 1-Track Jump Timing Chart**

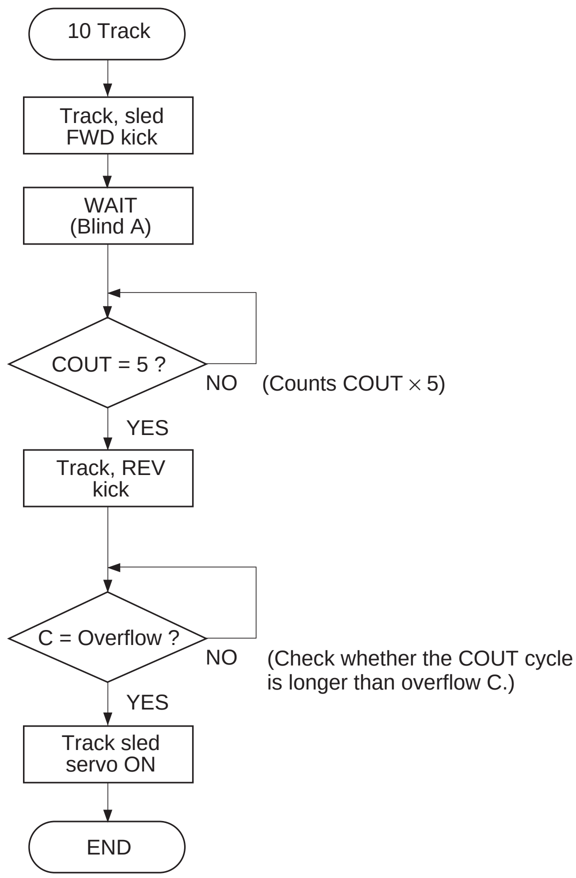



**Fig. 4-8-(a). 10-Track Jump Flow Chart**

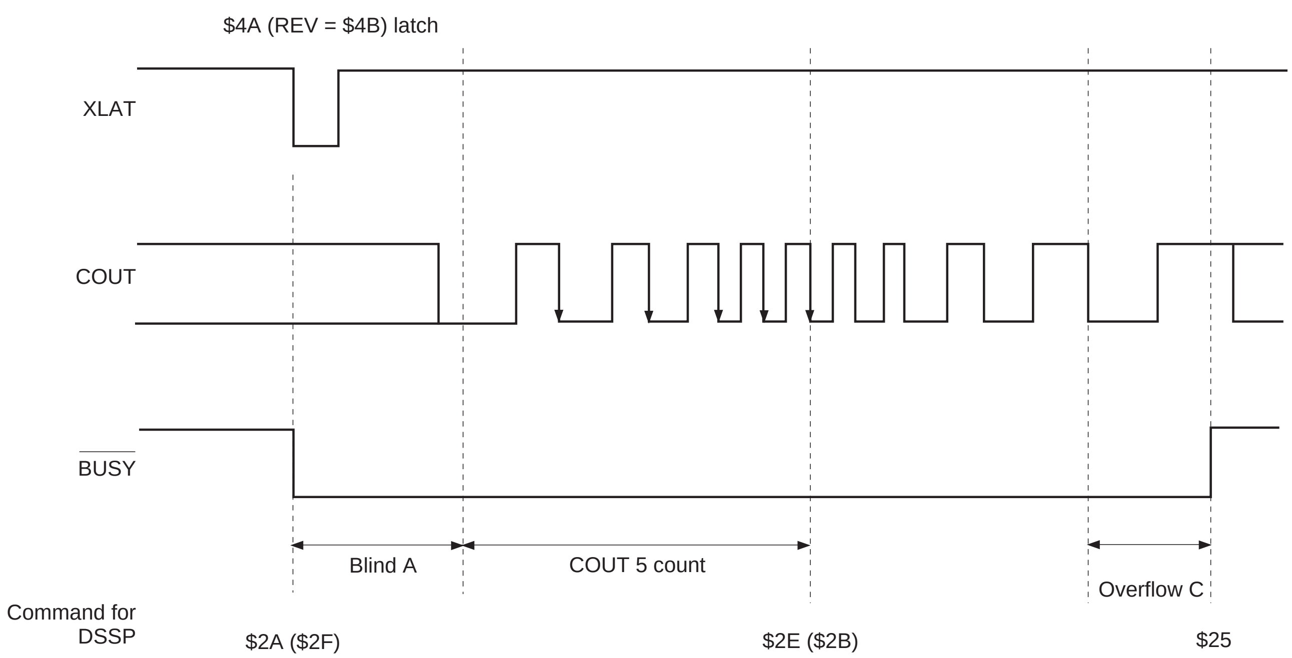



**Fig. 4-8-(b). 10-Track Jump Timing Chart**

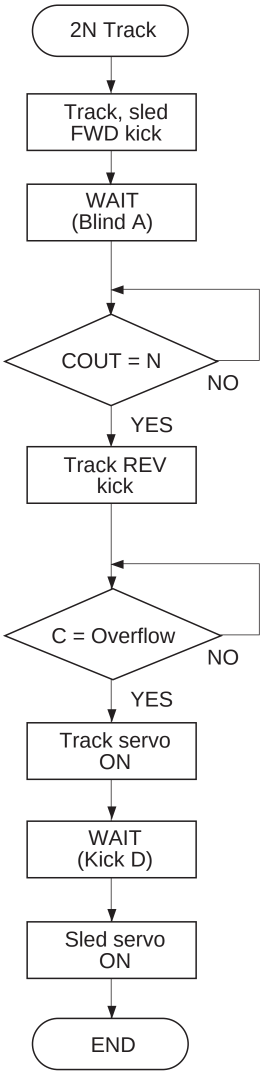



**Fig. 4-9-(a). 2N-Track Jump Flow Chart**

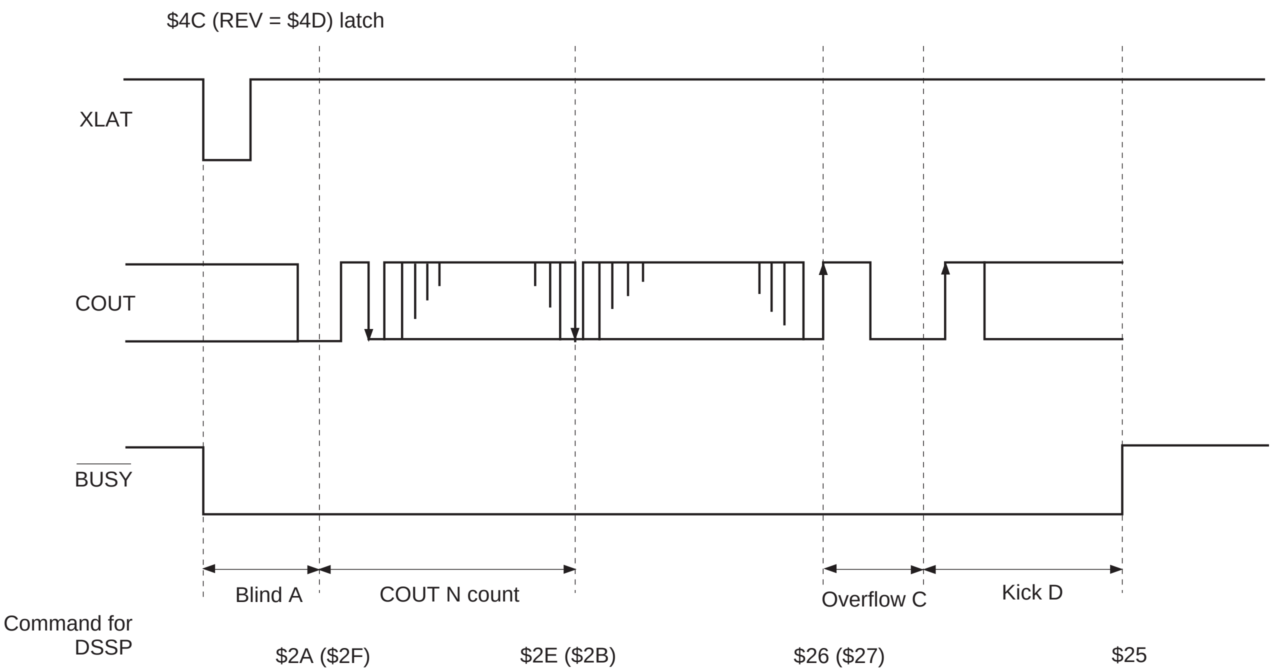



**Fig. 4-9-(b). 2N-Track Jump Timing Chart**

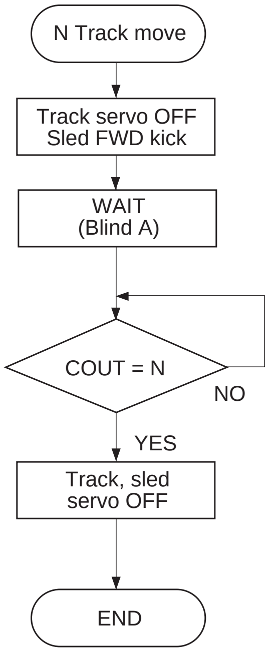



**Fig. 4-10-(a). N-Track Move Flow Chart**

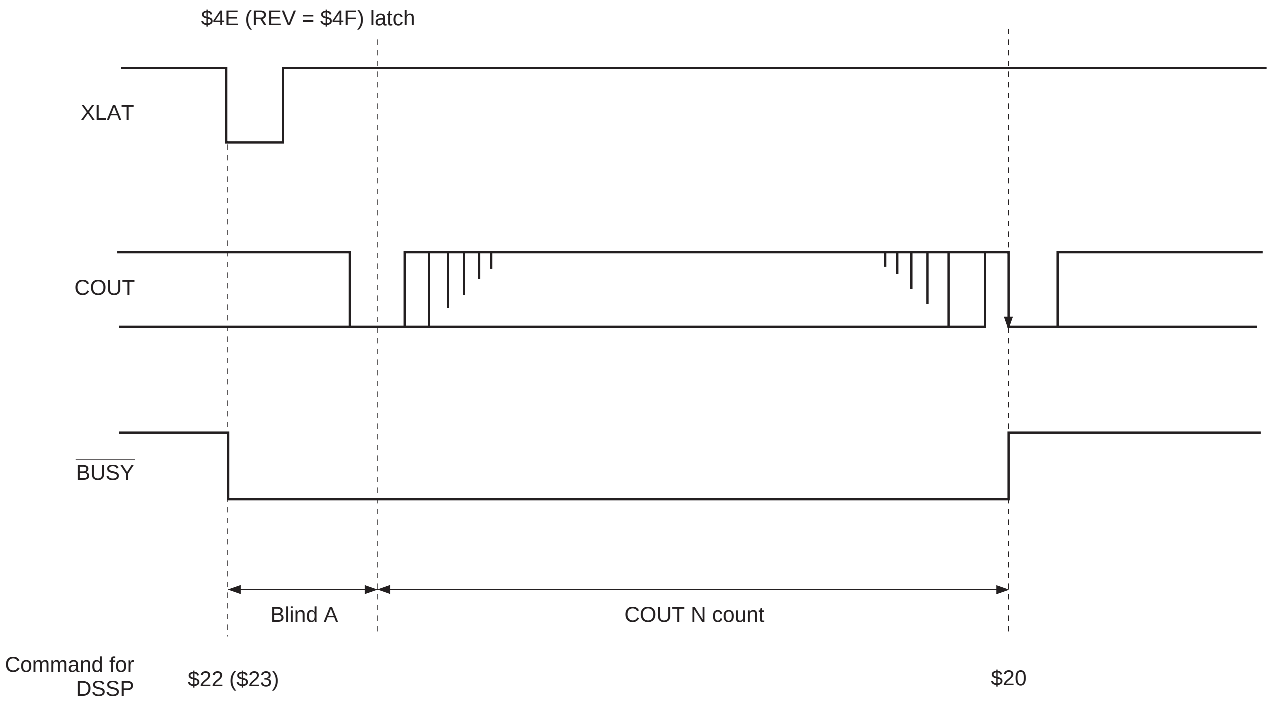
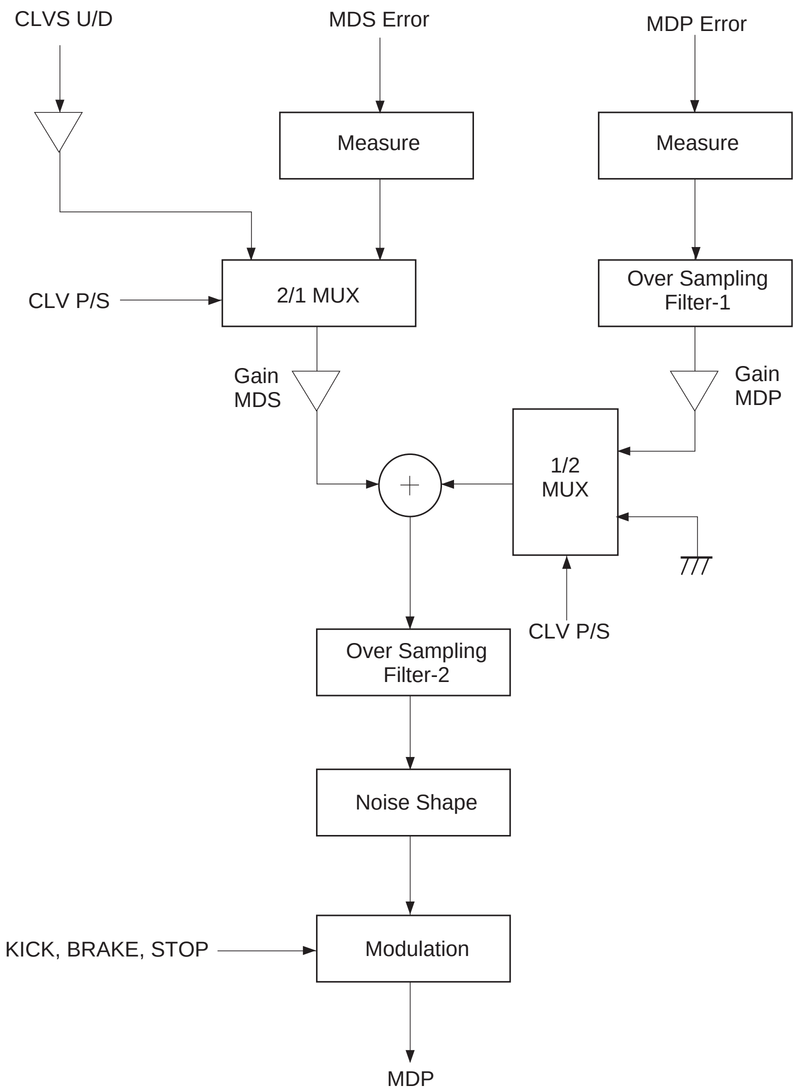



**Fig. 4-10-(b). N-Track Move Timing Chart**

**§4-7. Digital CLV**

Fig. 4-11 shows the block diagram. Digital CLV outputs MDS error and MDP error with PWM, with the sampling frequency increased up to 130Hz during normal-speed playback in CLVS, CLVP and other modes. In addition, the digital spindle servo gain is variable.

Digital CLV




CLVS U/D : Up/down signal from CLVS servo
MDS error : Frequency error for CLVP servo
MDP error : Phase error for CLVP servo

**Fig. 4-11. Block Diagram**

### §4-8. CD-DSP Block Playback Speed

In the CXD2597Q, the following playback modes can be selected through different combinations of the crystal, XTSL pin and the DSPB command of $9X.

**CD-DSP block playback speed**

| Crystal | XTSL | DSPB | CD-DSP block playback speed |
|---|---|---|---|
| 768Fs | 0 | 1 | 4×*1 |
| 768Fs | 1 | 0 | 1× |
| 768Fs | 1 | 1 | 2× |
| 384Fs | 0 | 0 | 1× |
| 384Fs | 0 | 1 | 2× |
| 384Fs | 1 | 1 | 1×*2 |

Fs = 44.1kHz.

*1 In 4× speed playback, the timer value for the auto sequence is halved.

*2 Low power consumption mode. The CD-DSP processing speed is halved, allowing power consumption to be reduced.

### §4-9. DAC Block Playback Speed

The operation speed for the DAC block is determined by the crystal and the MCSL command of $9X regardless of the CD-DSP operating conditions noted above. This allows the playback modes for the DAC and CD-DSP blocks to be set independently.

**1-bit DAC block playback speed**

| Crystal | MCSL | DAC block playback speed |
|---|---|---|
| 768Fs | 1 | 1× |
| 768Fs | 0 | 2× |
| 384Fs | 0 | 1× |

Fs = 44.1kHz.

## §4-10. Description of DAC Block Functions

### Zero data detection

When the condition where the lower 4 bits of the input data are DC and the remaining upper bits are all "0" or all "1" has continued about for 300ms, zero data is detected. Zero data detection is performed independently for the left and right channels.

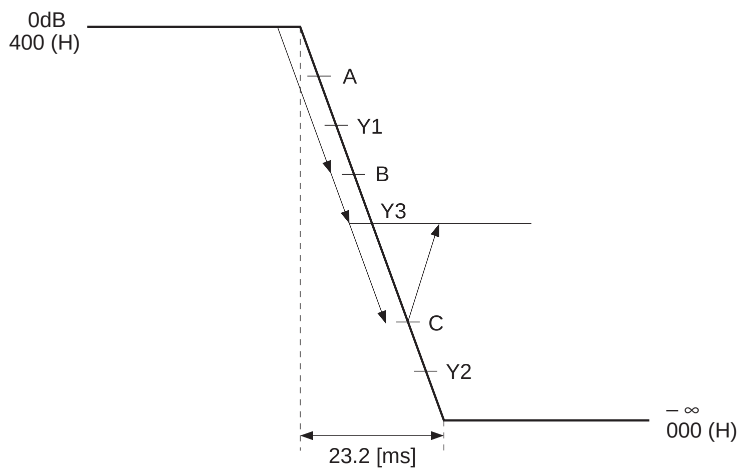
### Mute flag output

The LMUT and RMUT pins go active when any one of the following conditions is met.
The polarity can be selected with the ZDPL command of $9X.

- When zero data is detected
- When a high signal is input to the SYSM pin
- When the SMUT command of $AX is set

### Attenuation operation

Assuming the attenuation commands X1, X2 and X3, the corresponding audio outputs are Y1, Y2 and Y3 (Y1 > Y3 > Y2). First, the command X1 is sent and then the audio approaches Y1. When the command X2 is sent before the audio output reaches Y1 (A in the figure), the audio output passes Y1 and approaches Y2. And, when the command X3 is sent before the audio output reaches Y2 (B or C in the figure), the audio output approaches Y3 from the value (B or C in the figure) at that point.

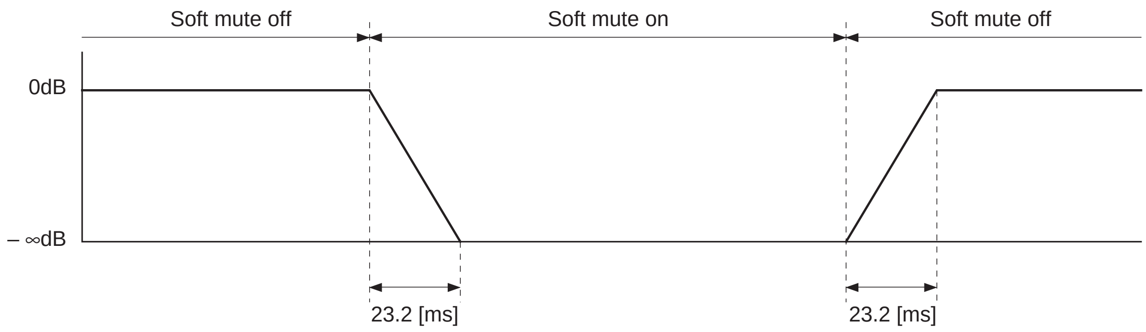


## DAC block mute operation

### Soft mute

Soft mute results and the input data is attenuated to zero when any one of the following conditions is met.

- When attenuation data of "000" (high) is set
- When the SMUT command of $AX is set to 1
- When a high signal is input to the SYSM input pin




### Forced mute

Forced mute results when the FMUT command of $AX is set to 1.
Forced mute fixes the PWM output that is input to the LPF block to low.
* When setting FMUT, set OPSL2 to 1. (See the $AX commands.)

### Zero detection mute

Forced mute is applied when the ZMUT command of $9X is set to 1 and the zero data is detected for the left and right channels.
(See "Zero data detection".)
When the ZMUT command of $9X is set to 1, the forced mute is applied even if the mute flag output condition is met. When the zero detection mute is on, set the DCOF command of $9X to 1.

**LRCK Synchronization**

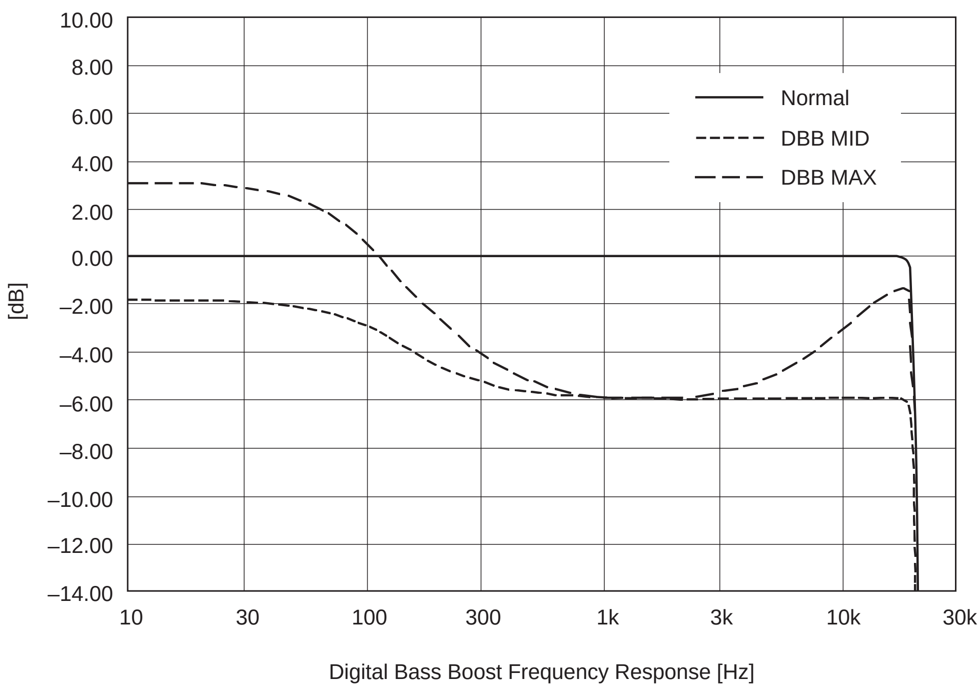
Synchronization is performed at the first falling edge of the LRCK input during reset.
After that, synchronization is lost when the LRCK input frequency changes and resynchronization must be performed.
The LRCK input frequency changes when the master clock of the LSI is switched and the playback speed changes such as the following cases.

- When the XTSL pin switches between high and low
- When the DSPB command of $9X setting changes
- When the MCSL command of $9X setting changes

For resynchronization, set the LRWO command of $AX to 1, wait for one LRCK cycle or more, and then set LRWO to 0.
* When setting LRWO, set OPSL2 to 1. (See the $AX commands.)

**Digital Bass Boost**

Bass boost without external parts is possible using the built-in digital filter. The boost strength has two levels: Mid. and Max. BSBST and BBSL of address A are used for the setting.
See Graph 4-12 for the digital bass boost frequency response.




**Graph 4-12.**

### §4-11. LPF Block

The CXD2597Q contains an initial-stage secondary active LPF with numerous resistors and capacitors and an operational amplifier with reference voltage.
The resistors and capacitors are attached externally, allowing the cut-off frequency fc to be determined flexibly.
The reference voltage ($V_C$) is ($AV_{DD} - AV_{SS}$) $\times$ 0.43.

The LPF block application circuit is shown below.
In this circuit, the cut-off frequency is fc ≈ 40kHz.

The external capacitors' values when fc = 30kHz and 50kHz are noted below as a reference.
The resistors' values do not change at this time.

- When fc ≈ 30kHz:
  C1 = 200pF, C2 = 910pF
- When fc ≈ 50kHz:
  C1 = 120pF, C2 = 560pF

**LPF Block Application Circuit**

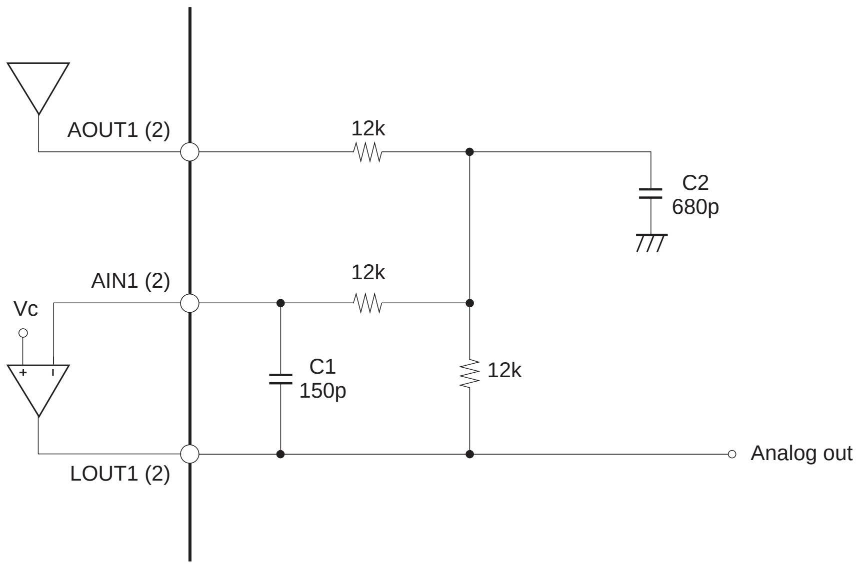



**Fig. 4-13. LPF External Circuit**

**§4-12. Asymmetry Correction**

Fig. 4-14 shows the block diagram and circuit example.

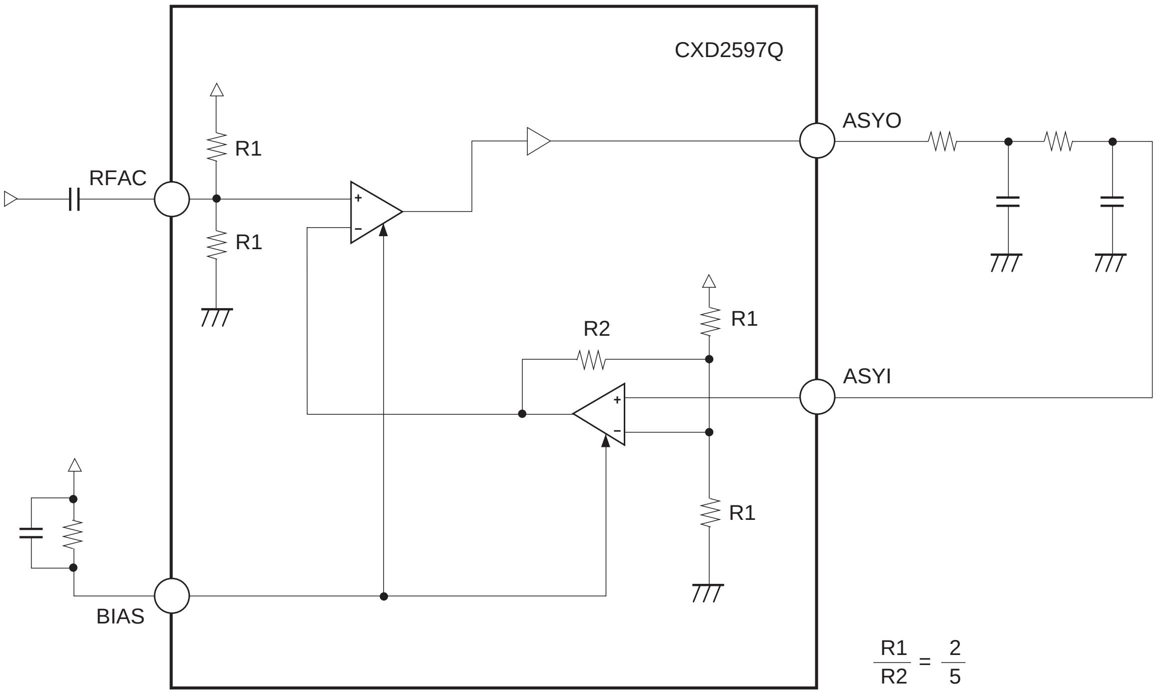



**Fig. 4-14. Asymmetry Correction Application Circuit**

**§4-13. CD TEXT Data Demodulation**

- In order to demodulate the CD TEXT data, set the command $8 Data 6 D3 TXON to 1. During TXON = 1
  It requires 26.7ms (max.) to demodulate the CD TEXT data correctly after TXON is set to 1.
- The CD TEXT data is output by switching the SQSO pin with the command. The CD TEXT data output is enabled by setting the command $8 Data 6 D2 TXOUT to 1. To read data, the readout clock should be input to SQCK.
- The readable data are the CRC counting results for the each pack and the CD TEXT data (16 bytes) except for CRC data.
- When the CD TEXT data is read, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.
- Data which can be stored in the LSI is 1 packet (4 packs).

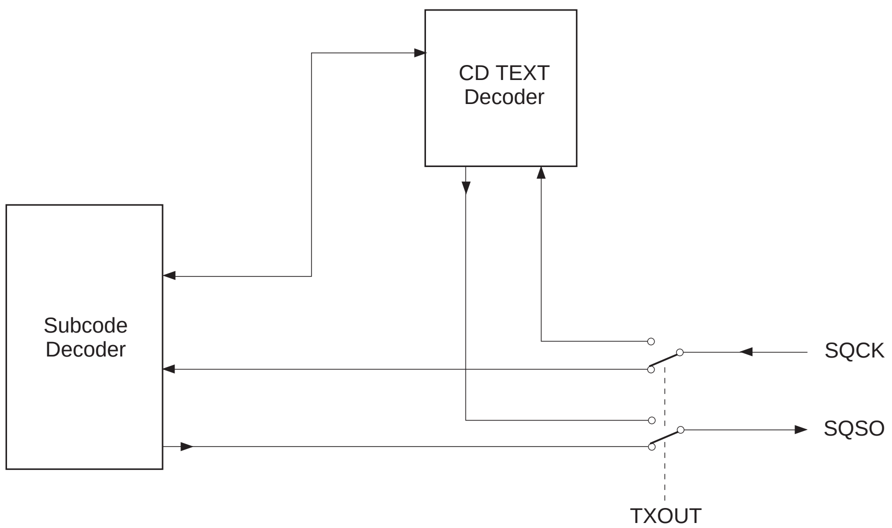



**Fig. 4-15. Block Diagram of CD TEXT Demodulation Circuit**

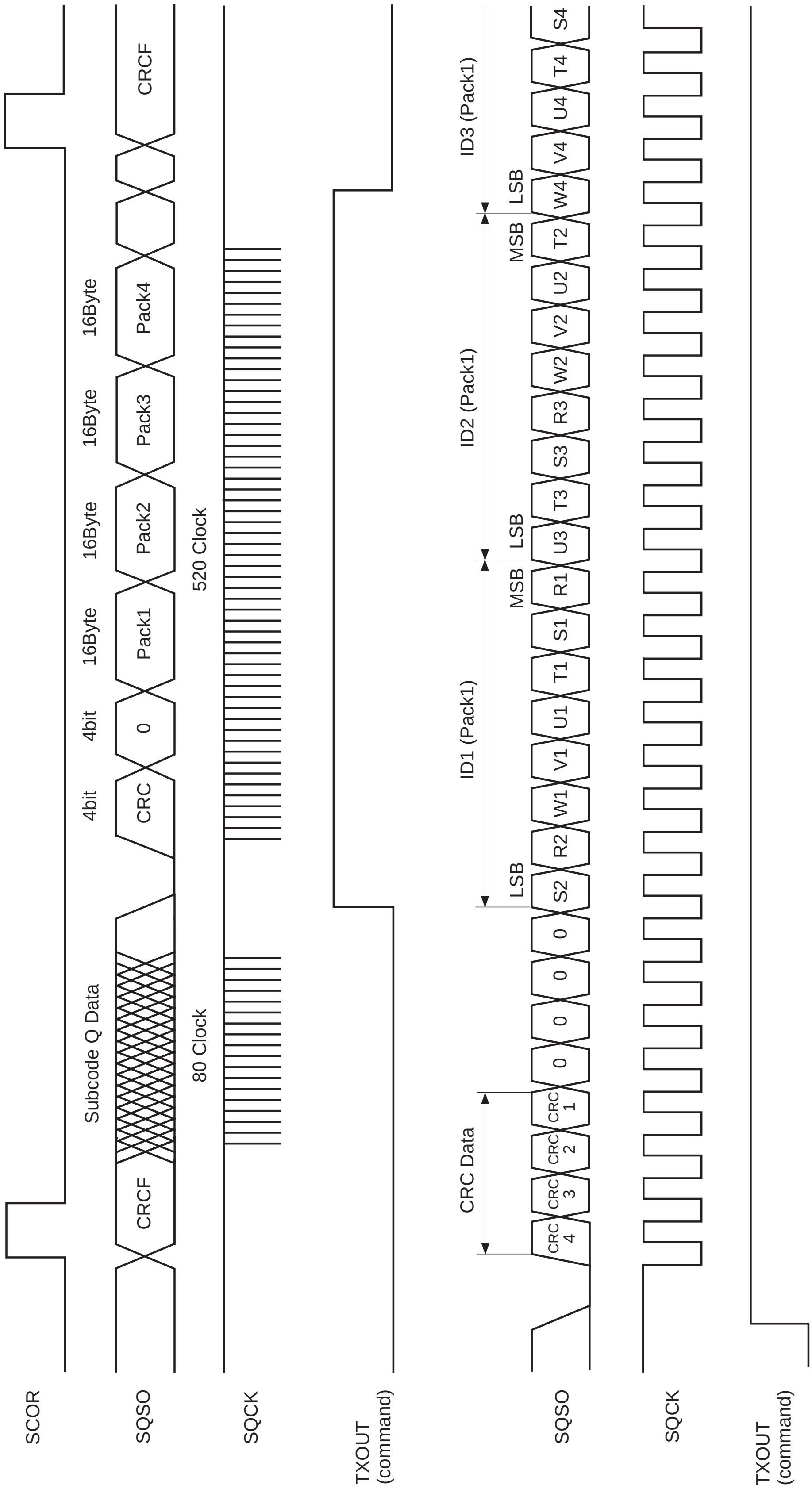



**Fig. 4-16. CD TEXT Data Timing Chart**

## §5. Description of Servo Signal Processing System Functions and Commands

### §5-1. General Description of Servo Signal Processing System ($V_{DD}$: Supply voltage)

Focus servo

| | |
|---|---|
| Sampling rate: | 88.2kHz (when MCK = 128Fs) |
| Input range: | $0.3V_{DD}$ to $0.7V_{DD}$ |
| Output format: | 7-bit PWM |
| Others: | Offset cancel<br>Focus bias adjustment<br>Focus search<br>Gain-down function<br>Defect countermeasure<br>Auto gain control |

Tracking servo

| | |
|---|---|
| Sampling rate: | 88.2kHz (when MCK = 128Fs) |
| Input range: | $0.3V_{DD}$ to $0.7V_{DD}$ |
| Output format: | 7-bit PWM |
| Others: | Offset cancel<br>E:F balance adjustment<br>Track jump<br>Gain-up function<br>Defect countermeasure<br>Drive cancel<br>Auto gain control<br>Vibration countermeasure |

Sled servo

| | |
|---|---|
| Sampling rate: | 345Hz (when MCK = 128Fs) |
| Input range: | $0.3V_{DD}$ to $0.7V_{DD}$ |
| Output format: | 7-bit PWM |
| Others: | Sled move |

FOK, MIRR, DFCT signals generation

| | |
|---|---|
| RF signal sampling rate: | 1.4MHz (when MCK = 128Fs) |
| Input range: | $0.43V_{DD}$ to $V_{DD}$ |
| Others: | RF zero level automatic measurement |

**§5-2. Digital Servo Block Master Clock (MCK)**

The clock with the 2/3 frequency of the crystal is supplied to the digital servo block.

The XT4D and XT2D commands can be set with D13 and D12 of $3F, and the XT1D command can be set with D1 of $3E. (Default = 0)

The digital servo block is designed with an MCK frequency of 5.6448MHz (128Fs) as typical.

| Mode | XTLI | Input to servo | XTSL | XT4D | XT2D | XT1D | Frequency division ratio | MCK |
|---|---|---|---|---|---|---|---|---|
| 1 | 384Fs | 256Fs | ∗ | ∗ | ∗ | 1 | 1 | 256Fs |
| 2 | 384Fs | 256Fs | ∗ | ∗ | 1 | 0 | 1/2 | 128Fs |
| 3 | 384Fs | 256Fs | 0 | 0 | 0 | 0 | 1/2 | 128Fs |
| 4 | 768Fs | 512Fs | ∗ | ∗ | ∗ | 1 | 1 | 512Fs |
| 5 | 768Fs | 512Fs | ∗ | ∗ | 1 | 0 | 1/2 | 256Fs |
| 6 | 768Fs | 512Fs | ∗ | 1 | 0 | 0 | 1/4 | 128Fs |
| 7 | 768Fs | 512Fs | 1 | 0 | 0 | 0 | 1/4 | 128Fs |

Fs = 44.1kHz, ∗: Don't care

**Table 5-1.**

**§5-3. AVRG (Average) Measurement and Compensation**

The CXD2597Q has a circuit that measures the averages of RFDC, VC, FE and TE and a circuit that compensates these signals to control the servo effectively.

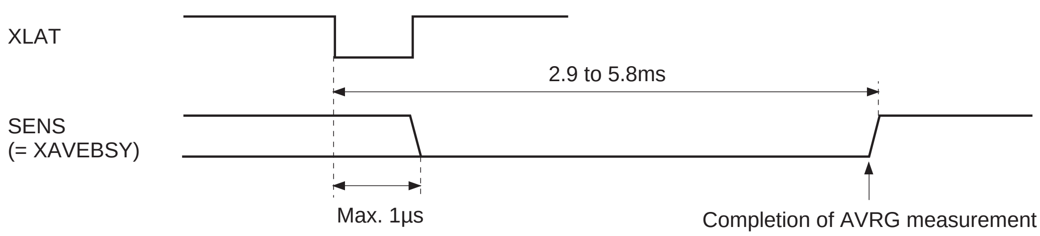
AVRG measurement and compensation is necessary to initialize the CXD2597Q, and is able to cancel the offset.

The level applied to the VC, FE, RFDC and TE pins can be measured by setting D15 (VCLM), D13 (FLM), D11 (RFLM) and D4 (TCLM) of $38 respectively to 1.

AVRG measurement takes the level applied to each analog input pin as the average of 256 samples, and then loads each value into the AVRG register.

AVRG measurement requires approximately 2.9ms to 5.8ms (when MCK = 128Fs) after the command is received.

During AVRG measurement, if the upper 8 bits of the command register are 38 (Hex), the completion of AVRG measurement operation can be confirmed through the SENS pin. (See Timing Chart 5-2.)




**Timing Chart 5-2.**

**<Measurement>**

• VC AVRG
The offset can be canceled by measuring the VC level which is the center voltage for the system and using that value to apply compensation to each input error signal.

• FE AVRG
The FE signal DC level is measured. In addition, compensation is applied to the FZC comparator level output from the SENS pin during FCS SEARCH (focus search) using these measurement results.

• TE AVRG
The TE signal DC level is measured.

• RF AVRG
The MIRR, DFCT and FOK signals are generated from the RF signal. Since the FOK signal is generated by comparing the RF signal at a certain level, it is necessary to establish a zero level which becomes the comparator level reference. Therefore, the RF signal is measured before playback, and is compensated to take this level as the zero level.

An example of sending AVRG measurement and compensation commands is shown below.
(Example) $380800 (RF AVRG measurement on)
$382000 (FE AVRG measurement on)
$380010 (TE AVRG measurement on)
$388000 (VC AVRG measurement on)
(Complete each AVRG measurement before starting the next.)
$38140A (RFLC, FLC0, FLC1 and TLC1 commands on)
(The required compensation should be turned on together; see Fig. 5-3.)
An interval of 5.8ms (when MCK = 128Fs) or more must be maintained between each command, or the SENS pin must be monitored to confirm that the previous command has been completed before the next AVRG command is sent.

**<Compensation>**

See Fig. 5-3 for the contents of each compensation below.

• RFLC
The difference by which the RF signal exceeds the RF AVRG value is input to the RF In register.
(00 is input when the RF signal is lower than the RF AVRG value.)
• TCL0
The value obtained by subtracting the VC AVRG value from the TE signal is input to the TRK In register.
• TCL1
The value obtained by subtracting the TE AVRG value from the TE signal is input to the TRK In register.
• VCLC
The value obtained by subtracting the VC AVRG value from the FE signal is input to the FCS In register.
• FLC1
The value obtained by subtracting the FE AVRG value from the FE signal is input to the FCS In register.
• FLC0
The value obtained by subtracting the FE AVRG value from the FE signal is input to the FZC register.

**§5-4. E:F Balance Adjustment Function**

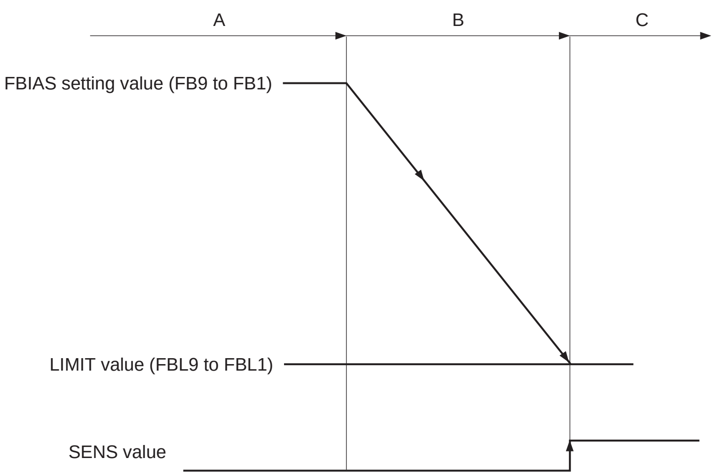
When the disc is rotated with the laser on, and with the FCS (focus) servo on via FCS Search (focus search), the traverse waveform appears in the TE signal due to disc eccentricity.
In this condition, the low-frequency component can be extracted from the TE signal using the built-in TRK hold filter by setting D5 (TBLM) of $38 to 1.
The extracted low-frequency component is loaded into the TRVSC register as a digital value, and the TRVSC register value is established when TBLM returns to 0.
Next, setting D2 (TLC2) of $38 to 1 compensates TE and SE values with the TRVSC register value (subtraction), making the E:F balance offset to be adjusted as a result. (See Fig. 5-3.)

**§5-5. FCS Bias (Focus Bias) Adjustment Function**

The FBIAS register value can be added to the FCS servo filter input by setting D14 (FBON) of $3A to 1. (See Fig. 5-3.)
When the FBIAS register value is set when D11 = 0 and D10 = 1 with $34F, data can be written using the 9-bit value of D9 to D1 (D9: MSB).
In addition, the RF jitter can be monitored by setting the SOCT command of $8 to 1. (See "DSP Block Timing Chart".)

The FBIAS register can be used as a counter by setting D13 (FBSS) of $3A to 1. The FBIAS register functions as an up counter when D12 (FBUP) of $3A = 1, and as a down counter when D12 (FBUP) of $3A = 0.
The number of up and down steps can be changed by setting D11 and D10 (FBV1 and FBV0) of $3A.

When using the FBIAS register as a counter, the counter stops if the FCSBIAS value and the value set beforehand in FBL9 to FBL1 of $34 matches. Also, if the upper 8 bits of the command register are $3A at this time, SENS becomes high and the counter stop can be monitored.




Here, assume the FBIAS setting value FB9 to FB1 and the FBIAS LIMIT value FBL9 to FBL1 like status A. For example, if command registers FBUP = 0, FBV1 = 0, FBV0 = 0 and FBSS = 1 are set from this status, down count starts from status A and approaches the set LIMIT value. When the FCSBIAS value matches FBL9 to FBL1, the counter stops and the SENS pin goes to high. Note that the up/down counter counts at each sampling cycle of the focus servo filter. The number of steps by which the count value changes can be selected from 1, 2, 4 or 8 steps by FBV1 and FBV0. When converted to FE input, 1 step corresponds to $1/512 \times V_{DD} \times 0.4$.

A: Register mode
B: Counter mode
C: Counter mode (when stopped)

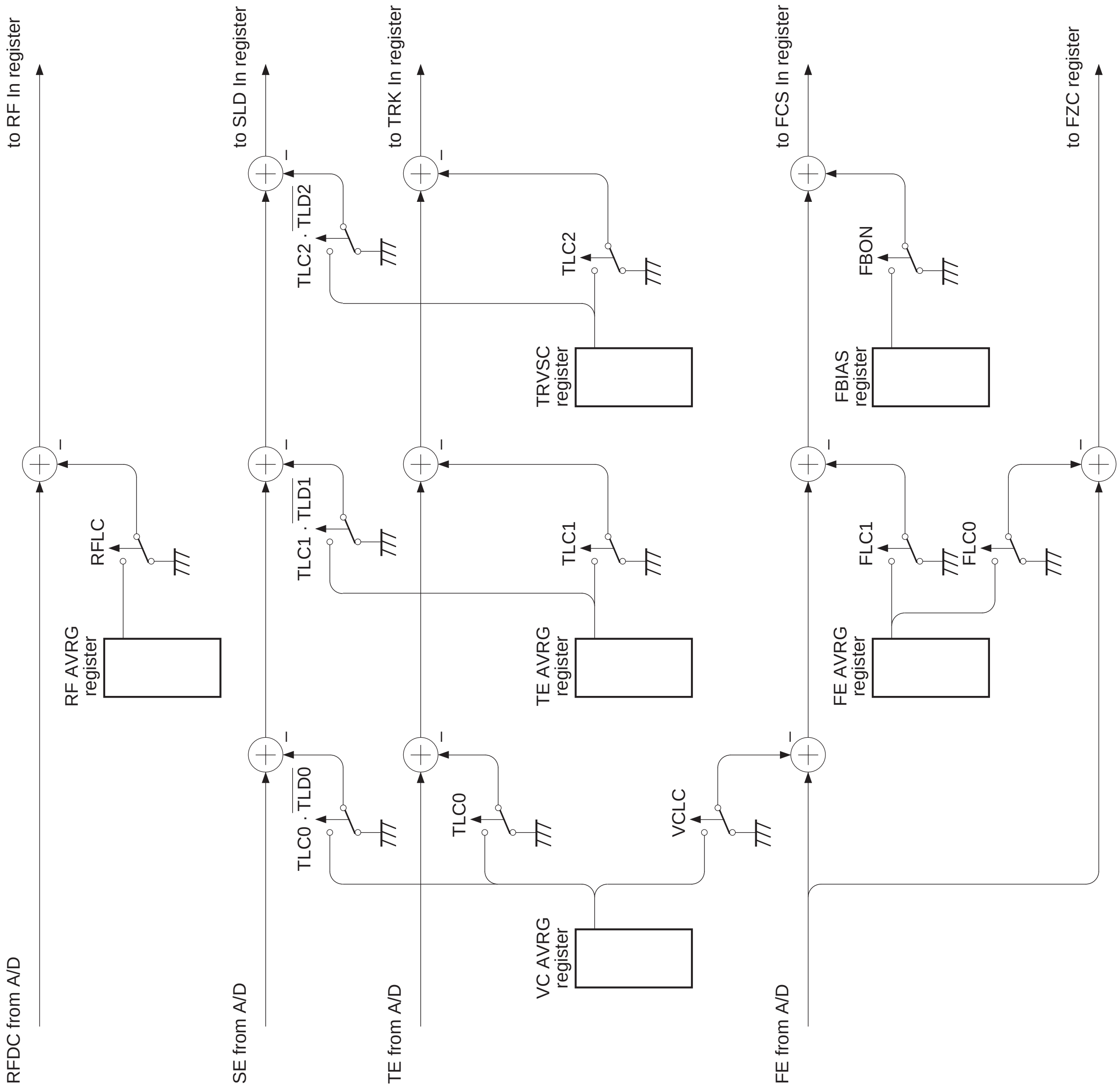
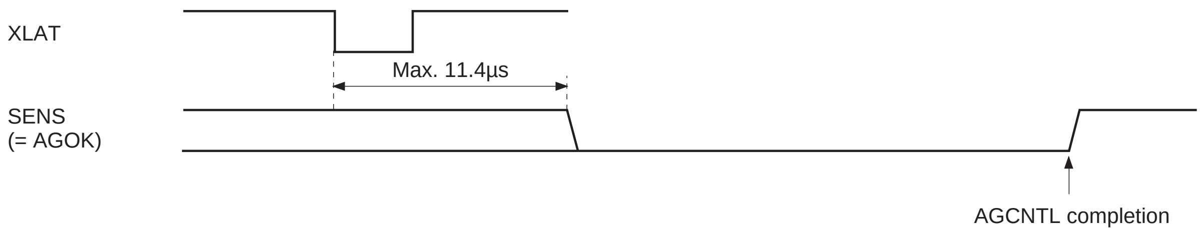

RFDC from A/D
to RF In register
RF AVRG register
RFLC
SE from A/D
to SLD In register
TLC0 · TLD0
TLC1 · TLD1
TLC2 · TLD2
TE from A/D
to TRK In register
TLC0
TLC1
TLC2
VC AVRG register
TE AVRG register
TRVSC register
VCLC
FE from A/D
to FCS In register
FE AVRG register
FBIAS register
FLC1
FLC0
FBON
to FZC register

**Fig. 5-3.**

### §5-6. AGCNTL (Automatic Gain Control) Function

The AGCNTL function automatically adjusts the filter internal gain in order to obtain the appropriate servo loop gain. AGCNTL not only copes with the sensitivity variation of the actuator and photo diode, etc., but also obtains the optimal gain for each disc.
The AGCNTL command is sent when each servo is turned on. During AGCNTL operation, if the upper 8 bits of the command register are 38 (Hex), the completion of AGCNTL operation can be confirmed through the SENS pin. (See Timing Chart 5-4 and "Description of SENS Signals".)
Setting D9 and D8 of $38 to 1 set FCS (focus) and TRK (tracking) respectively to AGCNTL operation.

**Note)** During AGCNTL operation, each servo filter gain must be normal, and the anti-shock circuit (described hereafter) must be disabled.




**Timing Chart 5-4.**

Coefficient K13 changes for AGF (focus AGCNTL) and coefficients K23 and K07 change for AGT (tracking AGCNTL) due to AGCNTL.
These coefficients change from 01 to 7F (Hex), and they must also be set within this range when written externally.
After AGCNTL operation has completed, these coefficient values can be confirmed by reading them out from the SENS pin with the serial readout function (described hereafter).

AGCNTL related settings

The following settings can be changed with $35, $36 and $37.

| | |
|---|---|
| FG6 to FG0; | AGF convergence gain setting, effective setting range: 00 to 57 (Hex) |
| TG6 to TG0; | AGT convergence gain setting, effective setting range: 00 to 57 (Hex) |
| AGS; | Self-stop on/off |
| AGJ; | Convergence completion judgment time |
| AGGF; | Internally generated sine wave amplitude (AGF) |
| AGGT; | Internally generated sine wave amplitude (AGT) |
| AGV1; | AGCNTL sensitivity 1 (during rough adjustment) |
| AGV2; | AGCNTL sensitivity 2 (during fine adjustment) |
| AGHS; | Rough adjustment on/off |
| AGHT; | Fine adjustment time |

**Note)** Converging servo loop gain values can be changed with the FG6 to FG0 and TG6 to TG0 setting values. In addition, these setting values must be within the effective setting range. The default settings aim for 0 dB at 1kHz. However, since convergence values vary according to the characteristics of each constituent element of the servo loop, FG and TG values should be set as necessary.

AGCNTL and default operation have two stages.
In the first stage, rough adjustment is performed with high sensitivity for a certain period of time (select 256/128ms with AGHT, when MCK = 128Fs), and the AGCNTL coefficient approaches the appropriate value. The sensitivity at this time can be selected from two types with AGV1.
In the second stage, the AGCNTL coefficient is finely adjusted to approach more appropriate value with relatively low sensitivity. The sensitivity for the second stage can be selected from two types with AGV2. In the second stage of default operation, when the AGCNTL coefficient reaches the appropriate value and stops changing, the CXD2597Q confirms that the AGCNTL coefficient has not changed for a certain period of time (select 63/31ms with AGHJ, when MCK = 128Fs), and then completes AGCNTL operation. (Self-stop mode)
This self-stop mode can be canceled by setting AGS to 0.
In addition, the first stage is omitted for AGCNTL operation when AGHS is set to 0.
An example of AGCNTL coefficient transitions during AGCNTL in various settings are shown in Fig. 5-5.

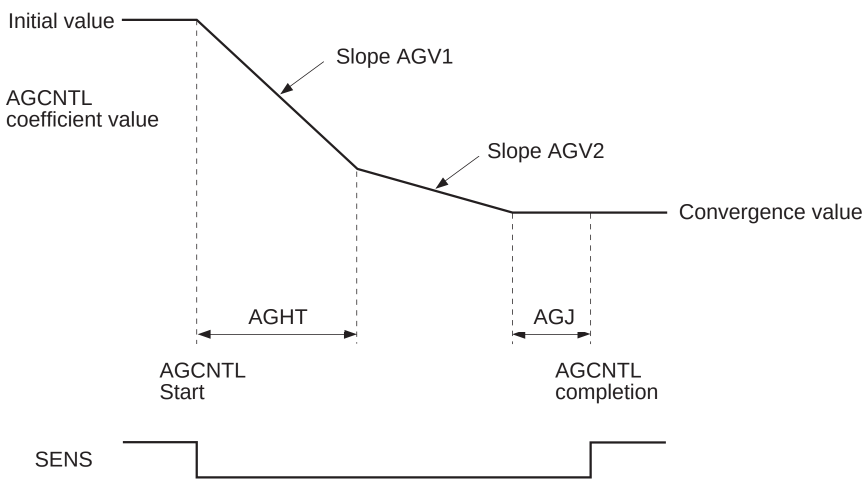



**Fig. 5-5.**

**Note)** Fig. 5-5 shows the example where the AGCNTL coefficient value converges to the smaller value from the initial value.

**§5-7. FCS Servo and FCS Search (Focus Search)**

The FCS servo is controlled by the 8-bit serial command $0X. (See Table 5-6.)

| Register name | Command | D23 to D20 | D19 to D16 | |
|---|---|---|---|---|
| 0 | FOCUS CONTROL | 0 0 0 0 | 1 0 * * | FOCUS SERVO ON (FOCUS GAIN NORMAL) |
| | | | 1 1 * * | FOCUS SERVO ON (FOCUS GAIN DOWN) |
| | | | 0 * 0 * | FOCUS SERVO OFF, 0V OUT |
| | | | 0 * 1 * | FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT |
| | | | 0 * 1 0 | FOCUS SEARCH VOLTAGE DOWN |
| | | | 0 * 1 1 | FOCUS SEARCH VOLTAGE UP |

*: Don't care

**Table 5-6.**

**FCS Search**

FCS search is required in the course of turning on the FCS servo.

Fig. 5-7 shows the signals for sending commands $00 → $02 → $03 and performing only FCS search operation.
Fig. 5-8 shows the signals for sending $08 (FCS on) after that.

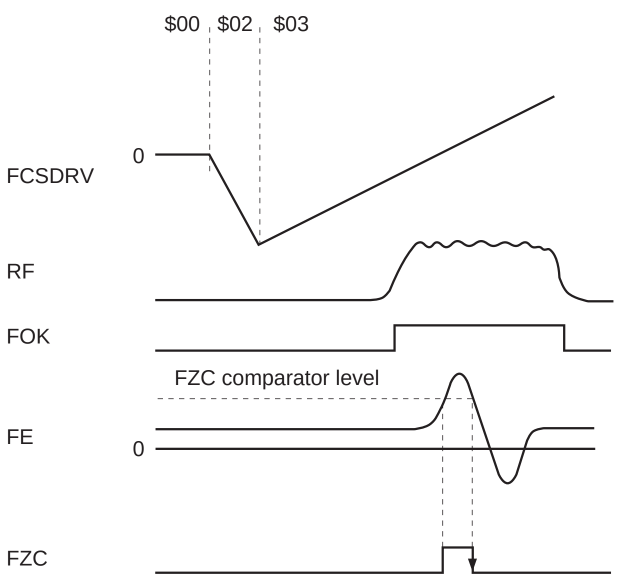



**Fig. 5-7.**

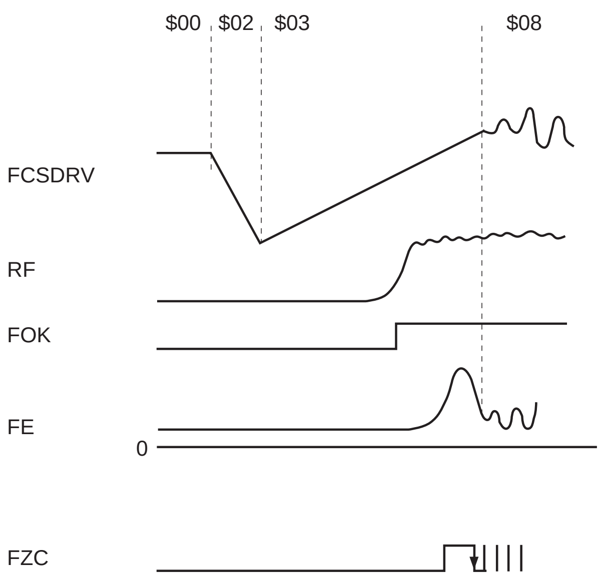



**Fig. 5-8.**

### §5-8. TRK (Tracking) and SLD (Sled) Servo Control

The TRK and SLD servos are controlled by the 8-bit command $2X. (See Table 5-9.)
When the upper 4 bits of the serial data are 2 (Hex), TZC is output to the SENS pin.

| Register name | Command | D23 to D20 | D19 to D16 | |
|---|---|---|---|---|
| 2 | TRACKING MODE | 0 0 1 0 | 0 0 ∗ ∗ | TRACKING SERVO OFF |
| | | | 0 1 ∗ ∗ | TRACKING SERVO ON |
| | | | 1 0 ∗ ∗ | FORWARD TRACK JUMP |
| | | | 1 1 ∗ ∗ | REVERSE TRACK JUMP |
| | | | ∗ ∗ 0 0 | SLED SERVO OFF |
| | | | ∗ ∗ 0 1 | SLED SERVO ON |
| | | | ∗ ∗ 1 0 | FORWARD SLED MOVE |
| | | | ∗ ∗ 1 1 | REVERSE SLED MOVE |

∗: Don't care

**Table 5-9.**

**TRK Servo**

The TRK JUMP (track jump) level can be set with 6 bits (D13 to D8) of $36.
In addition, when the TRK servo is on and D17 of $1 is set to 1, the TRK servo filter switches to gain-up mode. The filter also switches to gain-up mode when the LOCK signal goes low or when vibration is detected with the anti-shock circuit (described hereafter) enabled.
The CXD2597Q has two types of filters in TRK gain-up mode which can be selected by setting D16 of $1. (See Table 5-17.)

**SLD Servo**

The SLD MOV (sled move) output, composed of a basic value from 6 bits (D13 to D8) of $37, is determined by multiplying this value by 1×, 2×, 3× or 4× magnification set using D17 and D16 when D18 = D19 = 0 is set with $3. (See Table 5-10.)
SLD MOV must be performed continuously for 50µs or more. In addition, if the LOCK input signal goes low when the SLD servo is on, the SLD servo turns off.

**Note)** When the LOCK signal is low, the TRK servo switches to gain-up mode and the SLD servo is turned off by the default. These operations are disabled by setting D6 (LKSW) of $38 to 1.

| Register name | Command | D23 to D20 | D19 to D16 | |
|---|---|---|---|---|
| 3 | SELECT | 0 0 1 1 | 0 0 0 0 | SLED KICK LEVEL (basic value × ±1) |
| | | | 0 0 0 1 | SLED KICK LEVEL (basic value × ±2) |
| | | | 0 0 1 0 | SLED KICK LEVEL (basic value × ±3) |
| | | | 0 0 1 1 | SLED KICK LEVEL (basic value × ±4) |

**Table 5-10.**

## §5-9. MIRR and DFCT Signal Generation

The RF signal obtained from the RFDC pin is sampled at approximately 1.4MHz (when MCK = 128Fs) and loaded. The MIRR and DFCT signals are generated from this RF signal.

### MIRR Signal Generation

The loaded RF signal is applied to the peak hold and bottom hold circuits.
An envelope is generated from the waveforms generated in these circuits, and the MIRR comparator level is generated from the average of this envelope waveform.
The MIRR signal is generated by comparing the waveform generated by subtracting the bottom hold value from the peak hold value with this MIRR comparator level. (See Fig. 5-11.)
The bottom hold speed and mirror sensitivity can be selected from 4 values using D7 and D6, and D5 and D4, respectively, of $3C.

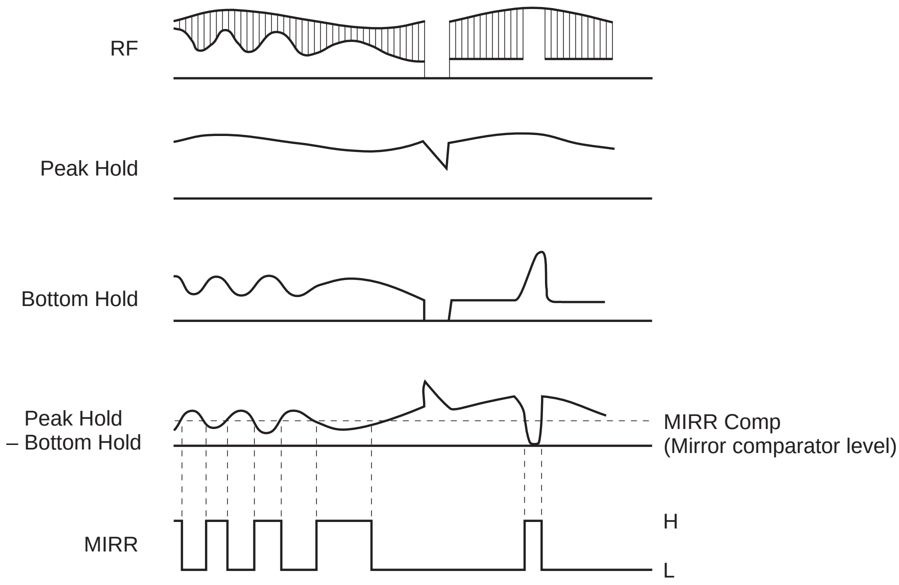



**Fig. 5-11.**

### DFCT Signal Generation

The loaded RF signal is input to two peak hold circuits with different time constants, and the DFCT signal is generated by comparing the difference between these two peak hold waveforms with the DFCT comparator level. (See Fig. 5-12.)
The DFCT comparator level can be selected from four values using D13 and D12 of $3B.

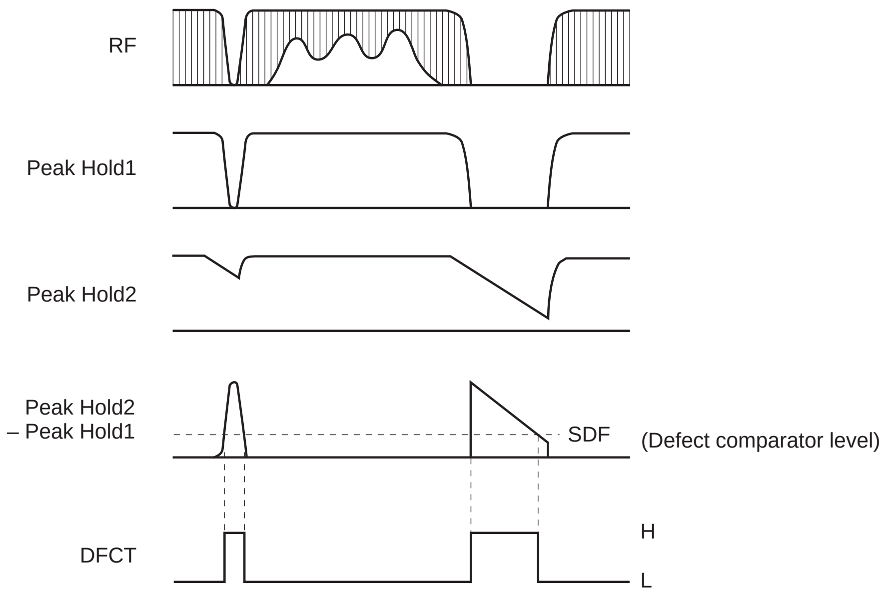



**Fig. 5-12.**

**§5-10. DFCT Countermeasure Circuit**

The DFCT countermeasure circuit maintains the directionality of the servo so that the servo does not become easily dislocated due to scratches or defects on discs.

Specifically, these operations are achieved by detecting scratch and defect with the DFCT signal generation circuit, and when DFCT goes high, applying the low-frequency component of the error signal before DFCT went high to the FCS and TRK servo filter inputs. (See Fig. 5-13.)

In addition, these operations are activated by the default. They can be disabled by setting D7 (DFSW) of $38 to 1.

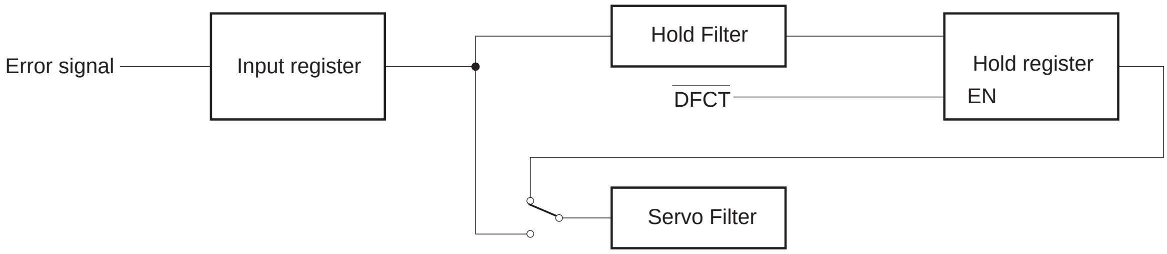



**Fig. 5-13.**

**§5-11. Anti-Shock Circuit**

When vibrations occurs in the CD player, this circuit forces the TRK filter to switch to gain-up mode so that the servo does not become easily dislocated. This circuit is for systems which require vibration countermeasures.

Concretely, vibrations are detected using an internal anti-shock filter and comparator circuit, and the gain is increased. (See Fig. 5-14.)

The comparator level is fixed to 1/16 of the maximum comparator input amplitude. However, the comparator level is practically variable by adjusting the value of the anti-shock filter output coefficient K35.

This function can be turned on and off by D19 of $1 when the brake circuit (described hereafter) is off. (See Table 5-17.)

This circuit can also support an external vibration detection circuit, and can set the TRK servo filter to gain-up mode by inputting high level to the ATSK pin.

When the upper 4 bits of the command register are 1 (Hex), vibration detection can be monitored from the SENS pin. It also can be monitored from the ATSK pin by setting the ASOT command of $3F.

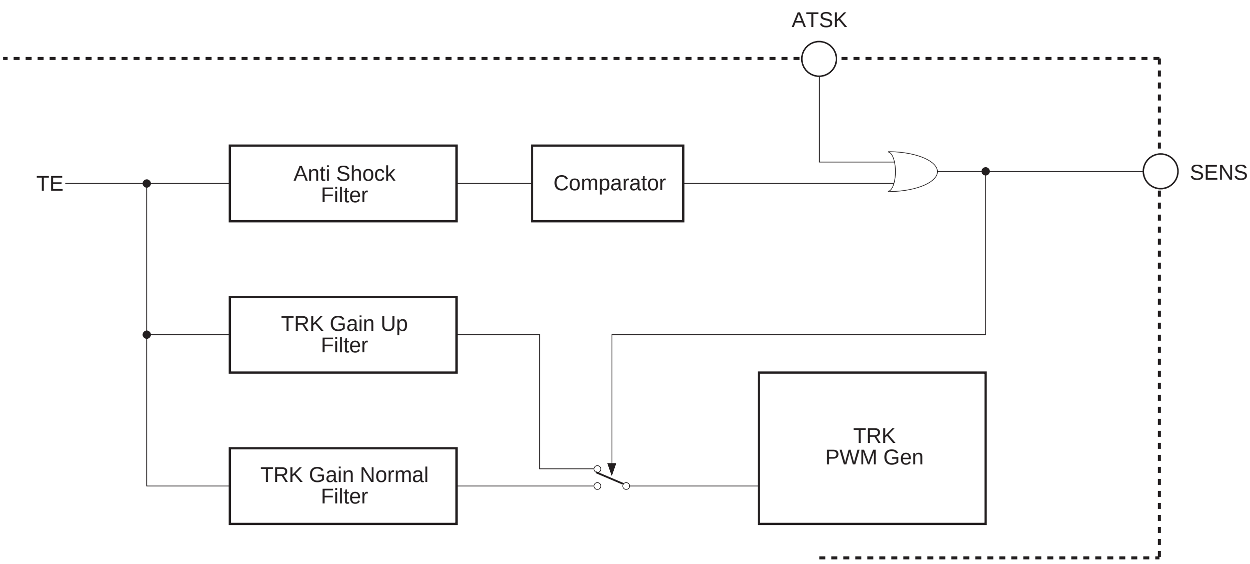



**Fig. 5-14.**

**§5-12. Brake Circuit**

Immediately after a long distance track jump it tends to be hard for the actuator to settle and for the servo to turn on.

The brake circuit prevents these phenomenon.

The brake circuit is to use tracking drive as a brake by cutting unnecessary portions of it utilizing the 180° offset in the RF envelope and tracking error phase relationship which occurs when the actuator traverses the track in the radial direction from the inner track to the outer track and vice versa. (See Figs. 5-15 and 5-16.)

Concretely, this operation is achieved by masking the tracking drive using the TRKCNCL signal generated by loading the MIRR signal at the edge of the TZC (Tracking Zero Cross) signal.

The brake circuit can be turned on and off by D18 of $1. (See Fig. 5-17.)

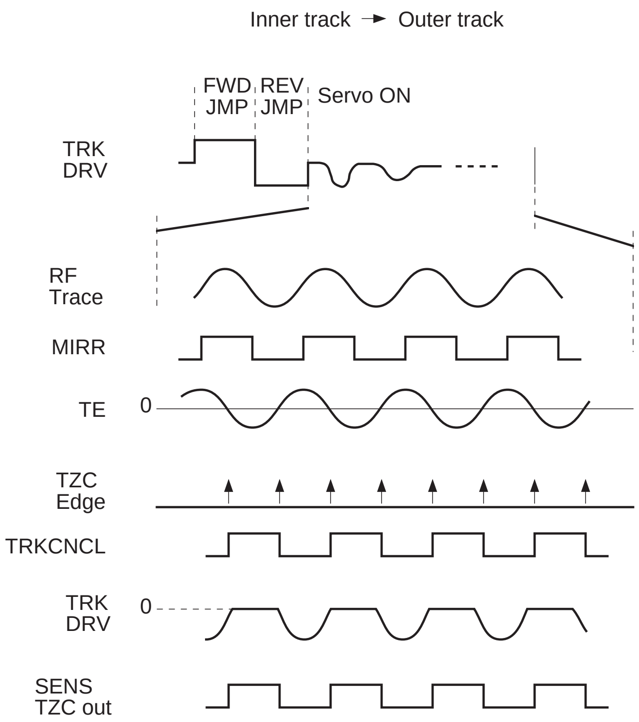



Fig. 5-15.

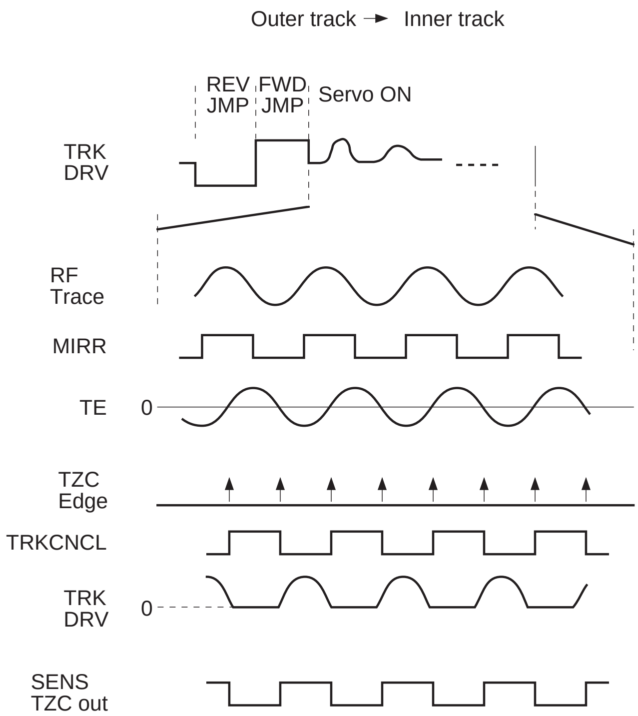



Fig. 5-16.

| Register name | Command | D23 to D20 | D19 to D16 | |
|---|---|---|---|---|
| 1 | TRACKING CONTROL | 0 0 0 1 | 1 0 ∗ ∗ | ANTI SHOCK ON |
| | | | 0 ∗ ∗ ∗ | ANTI SHOCK OFF |
| | | | ∗ 1 ∗ ∗ | BRAKE ON |
| | | | ∗ 0 ∗ ∗ | BRAKE OFF |
| | | | ∗ ∗ 0 ∗ | TRACKING GAIN NORMAL |
| | | | ∗ ∗ 1 ∗ | TRACKING GAIN UP |
| | | | ∗ ∗ ∗ 1 | TRACKING GAIN UP FILTER SELECT 1 |
| | | | ∗ ∗ ∗ 0 | TRACKING GAIN UP FILTER SELECT 2 |

∗: Don't care

Fig. 5-17.

**§5-13. COUT Signal**

The COUT signal is output to count the number of tracks during traverse, etc. It is basically generated by loading the MIRR signal at both edges of the TZC signal. And the used TZC signal can be selected among three different phases for each COUT signal application.

- HPTZC: For 1-track jumps
  Fast phase COUT signal generation with a fast phase TZC signal. (The TZC phase is advanced by a cut-off 1kHz digital HPF; when MCK = 128Fs.)
- STZC: For COUT signal generation when MIRR is externally input and for applications other than COUT generation.
  This is generated from sampling TE at 700kHz. (when MCK = 128Fs)
- DTZC: For high-speed traverse
  Reliable COUT signal generation with a delayed phase STZC signal.

Since it takes some time to generate the MIRR signal, it is necessary to delay the TZC signal in accordance with the MIRR signal delay during high-speed traverse.
The COUT signal output method is switched with D15 and D14 of $3C.
When D15 = 1 : STZC
When D15 = 0 and D14 = 0 : HPTZC
When D15 = 0 and D14 = 1 : DTZC
When the DTZC is selected, the delay can be selected from two values with D14 of $36.

**§5-14. Serial Readout Circuit**

The following measurement and adjustment results can be readout from the SENS pin by inputting the readout clock to the SCLK pin by $39. (See Fig. 5-18, Table 5-19 and "Description of SENS Signals".)

Specified commands
$390C: VC AVRG measurement result
$3908: FE AVRG measurement result
$3904: TE AVRG measurement result
$391F: RF AVRG measurement result
$3953: FCS AGCNTL coefficient result
$3963: TRK AGCNTL coefficient result
$391C: TRVSC adjustment result
$391D: FBIAS register value

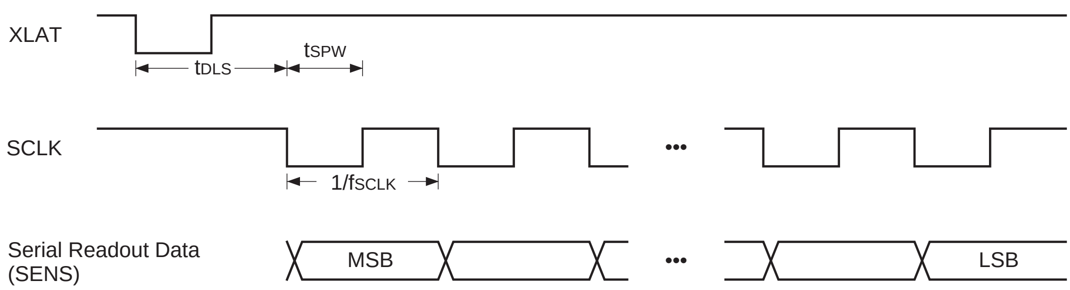



**Fig. 5-18.**

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| SCLK frequency | $f_{SCLK}$ | | | 16 | MHz |
| SCLK pulse width | $t_{SPW}$ | 31.3 | | | ns |
| Delay time | $t_{DLS}$ | 15 | | | µs |

**Table 5-19.**

During readout, the upper 8 bits of the command register must be 39 (Hex).

### §5-15. Writing to Coefficient RAM

The coefficient RAM can be rewritten by $34. All coefficients have default values in the built-in ROM, and transfer from the ROM to the RAM is completed approximately 40µs (when MCK = 128Fs) after the XRST pin rises. (The coefficient RAM cannot be rewritten during this period.)

After that, the characteristics of each built-in filter can be finely adjusted by rewriting the data for each address of the coefficient RAM.

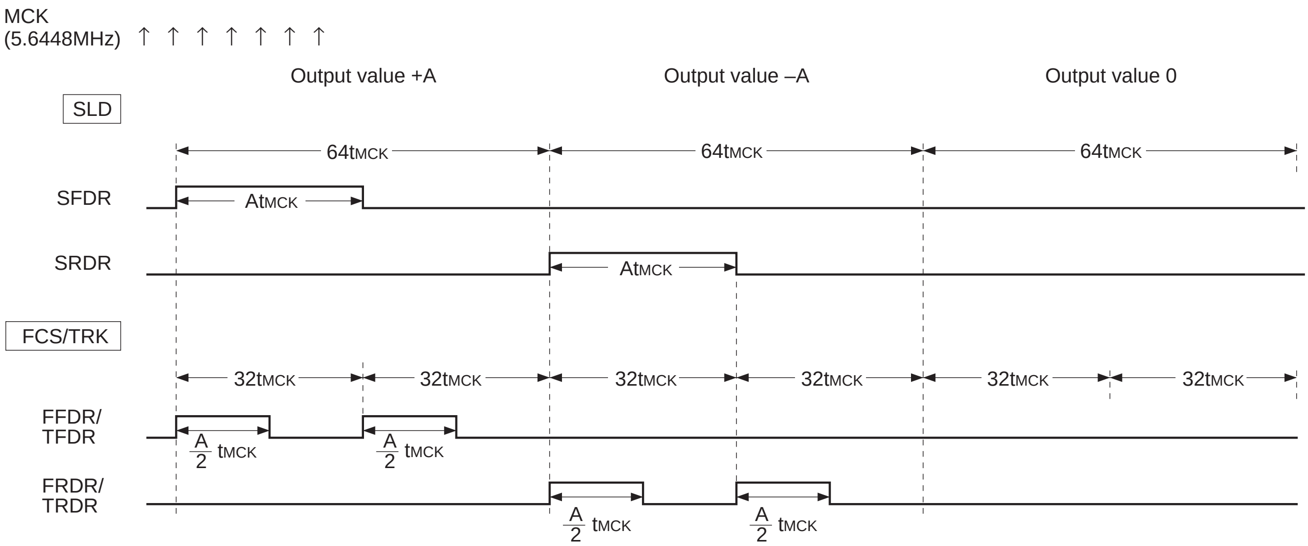
The coefficient rewrite command is comprised of 24 bits, with D14 to D8 of $34 as the address (D15 = 0) and D7 to D0 as data. Coefficient rewriting is completed 11.3µs (when MCK = 128Fs) after the command is received. When rewriting multiple coefficients continuously, be sure to wait 11.3µs (when MCK = 128Fs) before sending the next rewrite command.

### §5-16. PWM Output

FCS, TRK and SLD outputs are output as PWM waveforms.

In particular, FCS and TRK permit accurate drive by using a double oversampling noise shaper.

Timing Chart 5-20 and Fig. 5-21 show examples of output waveforms and drive circuits.




$$t_{MCK} = \frac{1}{5.6448\text{MHz}} \approx 180\text{ns}$$

**Timing Chart 5-20.**

**Example of Driver Circuit**

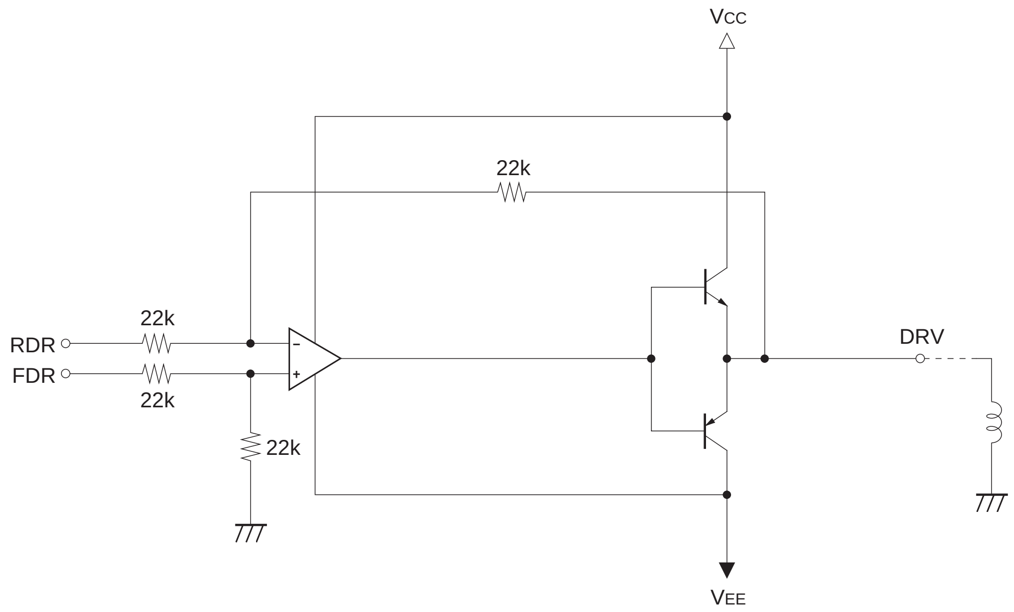



**Fig. 5-21. Driver Circuit**

### §5-17. Servo Status Changes Produced by LOCK Signal

When the LOCK signal becomes low, the TRK servo switches to the gain-up mode and the SLD servo turns off in order to prevent SLD free-running.
Setting D6 (LKSW) of $38 to 1 deactivates this function.
In other words, neither the TRK servo nor the SLD servo change even when the LOCK signal becomes low.
This enables microcomputer control.

### §5-18. Description of Commands and Data Sets

The following description contains portions which convert internal voltages into the values when they are output externally and describe them as input conversion or output conversion.
Input conversion converts these voltages into the voltages entering input pins before A/D conversion.
Output conversion converts PWM output values into analog voltage values.

**$34**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | KA6 | KA5 | KA4 | KA3 | KA2 | KA1 | KA0 | KD7 | KD6 | KD5 | KD4 | KD3 | KD2 | KD1 | KD0 |

When D15 = 0

KA6 to KA0: Coefficient address

KD7 to KD0: Coefficient data

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 0 | FBL9 | FBL8 | FBL7 | FBL6 | FBL5 | FBL4 | FBL3 | FBL2 | FBL1 | — |

When D15 = D14 = D13 = D12 = D11 = 1 ($34F)

D10 = 0

FBIAS LIMIT register write

FBL9 to FBL1: Data; data compared with FB9 to FB1, FBL9 = MSB.
When using the FBIAS register in counter mode, counter operation stops when the value of FB9 to FB1 matches with FBL9 to 1.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 0 | 1 | FB9 | FB8 | FB7 | FB6 | FB5 | FB4 | FB3 | FB2 | FB1 | — |

When D15 = D14 = D13 = D12 = 1 ($34F)

D11 = 0, D10 = 1

FBIAS register write

FB9 to FB1: Data; FB9 is MSB two's complement data.
For FE input conversion, FB9 to FB1 = 011111111 corresponds to 255/256 × $V_{DD}$/5 and FB9 to FB1 = 100000000 to –256/256 × $V_{DD}$/5 respectively. ($V_{DD}$: supply voltage)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 0 | 0 | TV9 | TV8 | TV7 | TV6 | TV5 | TV4 | TV3 | TV2 | TV1 | TV0 |

When D15 = D14 = D13 = D12 = 1 ($34F)

D11 = 0, D10 = 0

TRVSC register write

TV9 to TV0: Data; TV9 is MSB two's complement data.
For TE input conversion, TV9 to TV0 = 0011111111 corresponds to 255/256 × $V_{DD}$/5 and TV9 to TV0 = 1100000000 to –256/256 × $V_{DD}$/5 respectively. ($V_{DD}$: supply voltage)

**Note)**
- When the TRVSC register is readout, the data length is 9 bits. At this time, data corresponding to each bit TV8 to TV0 during external write are readout.
- When reading out internally measured values and then writing these values externally, set TV9 the same as TV8.

**$35 (preset: $35 58 2D)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FT1 | FT0 | FS5 | FS4 | FS3 | FS2 | FS1 | FS0 | FTZ | FG6 | FG5 | FG4 | FG3 | FG2 | FG1 | FG0 |

FT1, FT0, FTZ: Focus search-up speed
Default value: 010 (0.673 × $V_{DD}$ V/s)
Focus drive output conversion

| | FT1 | FT0 | FTZ | Focus search speed [V/s] |
|---|---|---|---|---|
| | 0 | 0 | 0 | 1.35 × $V_{DD}$ |
| ∗ | 0 | 1 | 0 | 0.673 × $V_{DD}$ |
| | 1 | 0 | 0 | 0.449 × $V_{DD}$ |
| | 1 | 1 | 0 | 0.336 × $V_{DD}$ |
| | 0 | 0 | 1 | 1.79 × $V_{DD}$ |
| | 0 | 1 | 1 | 1.08 × $V_{DD}$ |
| | 1 | 0 | 1 | 0.897 × $V_{DD}$ |
| | 1 | 1 | 1 | 0.769 × $V_{DD}$ |

∗: preset, $V_{DD}$: PWM driver supply voltage

FS5 to FS0: Focus search limit voltage
Default value: 011000 (±24/64 × $V_{DD}$, $V_{DD}$: PWM driver supply voltage)
Focus drive output conversion

FG6 to FG0: AGF convergence gain setting value
Default value: 0101101

**$36 (preset: $36 0E 2E)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TDZC | DTZC | TJ5 | TJ4 | TJ3 | TJ2 | TJ1 | TJ0 | SFJP | TG6 | TG5 | TG4 | TG3 | TG2 | TG1 | TG0 |

TDZC: Selects the TZC signal for generating the TRKCNCL signal during brake circuit operation.
TDZC = 0: the edge of the HPTZC or STZC signal, whichever has the faster phase, is used.
TDZC = 1: the edge of the HPTZC or STZC signal or the tracking drive signal zero-cross, whichever has the faster phase, is used. (See §5-12.)

DTZC: DTZC delay (8.5/4.25µs, when MCK = 128Fs)
Default value: 0 (4.25µs)

TJ5 to TJ0: Track jump voltage
Default value: 001110 (≈ ±14/64 × $V_{DD}$, $V_{DD}$: PWM driver supply voltage)
Tracking drive output conversion

SFJP: Surf jump mode on/off
The tracking PWM output is made by adding the tracking filter output and TJReg (TJ5 to TJ0), by setting D7 to 1 (on)

TG6 to TG0: AGT convergence gain setting value
Default value: 0101110

**$37 (preset: $37 50 BA)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FZSH | FZSL | SM5 | SM4 | SM3 | SM2 | SM1 | SM0 | AGS | AGJ | AGGF | AGGT | AGV1 | AGV2 | AGHS | AGHT |

FZSH, FZSL: FZC (Focus Zero Cross) slice level
Default value: 01 (1/8 × $V_{DD}$ × 0.4, $V_{DD}$: supply voltage); FE input conversion

| | FZSH | FZSL | Slice level |
|---|---|---|---|
| | 0 | 0 | 1/4 × $V_{DD}$ × 0.4 |
| ∗ | 0 | 1 | 1/8 × $V_{DD}$ × 0.4 |
| | 1 | 0 | 1/16 × $V_{DD}$ × 0.4 |
| | 1 | 1 | 1/32 × $V_{DD}$ × 0.4 |

∗: preset

SM5 to SM0: Sled move voltage
Default value: 010000 (≈ ±16/64 × $V_{DD}$, $V_{DD}$: PWM driver supply voltage)
Sled drive output conversion

AGS: AGCNTL self-stop on/off
Default value: 1 (on)

AGJ: AGCNTL convergence completion judgment time during low sensitivity adjustment (31/63ms, when MCK = 128Fs)
Default value: 0 (63ms)

AGGF: Focus AGCNTL internally generated sine wave amplitude (small/large)
Default value: 1 (large)

AGGT: Tracking AGCNTL internally generated sine wave amplitude (small/large)
Default value: 1 (large)

| | | FE/TE input conversion |
|---|---|---|
| AGGF | 0 (small) | 1/32 × $V_{DD}$ × 0.4 |
| | 1 (large)∗ | 1/16 × $V_{DD}$ × 0.4 |
| AGGT | 0 (small) | 1/16 × $V_{DD}$ × 0.4 |
| | 1 (large)∗ | 1/8 × $V_{DD}$ × 0.4 |

∗: preset

AGV1: AGCNTL convergence sensitivity during high sensitivity adjustment; high/low
Default value: 1 (high)

AGV2: AGCNTL convergence sensitivity during low sensitivity adjustment; high/low
Default value: 0 (low)

AGHS: AGCNTL high sensitivity adjustment on/off
Default value: 1 (on)

AGHT: AGCNTL high sensitivity adjustment time (128/256ms, when MCK = 128Fs)
Default value: 0 (256ms)

**$38 (preset: $38 00 00)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VCLM | VCLC | FLM | FLC0 | RFLM | RFLC | AGF | AGT | DFSW | LKSW | TBLM | TCLM | FLC1 | TLC2 | TLC1 | TLC0 |

◎ VCLM: VC level measurement (on/off)
VCLC: VC level compensation for FCS In register (on/off)
◎ FLM: Focus zero level measurement (on/off)
FLC0: Focus zero level compensation for FZC register (on/off)
◎ RFLM: RF zero level measurement (on/off)
RFLC: RF zero level compensation (on/off)
AGF: Focus auto gain adjustment (on/off)
AGT: Tracking auto gain adjustment (on/off)
DFSW: Defect disable switch (on/off)
Setting this switch to 1 (on) disables the defect countermeasure circuit.
LKSW: Lock switch (on/off)
Setting this switch to 1 (on) disables the sled free-running prevention circuit.
TBLM: Traverse center measurement (on/off)
◎ TCLM: Tracking zero level measurement (on/off)
FLC1: Focus zero level compensation for FCS In register (on/off)
TLC2: Traverse center compensation (on/off)
TLC1: Tracking zero level compensation (on/off)
TLC0: VC level compensation for TRK/SLD In register (on/off)

**Note)** Commands marked with ◎ are accepted every 2.9ms. (when MCK = 128Fs)
All commands are on when set to 1.

**$39**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| DAC | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 | SD0 |

DAC: Serial data readout DAC mode (on/off)
SD6 to SD0: Serial readout data select

| SD6 | SD5 | SD4 | SD3 to SD0 | Readout data | Readout data length | |
|---|---|---|---|---|---|---|
| 1 | Coefficient RAM data for address = SD5 to SD0 | | | | 8 bits | |
| 0 | 1 | Data RAM data for address = SD4 to SD0 | | | 16 bits | |
| 0 | 0 | SD4 | SD3 to SD0 | | | |
| | | 1 | 1 1 1 1 | RF AVRG register | 8 bits | $399F |
| | | | 1 1 1 0 | RFDC input signal | 8 bits | $399E |
| | | | 1 1 0 1 | FBIAS register | 9 bits | $399D |
| | | | 1 1 0 0 | TRVSC register | 9 bits | $399C |
| | | | 0 0 1 1 | RFDC envelope (bottom) | 8 bits | $3993 |
| | | | 0 0 1 0 | RFDC envelope (peak) | 8 bits | $3992 |
| | | | 0 0 0 1 | RFDC envelope (peak) – (bottom) | 8 bits | $3991 |
| | | 0 | 1 1 * * | VC AVRG register | 9 bits | $398C |
| | | | 1 0 * * | FE AVRG register | 9 bits | $3988 |
| | | | 0 1 * * | TE AVRG register | 9 bits | $3984 |
| | | | 0 0 1 1 | FE input signal | 8 bits | $3983 |
| | | | 0 0 1 0 | TE input signal | 8 bits | $3982 |
| | | | 0 0 0 1 | SE input signal | 8 bits | $3981 |
| | | | 0 0 0 0 | VC input signal | 8 bits | $3980 |

**Note)** Coefficients K40 to K4F cannot be readout. ∗: Don't care
See the description for SRO1 of $3F concerning readout methods for the above data.

**$3A (preset: $3A 00 00)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | FBON | FBSS | FBUP | FBV1 | FBV0 | 0 | TJD0 | FPS1 | FPS0 | TPS1 | TPS0 | 0 | SJHD | INBK | MTI0 |

FBON: FBIAS (focus bias) register addition (on/off)
The FBIAS register value is added to the signal loaded into the FCS In register by FBON = 1 (on).

FBSS: FBIAS (focus bias) register/counter switching
FBSS = 0: register, FBSS = 1: counter.

FBUP: FBIAS (focus bias) counter up/down operation switching
This performs counter up/down control when FBSS = 1. FBUP = 0: down counter,
FBUP = 1: up counter.

FBV1, FBV0: FBIAS (focus bias) counter voltage switching
The number of FCS BIAS count-up/-down steps per cycle is decided by these bits.

| | FBV1 | FBV0 | Number of steps per cycle |
|---|---|---|---|
| * | 0 | 0 | 1 |
| | 0 | 1 | 2 |
| | 1 | 0 | 4 |
| | 1 | 1 | 8 |

*: preset

The counter changes once for each sampling cycle of the focus servo filter. When MCK is 128Fs, the sampling frequency is 88.2kHz. When converted to FE input, 1 step is approximately $1/2^9 \times V_{DD} \times 0.4$, $V_{DD}$ = supply voltage.

TJD0: This sets the tracking servo filter data RAM to 0 when switched from track jump to servo on only when SFJP = 1 (during surf jump operation).

FPS1, FPS0: Gain setting when transferring data from the focus filter to the PWM block.

TPS1, TPS0: Gain setting when transferring data from the tracking filter to the PWM block.
This is effective for increasing the overall gain in order to widen the servo band.
Operation when FPS1, FPS0 (TPS1, TPS0) = 00 is the same as usual (7-bit shift). However, 6dB, 12dB and 18dB can be selected independently for focus and tracking by setting the relative gain to 0dB when FPS1, FPS0 (TPS1, TPS0) = 00.

| | FPS1 | FPS0 | Relative gain |
|---|---|---|---|
| * | 0 | 0 | 0dB |
| | 0 | 1 | +6dB |
| | 1 | 0 | +12dB |
| | 1 | 1 | +18dB |

| TPS1 | TPS0 | Relative gain | |
|---|---|---|---|
| 0 | 0 | 0dB | * |
| 0 | 1 | +6dB | |
| 1 | 0 | +12dB | |
| 1 | 1 | +18dB | |

*: preset

SJHD: This holds the tracking filter output at the value when surf jump starts during surf jump.

INBK: When INBK = 0 (off), the brake circuit masks the tracking drive signal with TRKCNCL which is generated by taking the MIRR signal at the TZC edge. When INBK = 1 (on), the tracking filter input is masked instead of the drive output.

MTI0: The tracking filter input is masked when the MIRR signal is high by setting MTI0 = 1 (on).

**$3B (preset: $3B E0 50)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SFO2 | SFO1 | SDF2 | SDF1 | MAX2 | MAX1 | SFOX | BTF | D2V2 | D2V1 | D1V2 | D1V1 | RINT | 0 | 0 | 0 |

SFOX, SFO2, SFO1: FOK slice level
Default value: 011 (28/256 × $V_{DD}$ × 0.57, $V_{DD}$ = supply voltage)
RFDC input conversion

| | SFOX | SFO2 | SFO1 | Slice level |
|---|---|---|---|---|
| | 0 | 0 | 0 | 16/256 × $V_{DD}$ × 0.57 |
| | 0 | 0 | 1 | 20/256 × $V_{DD}$ × 0.57 |
| | 0 | 1 | 0 | 24/256 × $V_{DD}$ × 0.57 |
| * | 0 | 1 | 1 | 28/256 × $V_{DD}$ × 0.57 |
| | 1 | 0 | 0 | 32/256 × $V_{DD}$ × 0.57 |
| | 1 | 0 | 1 | 40/256 × $V_{DD}$ × 0.57 |
| | 1 | 1 | 0 | 48/256 × $V_{DD}$ × 0.57 |
| | 1 | 1 | 1 | 50/256 × $V_{DD}$ × 0.57 |

*: preset

SDF2, SDF1: DFCT slice level
Default value: 10 (0.0313 × $V_{DD}$ × 1.14V)
RFDC input conversion

| | SDF2 | SDF1 | Slice level |
|---|---|---|---|
| | 0 | 0 | 0.0156 × $V_{DD}$ × 1.14 |
| | 0 | 1 | 0.0234 × $V_{DD}$ × 1.14 |
| * | 1 | 0 | 0.0313 × $V_{DD}$ × 1.14 |
| | 1 | 1 | 0.0391 × $V_{DD}$ × 1.14 |

*: preset, $V_{DD}$: supply voltage

MAX2, MAX1: DFCT maximum time (MCK = 128Fs)
Default value: 00 (no timer limit)

| | MAX2 | MAX1 | DFCT maximum time |
|---|---|---|---|
| * | 0 | 0 | No timer limit |
| | 0 | 1 | 2.00ms |
| | 1 | 0 | 2.36 |
| | 1 | 1 | 2.72 |

*: preset

BTF: Bottom hold double-speed count-up mode for MIRR signal generation
On/off (default: off)
On when set to 1.

D2V2, D2V1: Peak hold 2 for DFCT signal generation
Count-down speed setting
Default value: 01 (0.086 × $V_{DD}$ × 1.14V/ms, 44.1kHz)
[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

| | D2V2 | D2V1 | Count-down speed | |
|---|---|---|---|---|
| | | | [V/ms] | [kHz] |
| | 0 | 0 | 0.0431 × $V_{DD}$ × 1.14 | 22.05 |
| * | 0 | 1 | 0.0861 × $V_{DD}$ × 1.14 | 44.1 |
| | 1 | 0 | 0.172 × $V_{DD}$ × 1.14 | 88.2 |
| | 1 | 1 | 0.344 × $V_{DD}$ × 1.14 | 176.4 |

*: preset, $V_{DD}$: supply voltage

D1V2, D1V1: Peak hold 1 for DFCT signal generation
Count-down speed setting
Default value: 01 (0.688 × $V_{DD}$ × 1.14V/ms, 352.8kHz)
[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

| | D2V2 | D2V1 | Count-down speed | |
|---|---|---|---|---|
| | | | [V/ms] | [kHz] |
| | 0 | 0 | 0.344 × $V_{DD}$ × 1.14 | 176.4 |
| * | 0 | 1 | 0.688 × $V_{DD}$ × 1.14 | 352.8 |
| | 1 | 0 | 1.38 × $V_{DD}$ × 1.14 | 705.6 |
| | 1 | 1 | 2.75 × $V_{DD}$ × 1.14 | 1411.2 |

*: preset, $V_{DD}$: supply voltage

RINT: This initializes the initial-state registers of the circuits which generate MIRR, DFCT and FOK.

**$3C (preset: $3C 00 80)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| COSS | COTS | 0 | 0 | COT2 | COT1 | MOT2 | 0 | BTS1 | BTS0 | MRC1 | MRC0 | 0 | 0 | 0 | 0 |

COSS, COTS: These select the TZC signal used when generating the COUT signal.
Preset = HPTZC.

| | COSS | COTS | TZC |
|---|---|---|---|
| | 1 | — | STZC |
| * | 0 | 0 | HPTZC |
| | 0 | 1 | DTZC |

∗: preset, —: don't care

STZC is the TZC generated by sampling the TE signal at 700kHz. (when MCK = 128Fs)
DTZC is the delayed phase STZC. (The delay amount can be selected by D14 of $36.)
HPTZC is the fast phase TZC passed through a HPF with a cut-off frequency of 1kHz.
See §5-13.

These commands output the TZC signal.
COT2, COT1: This outputs the TZC signal from the COUT pin.

| | COT2 | COT1 | COUT pin output |
|---|---|---|---|
| | 1 | — | STZC |
| | 0 | 1 | HPTZC |
| * | 0 | 0 | COUT |

∗: preset, —: don't care

MOT2: The STZC signal is output from the MIRR pin by setting MOT2 to 1.

These commands set the MIRR signal generation circuit.
BTS1, BTS0: This sets the count-up speed for the bottom hold value of the MIRR generation circuit. The time per step is approximately 708 ns (when MCK = 128Fs). The preset value is BTS1 = 1, BTS0 = 0. However, this is valid only when BTF of $3B is 0.
MRC1, MRC0: This sets the minimum pulse width for masking the MIRR signal of the MIRR generation circuit. As noted in §5-9, the MIRR signal is generated by comparing the waveform obtained by subtracting the bottom hold value from the peak hold value with the MIRR comparator level. Strictly speaking, however, for MIRR to become high, these levels must be compared continuously for a certain time. This sets that time.
The preset value is MRC1 = 0, MRC0 = 0.

| | BTS1 | BTS0 | Number of count-up steps per cycle |
|---|---|---|---|
| | 0 | 0 | 1 |
| | 0 | 1 | 2 |
| * | 1 | 0 | 4 |
| | 1 | 1 | 8 |

| MRC1 | MRC0 | Setting time [µs] |
|---|---|---|
| 0 | 0 | 5.669 ∗ |
| 0 | 1 | 11.338 |
| 1 | 0 | 22.675 |
| 1 | 1 | 45.351 |

∗: preset (when MCK = 128Fs)

**$3D (preset: $3D 00 00)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SFID | SFSK | THID | THSK | 0 | TLD2 | TLD1 | TLD0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SFID: SLED servo filter input can be obtained not from SLD in Reg, but from M0D, which is the TRK filter second-stage output.
When the low-frequency component of the tracking error signal obtained from the RF amplifier is attenuated, the low frequency can be amplified and input to the SLD servo filter.

SFSK: Only during TRK servo gain up2 operation, coefficient K30 is used instead of K00. Normally the DC gain between the TE input pin and M0D changes for TRK filter gain normal and gain up2, and error occurs in the DC level at M0D. In this case, the DC level of the signal transmitted to M00 can be kept uniform by adjusting the K30 value even during the above switching.

THID: TRK hold filter input can be obtained not from SLD in Reg, but from M0D, which is the TRK filter second-stage output.
When signals other than the tracking error signal from the RF amplifier are input to the SE input pin, the signal transmitted from the TE pin can be obtained as TRK hold filter input.

THSK: Only during TRK servo gain up2 operation, coefficient K46 is used instead of K40. Normally the DC gain between the TE input pin and M0D changes for TRK filter gain normal and gain up 2, and error occurs in the DC level at M0D. In this case, the DC level of the signal transmitted to M18 can be kept uniform by adjusting the K46 value even during the above switching.

∗ Please refer to § 5-20. Filter Composition, for further information on SFID, SFSK, THID and THSK commands.

TLD0 to 2: SLD filter correction turns on and off independently of the TRK filter.
Please refer also to $38 (TLC0 to 2) and Figure 5-3.

| | TLC2 | TLD2 | Traverse center correction | |
|---|---|---|---|---|
| | | | TRK filter | SLD filter |
| ∗ | 0 | — | OFF | OFF |
| | 1 | 0 | ON | ON |
| | | 1 | ON | OFF |

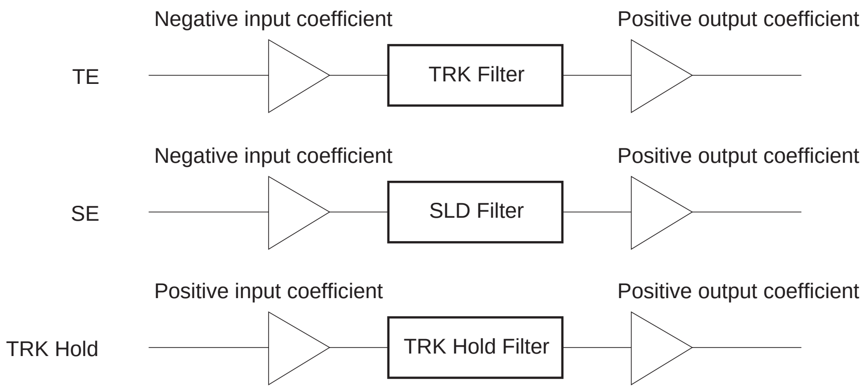
| | TLC1 | TLD1 | Tracking zero level correction | |
|---|---|---|---|---|
| | | | TRK filter | SLD filter |
| ∗ | 0 | — | OFF | OFF |
| | 1 | 0 | ON | ON |
| | | 1 | ON | OFF |

| | TLC0 | TLD0 | VC level correction | |
|---|---|---|---|---|
| | | | TRK filter | SLD filter |
| ∗ | 0 | — | OFF | OFF |
| | 1 | 0 | ON | ON |
| | | 1 | ON | OFF |

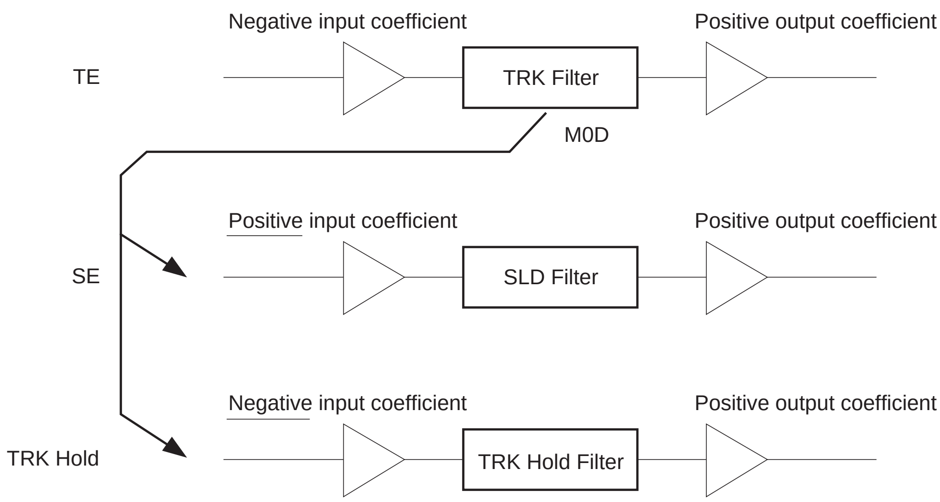
∗: preset, — : Don't care

• Input coefficient inversion when SFID = 1 and THID = 1

The preset coefficients for the TRK filter are negative for input and positive for output. With this, the CXD2597Q outputs the servo drives which have the reversed phase to the error inputs.




When SFID = 1, the TRK filter negative input coefficient is applied to the SLD filter, so invert the SLD input coefficient (K00) code.
For the same reason, when THID = 1, invert the TRK hold input coefficient (K40) code.




Please refer also to § 5-20. Filter Composition.

**$3E (preset: $3E 00 00)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| F1NM | F1DM | F3NM | F3DM | T1NM | T1UM | T3NM | T3UM | DFIS | TLCD | 0 | LKIN | COIN | MDFI | MIRI | XT1D |

F1NM, F1DM: Quasi double accuracy setting for FCS servo filter first-stage
On when set to 1; default = 0.
F1NM: Gain normal
F1DM: Gain down

T1NM, T1UM: Quasi double accuracy setting for TRK servo filter first-stage
On when set to 1; default = 0.
T1NM: Gain normal
T1UM: Gain up

F3NM, F3DM: Quasi double accuracy setting for FCS servo filter third-stage
On when set to 1; default = 0.
Generally, the advance amount of the phase becomes large by partially setting the FCS servo third-stage filter which is used as the phase compensation filter to double accuracy.
F3NM: Gain normal
F3DM: Gain down

T3NM, T3UM: Quasi double accuracy setting for TRK servo filter third-stage
On when set to 1; default = 0.
Generally, the advance amount of the phase becomes large by partially setting the TRK servo third-stage filter which is used as the phase compensation filter to double accuracy.
T3NM: Gain normal
T3UM: Gain up

**Note)** Filter first- and third-stage quasi double accuracy settings can be set individually.
See "Filter Composition" at the end of this specification concerning quasi double accuracy.

DFIS: FCS hold filter input extraction node selection
0: M05 (Data RAM address 05); default
1: M04 (Data RAM address 04)

TLCD: This command masks the TLC2 command set by D2 of $38 only when FOK is low.
On when set to 1; default = 0

LKIN: When 0, the internally generated LOCK signal is output to the LOCK pin. (default)
When 1, the LOCK signal can be input from an external source to the LOCK pin.

COIN: When 0, the internally generated COUT signal is output to the COUT pin. (default)
When 1, the COUT signal can be input from an external source to the COUT pin.
The MIRR, DFCT and FOK signals can also be input from an external source.

MDFI: When 0, the MIRR, DFCT and FOK signals are generated internally. (default)
When 1, the MIRR, DFCT and FOK signals can be input from an external source through the MIRR, DFCT and FOK pins.

MIRI: When 0, the MIRR signal is generated internally. (default)
When 1, the MIRR signal can be input from an external source through the MIRR pin.

| | MDFI | MIRI | |
|---|---|---|---|
| * | 0 | 0 | MIRR, DFCT and FOK are all generated internally. |
| | 0 | 1 | MIRR only is input from an external source. |
| | 1 | — | MIRR, DFCT and FOK are all input from an external source. |

*: preset, —: don't care

XT1D: The clock input from FSTI can be used without being frequency-divided as the master clock for the servo block by setting D0 to 1. This command takes precedence over the XTSL pin, XT2D and XT4D. See the description of $3F for XT2D and XT4D.

**$3F (preset: $3F 00 00)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | AGG4 | XT4D | XT2D | 0 | DRR2 | DRR1 | DRR0 | 0 | ASFG | FTQ | LPAS | SRO1 | 0 | AGHF | ASOT |

AGG4: This varies the amplitude of the internally generated sine wave using the AGGF and AGGT commands during AGC.
When AGG4 = 0, the default is used. When AGG4 = 1, the setting is as shown in the table below.

| | AGGF (MSB) | AGGT (LSB) | TE/FE input conversion |
|---|---|---|---|
| * | 0 | 0 | 1/64 × VDD × 0.4 [V] |
| | 0 | 1 | 1/32 × VDD × 0.4 |
| | 1 | 0 | 1/16 × VDD × 0.4 |
| | 1 | 1 | 1/8 × VDD × 0.4 |

∗: preset

These settings are the same for both focus auto gain control and tracking auto gain control.

XT4D, XT2D: MCK (digital servo master clock) frequency division setting
This command forcibly sets the frequency division ratio to 1/4, 1/2 or 1/1 when MCK is generated from the signal input to the FSTI pin. See the description of $3E for XT1D.

| | XT1D | XT2D | XT4D | Frequency division ratio |
|---|---|---|---|---|
| * | 0 | 0 | 0 | According to XTSL |
| | 1 | — | — | 1/1 |
| | 0 | 1 | — | 1/2 |
| | 0 | 0 | 1 | 1/4 |

∗: preset, —: don't care

DRR2 to DRR0: Partially clears the Data RAM values (0 write).
The following values are cleared when set to 1 (on) respectively; default = 0
DRR2: M08, M09, M0A
DRR1: M00, M01, M02
DRR0: M00, M01, M02 only when LOCK = low
**Note)** Set DRR1 and DRR0 on for 50µs or more.

ASFG: When vibration detection is performed during anti-shock circuit operation, FCS servo filter is forcibly set to gain normal status.
On when set to 1; default = 0

LPAS: Built-in analog buffer low-current consumption mode
This mode reduces the total analog buffer current consumption for the VC, TE, SE and FE input analog buffers by using a single operational amplifier.
On when set to 1; default = 0
**Note)** When using this mode, first check whether each error signal is properly A/D converted using the SRO1 and SRO0 commands of $3F.

SRO1: These commands are used to output various data externally continuously which have been specified with the $39 command. (However, D15 (DAC) of $39 must be set to 1.)
Digital output (SOCK, XOLT and SOUT) can be obtained from three specified pins by setting these commands to 1 respectively. The default is 0, 0. (no readout)

The output pins for each case are shown below.

| | SRO1 = 1 |
|---|---|
| SOCK | LMUT pin |
| XOLT | WFCK pin |
| SOUT | RMUT pin |

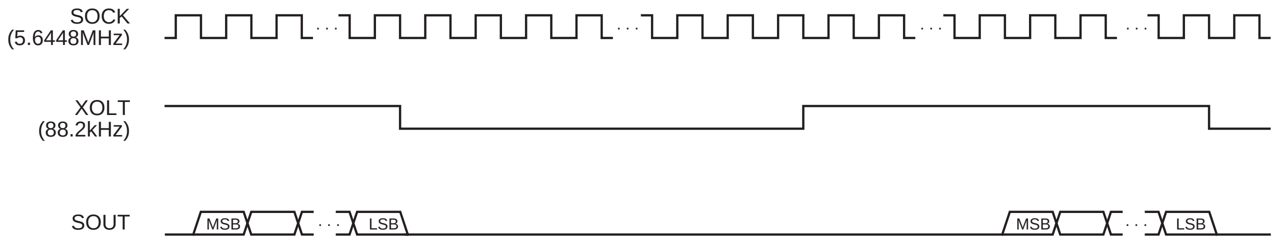
(See "Description of Data Readout" on the following page.)

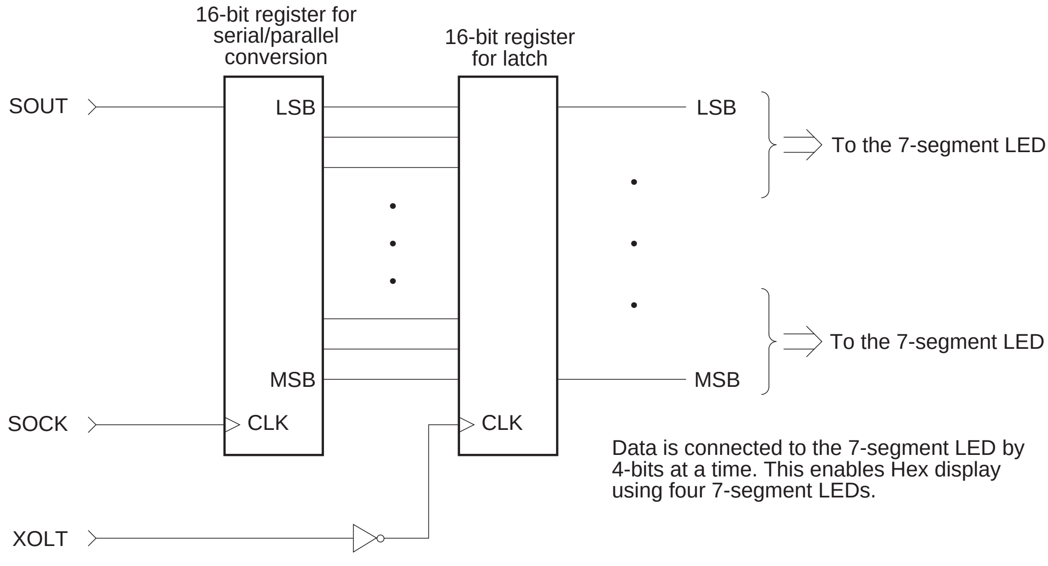
AGHF: This halves the frequency of the internally generated sine wave during AGC.

FTQ: The slope of the output during focus search is a quarter of the conventional output slope. ON when set to 1, default = 0.

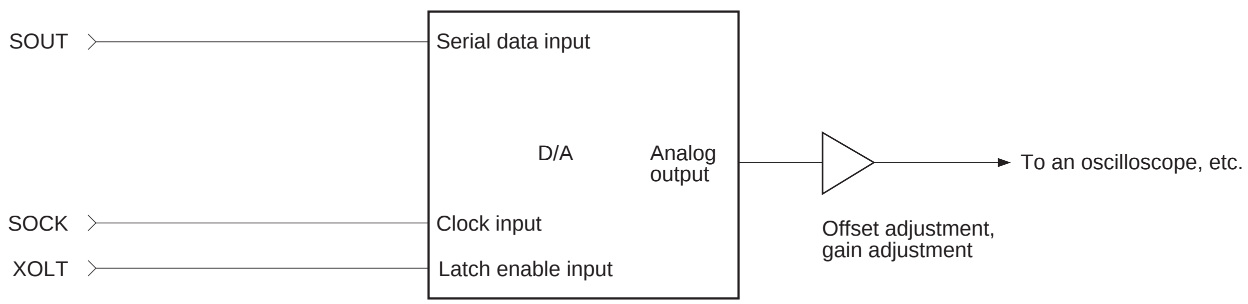
ASOT: The anti-shock signal, which is internally detected, is output from the ATSK pin. Output when set to 1; default = 0.
Vibration detection when a high signal is output for the anti-shock signal output.

## Description of Data Readout




Data is connected to the 7-segment LED by 4-bits at a time. This enables Hex display using four 7-segment LEDs.




Waveforms can be monitored with an oscilloscope using a serial input-type D/A converter as shown above.

## §5-19. List of Servo Filter Coefficients

### <Coefficient Preset Value Table (1)>

| ADDRESS | DATA | CONTENTS |
|---|---|---|
| K00 | E0 | SLED INPUT GAIN |
| K01 | 81 | SLED LOW BOOST FILTER A-H |
| K02 | 23 | SLED LOW BOOST FILTER A-L |
| K03 | 7F | SLED LOW BOOST FILTER B-H |
| K04 | 6A | SLED LOW BOOST FILTER B-L |
| K05 | 10 | SLED OUTPUT GAIN |
| K06 | 14 | FOCUS INPUT GAIN |
| K07 | 30 | SLED AUTO GAIN |
| K08 | 7F | FOCUS HIGH CUT FILTER A |
| K09 | 46 | FOCUS HIGH CUT FILTER B |
| K0A | 81 | FOCUS LOW BOOST FILTER A-H |
| K0B | 1C | FOCUS LOW BOOST FILTER A-L |
| K0C | 7F | FOCUS LOW BOOST FILTER B-H |
| K0D | 58 | FOCUS LOW BOOST FILTER B-L |
| K0E | 82 | FOCUS PHASE COMPENSATE FILTER A |
| K0F | 7F | FOCUS DEFECT HOLD GAIN |
| K10 | 4E | FOCUS PHASE COMPENSATE FILTER B |
| K11 | 32 | FOCUS OUTPUT GAIN |
| K12 | 20 | ANTI SHOCK INPUT GAIN |
| K13 | 30 | FOCUS AUTO GAIN |
| K14 | 80 | HPTZC / Auto Gain HIGH PASS FILTER A |
| K15 | 77 | HPTZC / Auto Gain HIGH PASS FILTER B |
| K16 | 80 | ANTI SHOCK HIGH PASS FILTER A |
| K17 | 77 | HPTZC / Auto Gain LOW PASS FILTER B |
| K18 | 00 | Fix* |
| K19 | F1 | TRACKING INPUT GAIN |
| K1A | 7F | TRACKING HIGH CUT FILTER A |
| K1B | 3B | TRACKING HIGH CUT FILTER B |
| K1C | 81 | TRACKING LOW BOOST FILTER A-H |
| K1D | 44 | TRACKING LOW BOOST FILTER A-L |
| K1E | 7F | TRACKING LOW BOOST FILTER B-H |
| K1F | 5E | TRACKING LOW BOOST FILTER B-L |
| K20 | 82 | TRACKING PHASE COMPENSATE FILTER A |
| K21 | 44 | TRACKING PHASE COMPENSATE FILTER B |
| K22 | 18 | TRACKING OUTPUT GAIN |
| K23 | 30 | TRACKING AUTO GAIN |
| K24 | 7F | FOCUS GAIN DOWN HIGH CUT FILTER A |
| K25 | 46 | FOCUS GAIN DOWN HIGH CUT FILTER B |
| K26 | 81 | FOCUS GAIN DOWN LOW BOOST FILTER A-H |
| K27 | 3A | FOCUS GAIN DOWN LOW BOOST FILTER A-L |
| K28 | 7F | FOCUS GAIN DOWN LOW BOOST FILTER B-H |
| K29 | 66 | FOCUS GAIN DOWN LOW BOOST FILTER B-L |
| K2A | 82 | FOCUS GAIN DOWN PHASE COMPENSATE FILTER A |
| K2B | 44 | FOCUS GAIN DOWN DEFECT HOLD GAIN |
| K2C | 4E | FOCUS GAIN DOWN PHASE COMPENSATE FILTER B |
| K2D | 1B | FOCUS GAIN DOWN OUTPUT GAIN |
| K2E | 00 | NOT USED |
| K2F | 00 | NOT USED |

* Fix indicates that normal preset values.

**<Coefficient Preset Value Table (2)>**

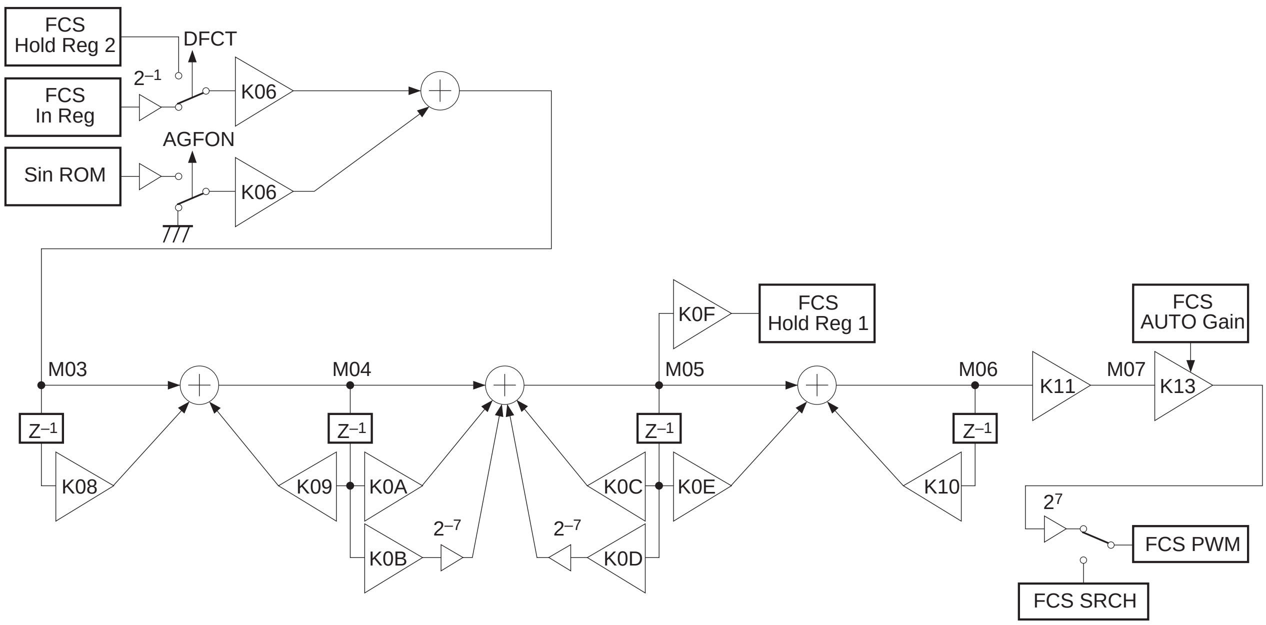
| ADDRESS | DATA | CONTENTS |
|---|---|---|
| K30 | 80 | SLED INPUT GAIN (Only when TRK Gain Up2 is accessed with SFSK = 1.) |
| K31 | 66 | ANTI SHOCK LOW PASS FILTER B |
| K32 | 00 | NOT USED |
| K33 | 7F | ANTI SHOCK HIGH PASS FILTER B-H |
| K34 | 6E | ANTI SHOCK HIGH PASS FILTER B-L |
| K35 | 20 | ANTI SHOCK FILTER COMPARATE GAIN |
| K36 | 7F | TRACKING GAIN UP2 HIGH CUT FILTER A |
| K37 | 3B | TRACKING GAIN UP2 HIGH CUT FILTER B |
| K38 | 80 | TRACKING GAIN UP2 LOW BOOST FILTER A-H |
| K39 | 44 | TRACKING GAIN UP2 LOW BOOST FILTER A-L |
| K3A | 7F | TRACKING GAIN UP2 LOW BOOST FILTER B-H |
| K3B | 77 | TRACKING GAIN UP2 LOW BOOST FILTER B-L |
| K3C | 86 | TRACKING GAIN UP PHASE COMPENSATE FILTER A |
| K3D | 0D | TRACKING GAIN UP PHASE COMPENSATE FILTER B |
| K3E | 57 | TRACKING GAIN UP OUTPUT GAIN |
| K3F | 00 | NOT USED |
| K40 | 04 | TRACKING HOLD FILTER INPUT GAIN |
| K41 | 7F | TRACKING HOLD FILTER A-H |
| K42 | 7F | TRACKING HOLD FILTER A-L |
| K43 | 79 | TRACKING HOLD FILTER B-H |
| K44 | 17 | TRACKING HOLD FILTER B-L |
| K45 | 6D | TRACKING HOLD FILTER OUTPUT GAIN |
| K46 | 00 | TRACKING HOLD FILTER INPUT GAIN (Only when TRK Gain Up2 is accessed with THSK = 1.) |
| K47 | 00 | NOT USED |
| K48 | 02 | FOCUS HOLD FILTER INPUT GAIN |
| K49 | 7F | FOCUS HOLD FILTER A-H |
| K4A | 7F | FOCUS HOLD FILTER A-L |
| K4B | 79 | FOCUS HOLD FILTER B-H |
| K4C | 17 | FOCUS HOLD FILTER B-L |
| K4D | 54 | FOCUS HOLD FILTER OUTPUT GAIN |
| K4E | 00 | NOT USED |
| K4F | 00 | NOT USED |

## §5-20. Filter Composition

The internal filter composition is shown below.

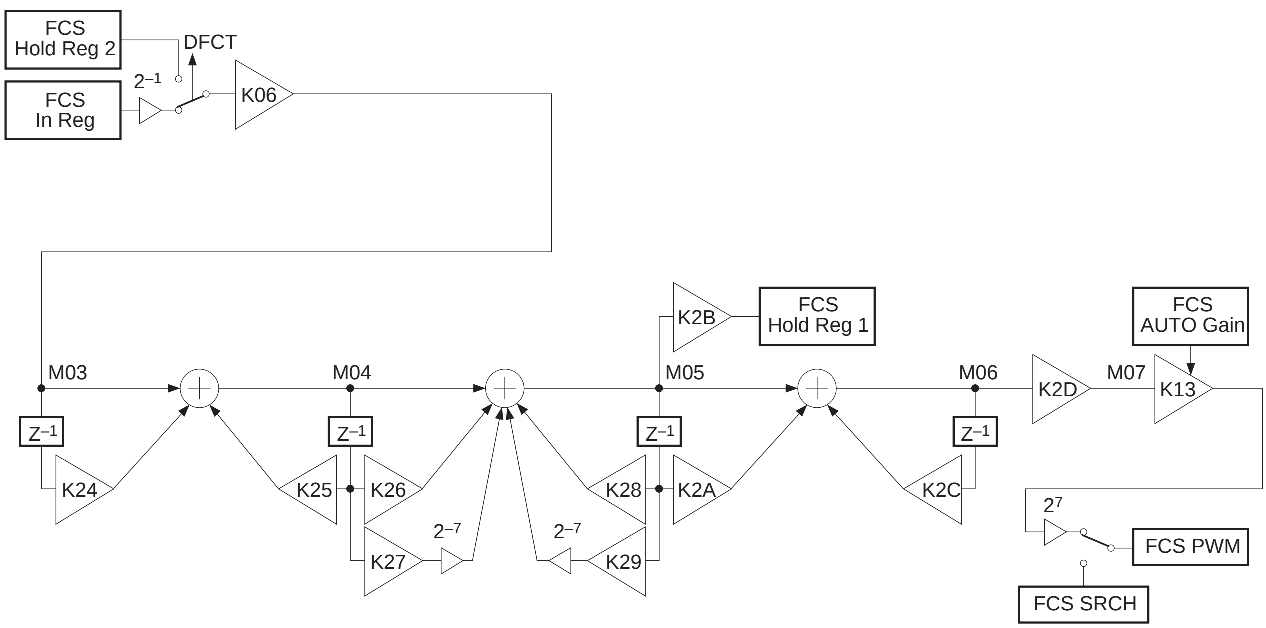
K∗∗ and M∗∗ indicate coefficient RAM and Data RAM address values respectively.

### FCS Servo Gain Normal fs = 88.2kHz



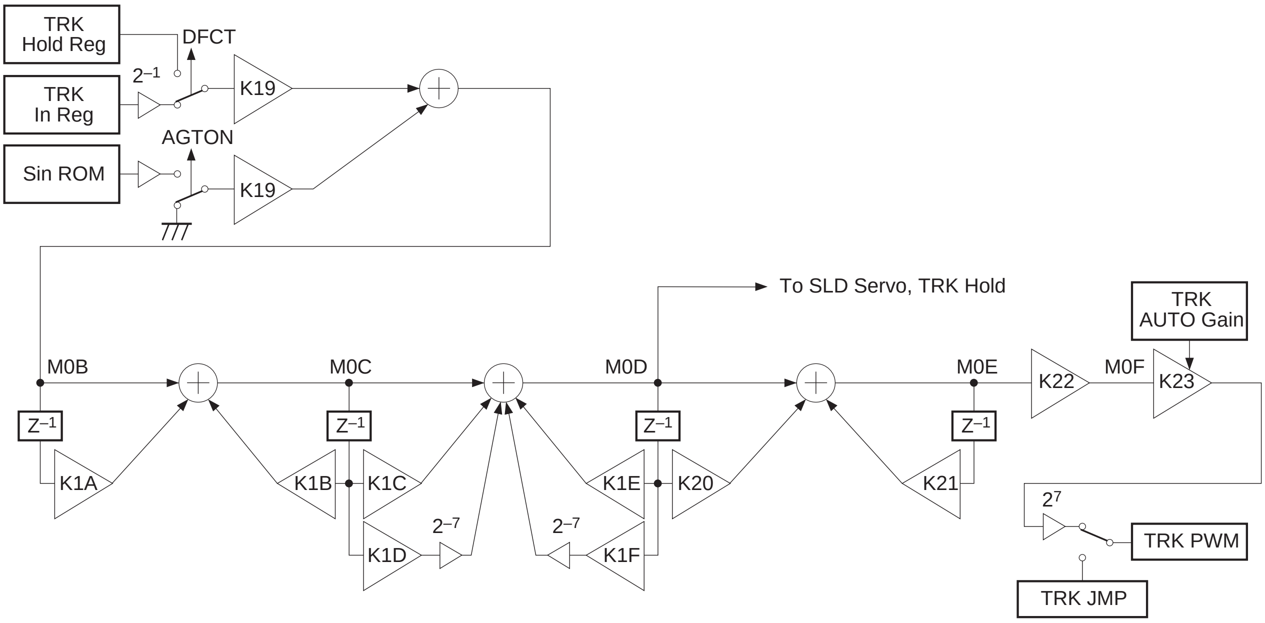

Note) Set the MSB bit of the K0B and K0D coefficients to 0.

### FCS Servo Gain Down fs = 88.2kHz



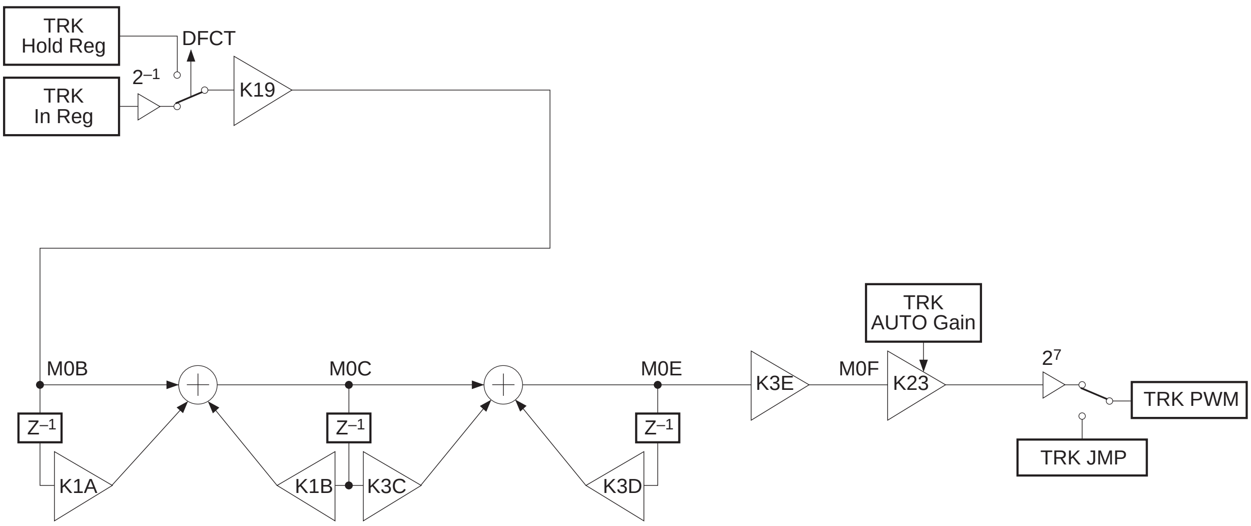

Note) Set the MSB bit of the K27 and K29 coefficients to 0.

**TRK Servo Gain Normal fs = 88.2kHz**

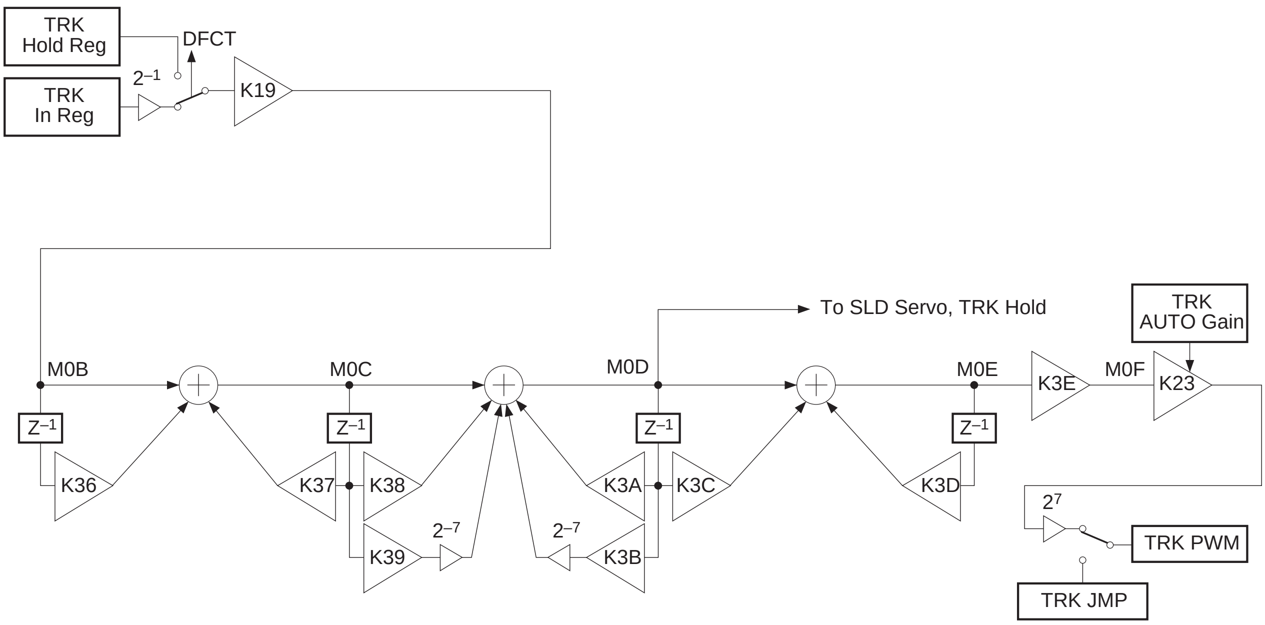



Note) Set the MSB bit of the K1D and K1F coefficients to 0.

**TRK Servo Gain Up 1 fs = 88.2kHz**

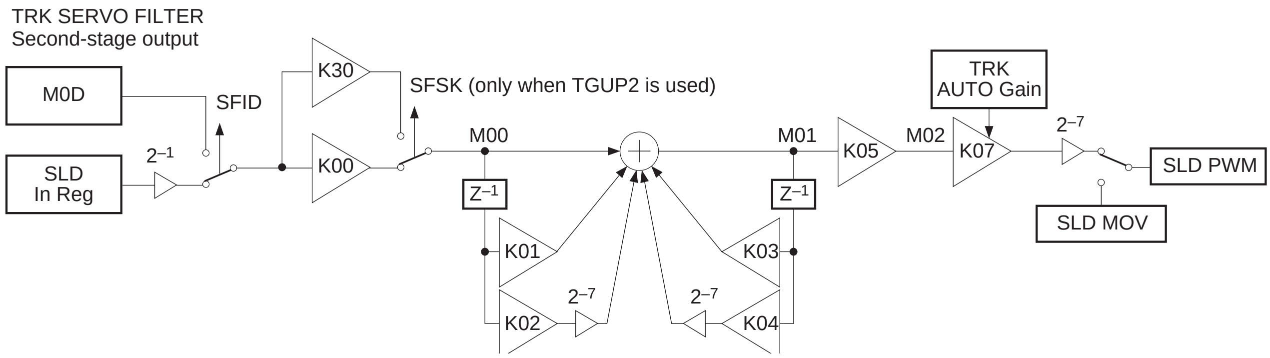


### TRK Servo Gain Up 2   fs = 88.2kHz



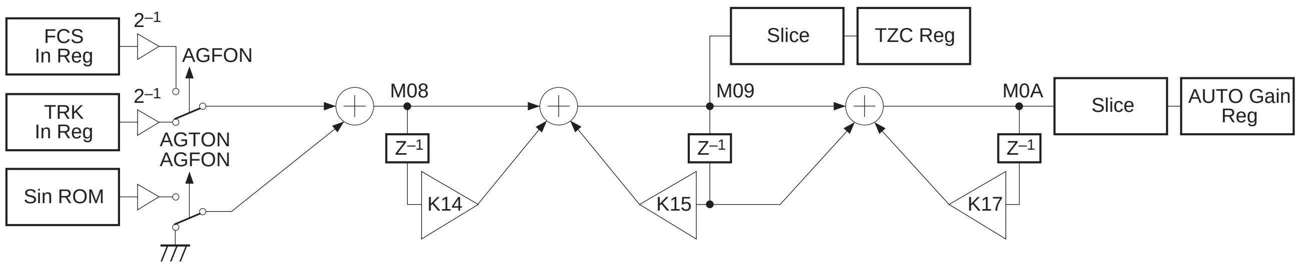

Note) Set the MSB bit of the K39 and K3B coefficients to 0.

### SLD Servo   fs = 345Hz

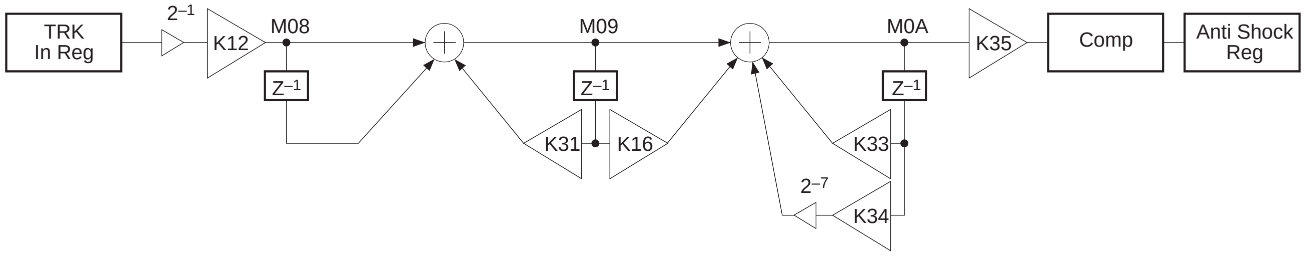



Note) Set the MSB bit of the K02 and K04 coefficients to 0.

### HPTZC/Auto Gain   fs = 88.2kHz

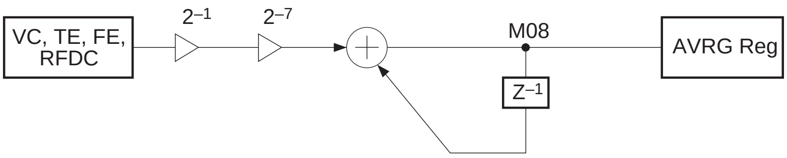


**Anti Shock fs = 88.2kHz**

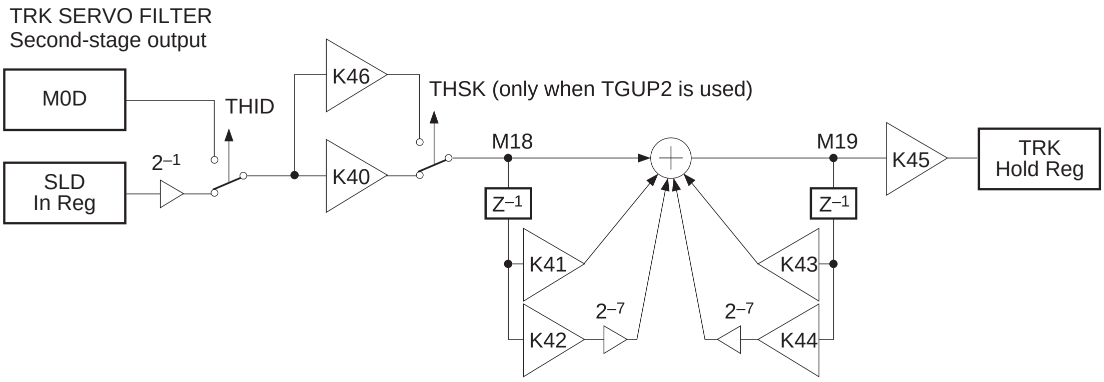



Note) Set the MSB bit of the K34 coefficient to 0.
The comparator input is 1/16 the maximum amplitude of the comparator input.

**AVRG fs = 88.2kHz**

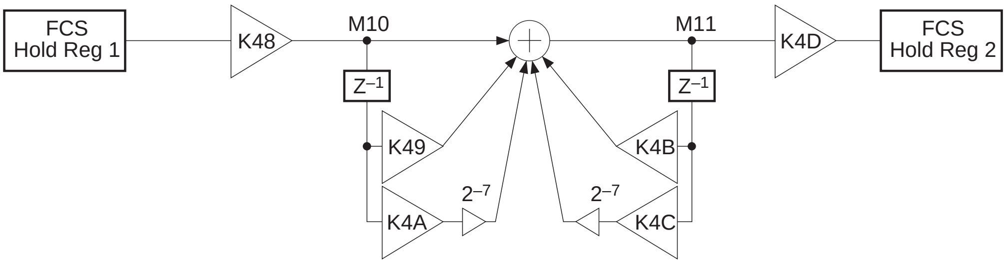



**TRK Hold fs = 345Hz**



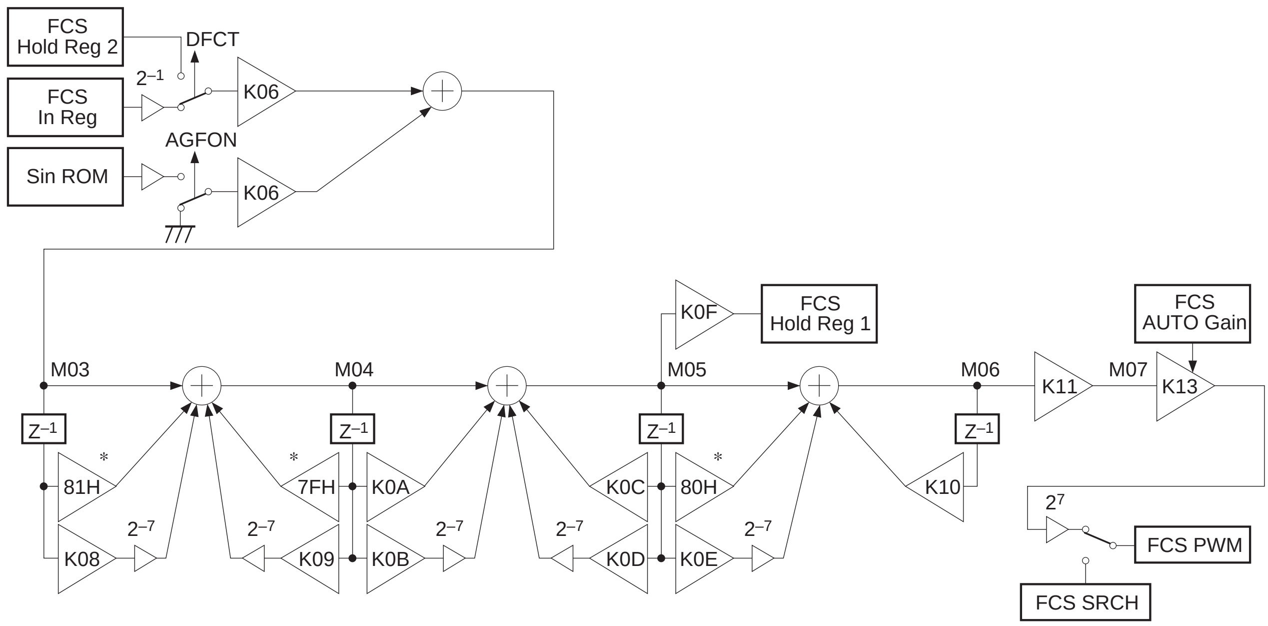

Note) Set the MSB bit of the K42 and K44 coefficients to 0.

**FCS Hold fs = 345Hz**




Note) Set the MSB bit of the K4A and K4C coefficients to 0.

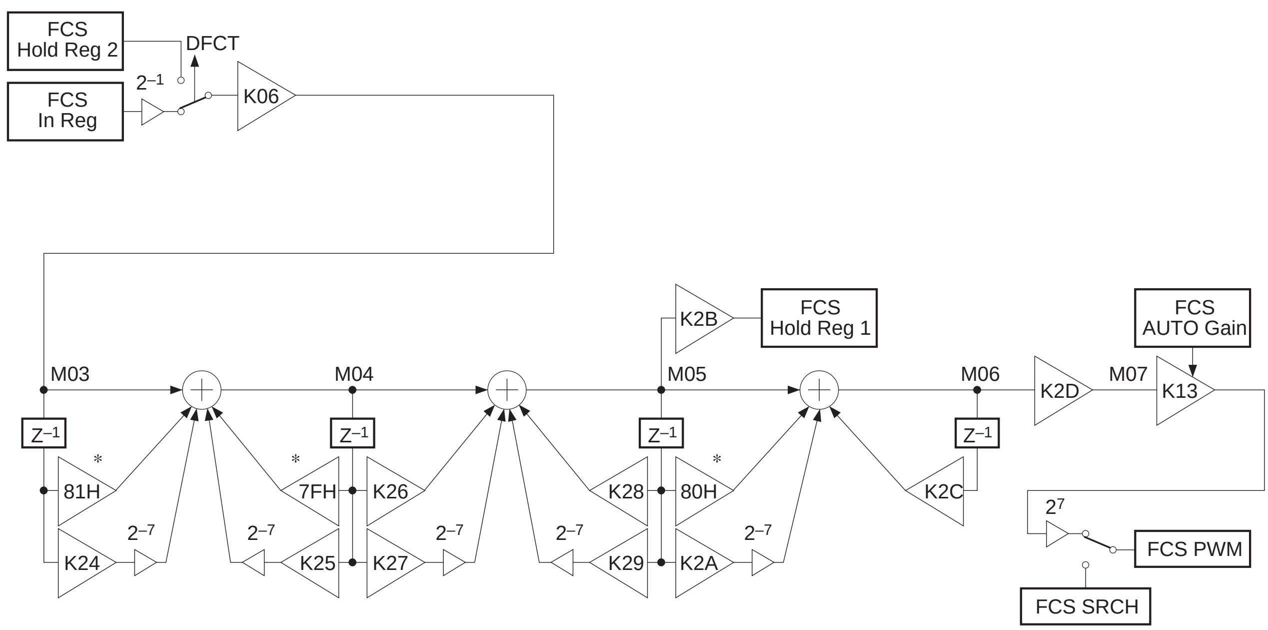
## FCS Servo Gain Normal; Fs = 88.2kHz, during quasi double accuracy (Ex.: $3EAXX0)




* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K0B and K0D coefficients during normal operation, and of the K08, K09 and K0E coefficients during quasi double accuracy to 0.

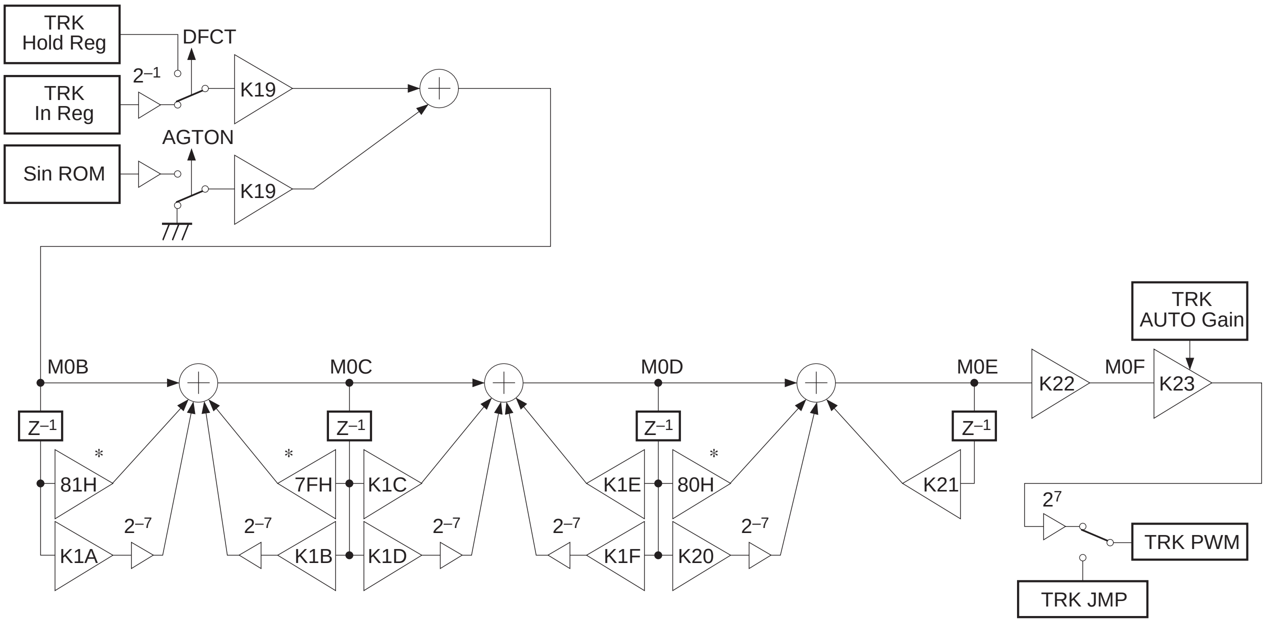
## FCS Servo Gain Down; Fs = 88.2kHz, during quasi double accuracy (Ex.: $3E5XX0)




* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K27 and K29 coefficients during normal operation, and of the K24, K25 and K2A coefficients during quasi double accuracy to 0.

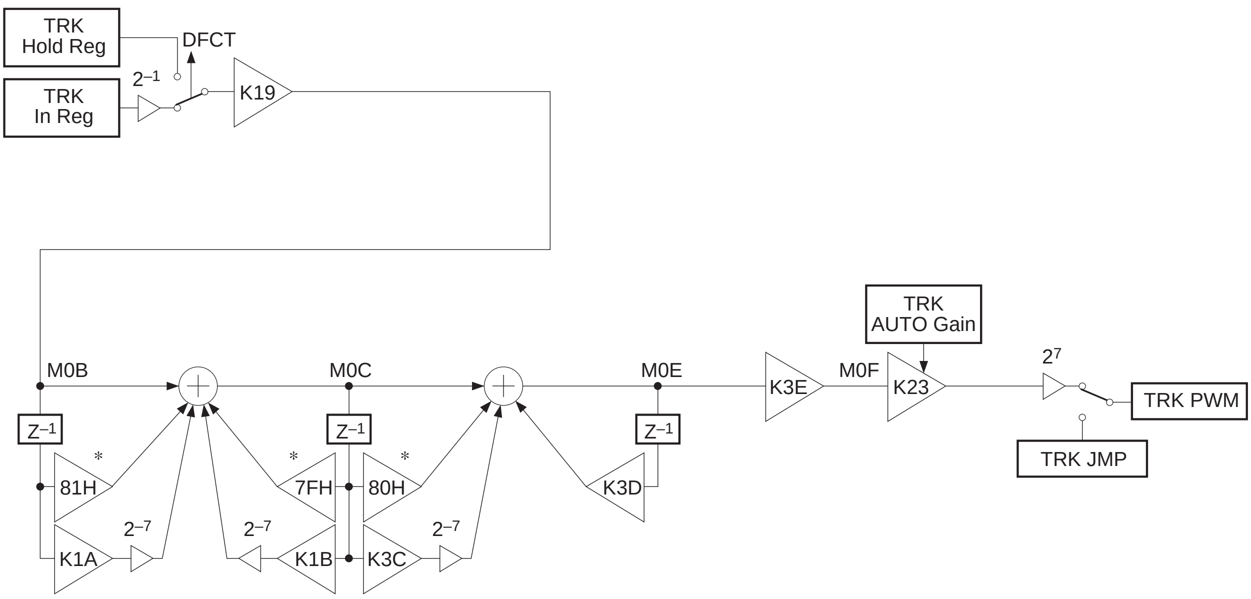
**TRK Servo Gain Normal; Fs = 88.2kHz, during quasi double accuracy (Ex.: $3EXAX0)**




* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K1D and K1F coefficients during normal operation, and of the K1A, K1B and K20 coefficients during quasi double accuracy to 0.

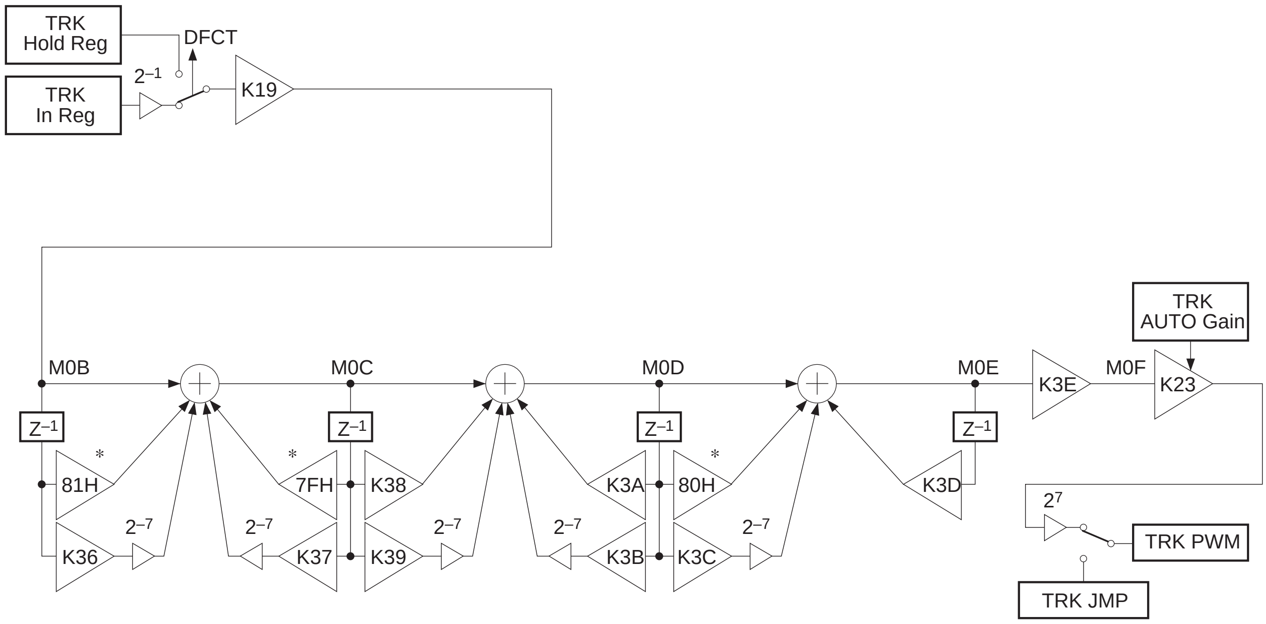
**TRK Servo Gain Up 1; Fs = 88.2kHz, during quasi double accuracy (Ex.: $3EX5X0)**




* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K1A, K1B and K3C coefficients during quasi double accuracy to 0.

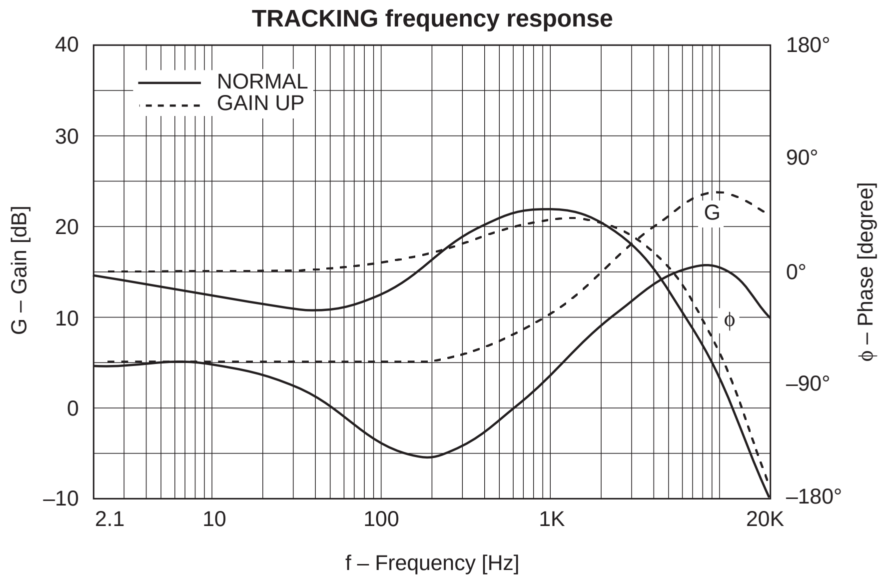
**TRK Servo Gain Up 2; Fs = 88.2kHz, during quasi double accuracy (Ex.: $3EX5X0)**

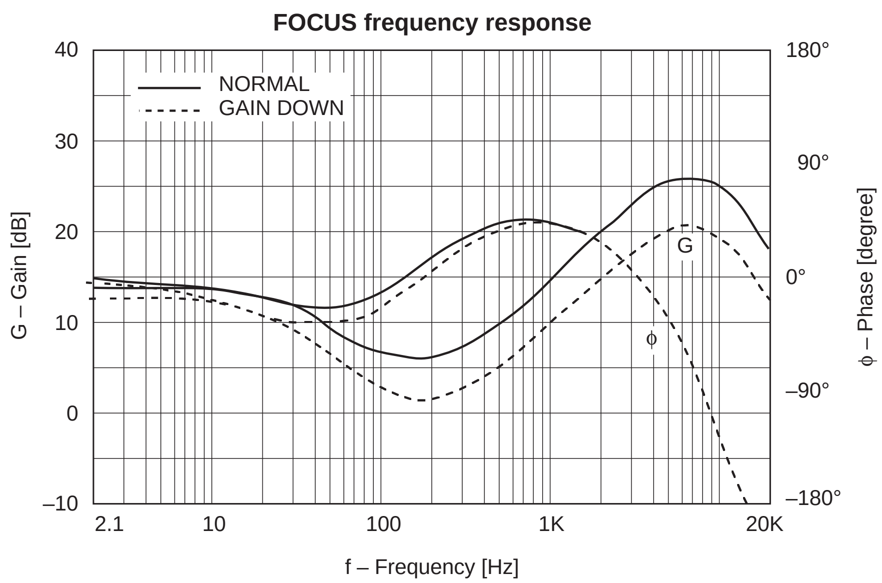



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

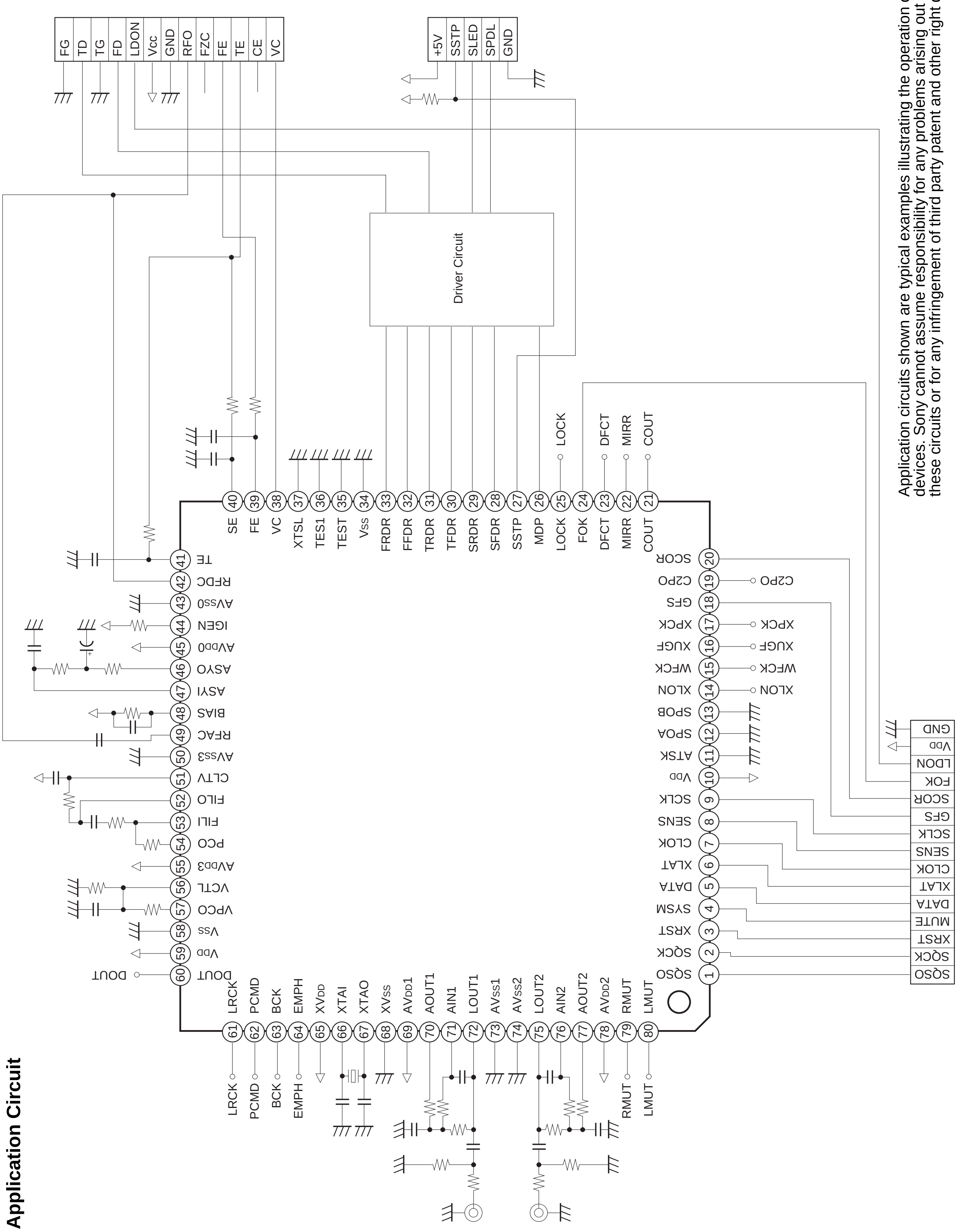
Note) Set the MSB bit of the K39 and K3B coefficients during normal operation, and of the K36, K37 and K3C coefficients during quasi double accuracy to 0.

## §5-21. TRACKING and FOCUS Frequency Response



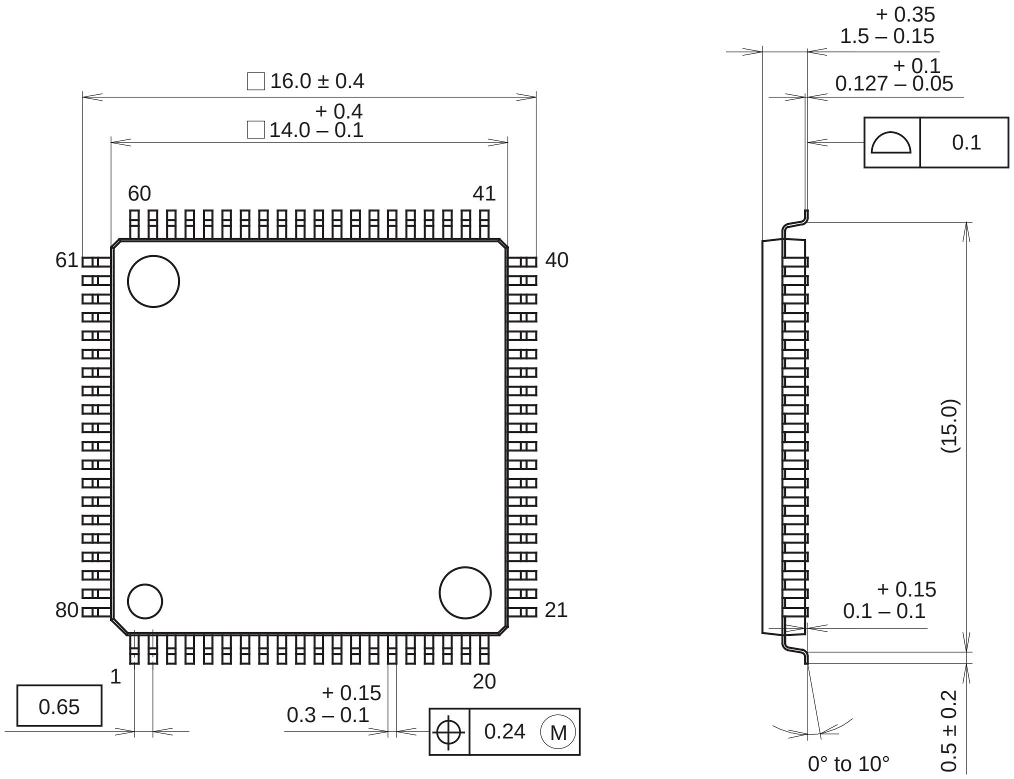
## S6. Application Circuit




Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

**Package Outline** Unit: mm

80PIN QFP (PLASTIC)




| | |
|---|---|
| SONY CODE | QFP-80P-L03 |
| EIAJ CODE | QFP080-P-1414 |
| JEDEC CODE | ———— |

PACKAGE STRUCTURE

| | |
|---|---|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER PLATING |
| LEAD MATERIAL | 42/COPPER ALLOY |
| PACKAGE MASS | 0.6g |