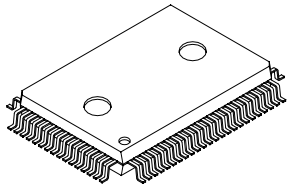
SONY

CXA2108AQ

Constant-Current Driver for Full Color LED Display

80 pin QFP (Plastic)



Description

The CXA2108AQ is a 1,024-gradation LED driver which is ideal for full color LED displays. This IC has 24 outputs and a maximum output current of 70mA. Time division allows driving of either two or six LEDs per output by connecting an external FET or other switch. The luminance (PWM) and drive current for each LED are set using the internal RAM. The LED type is common anode.

Features

- 24 outputs: 10-bit (1,024-gradation) PWM current outputs
- Maximum output current: 70mA
- LED type: Common anode
- 4-bit brightness function capable of switching the basic PWM pulse width in 16 steps
- Time division allows driving of up to six LEDs with a single output, making it possible to configure a high definition display with few driver ICs.
- Coarse Adj. (2 bits) and Fine Adj. (8 bits) output current adjustment for each LED makes it possible to drive R, G and B using the same output from the same IC. In addition, the characteristics variance of each LED can also be corrected.
- All luminance (PWM) data and drive current data are set by writing to the internal RAM.
- PWM emitting can be performed up to 15 times per frame to realize a screen with little flicker.
- Two built-in PWM data RAM make it possible to set the next luminance data even during PWM operation.
- Abnormal internal temperature detection circuit
- Single 5V power supply
- Current output with protection diode (diode cathode voltage: VPD can be supplied independently of the 5V power supply.)
- Surface mounting package (80-pin QFP)

Applications

LED display panels

Structure

Bi-CMOS silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV_{CC}, DV_{CC}	–0.3 to +6.0	V
	VPD	–0.3 to +10.5	V
• Digital input voltage	V_{I}_D	–0.3 to DV_{CC} + 0.3	V
• Digital output current	Io_D	–5.0 to +5.0	mA
• Driver output voltage	V_DVR	0 to VPD + 0.3	V
• Driver output current	I_DVR	–1 to +80	mA
• Operating temperature*1	Topr	–40 to +80	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation*1 (Ta = 65°C or less)	P_D	1.5	W

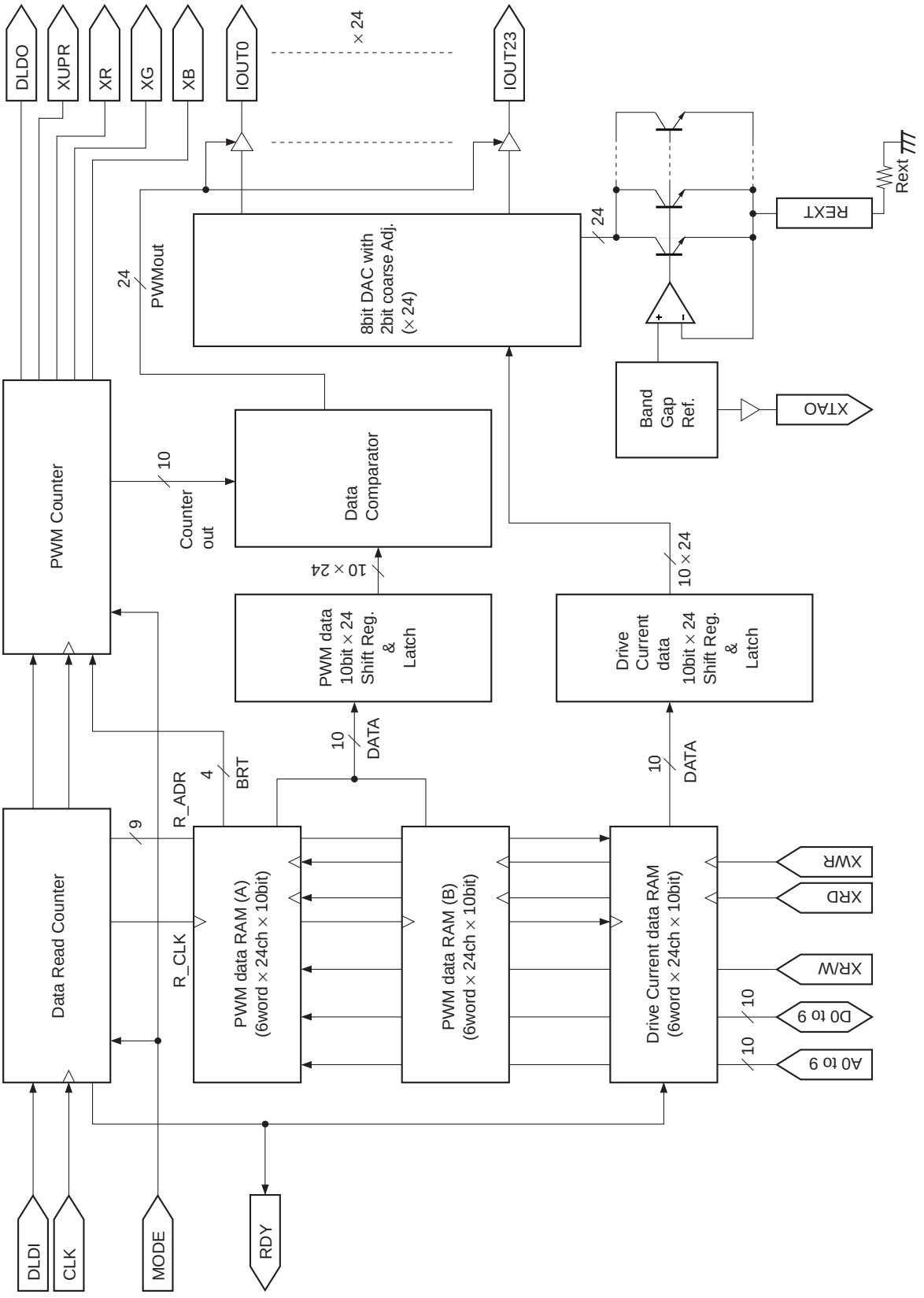
Recommended Operating Range

• Supply voltage	AV_{CC}, DV_{CC}	4.75 to 5.25	V
	VPD	AV_{CC} to 10	V
• Driver output compliance voltage	Vcmp	1.0 to VPD + 0.3 (I_DVR = 0 to 70mA)	V
• Operating temperature (ambient temperature)*1	Ta	–20 to +65	°C
• Operating temperature (case temperature)*1	Tc	–20 to +110	°C

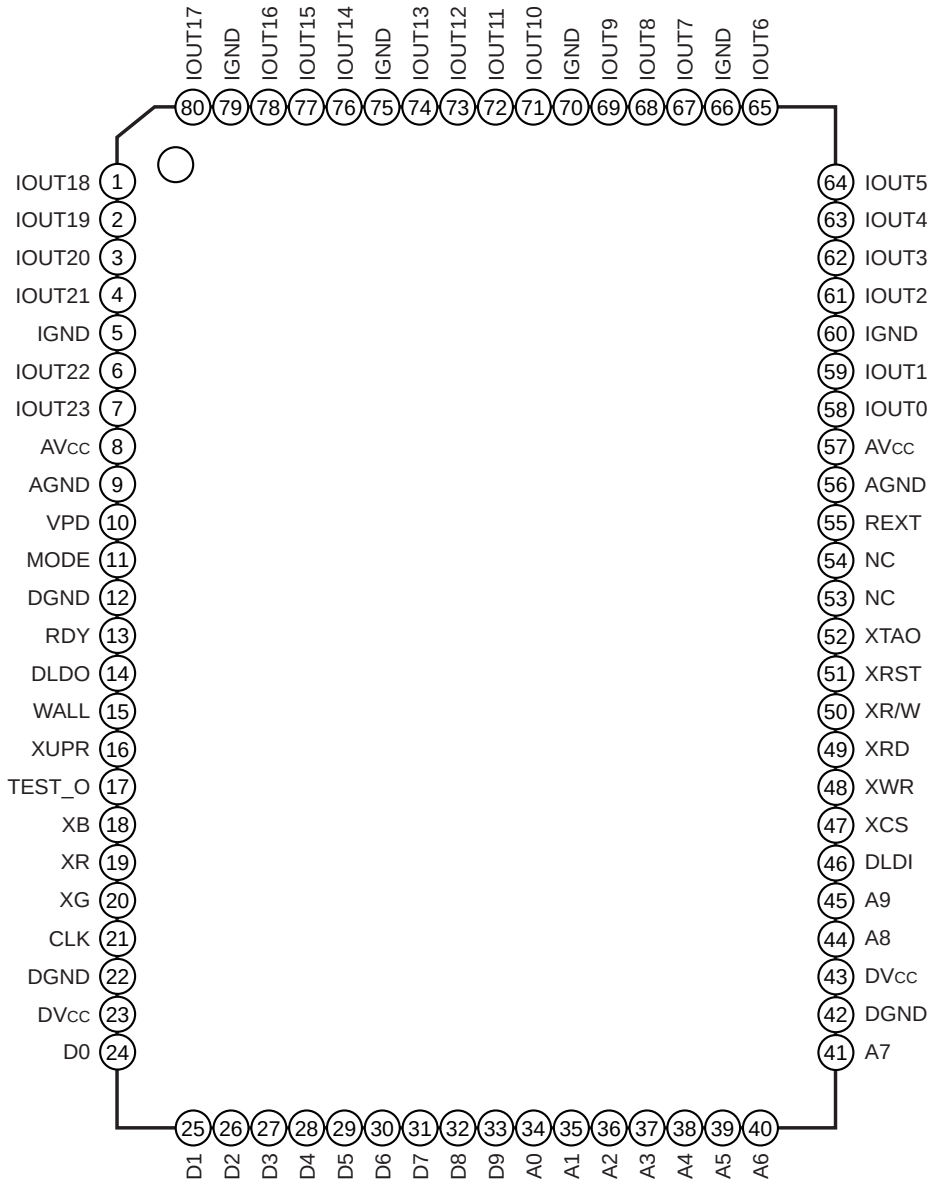
*1 When mounted on a printed circuit board

E99160-PS

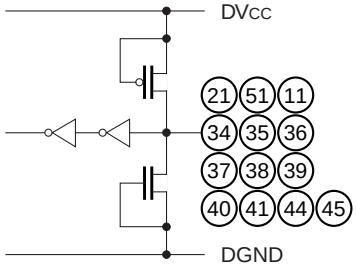
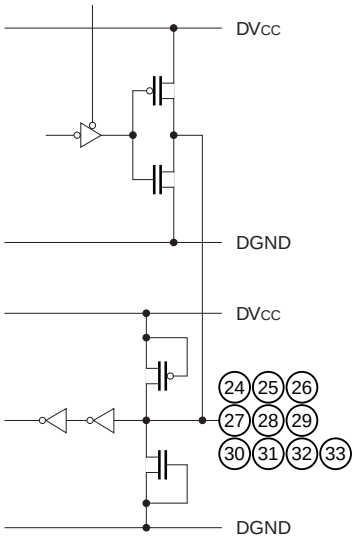
Block Diagram

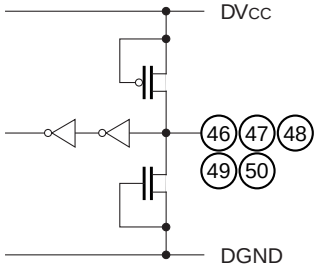


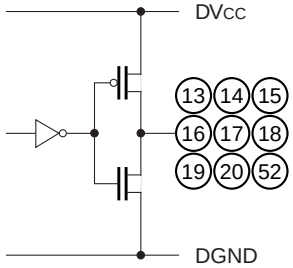
Pin Configuration (Top View)

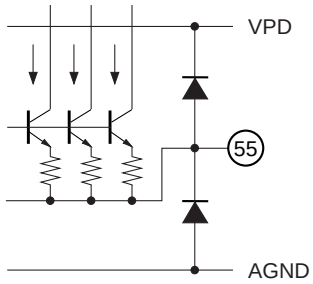
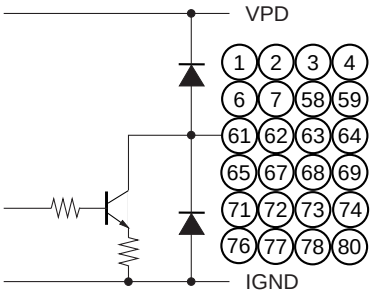


Pin Description

Pin No.	Symbol	I/O	Reference voltage level	Equivalent circuit	Description
9, 56	AGND	—	GND		Analog GND.
8, 57	AVCC	—	5V (Typ.)		Analog power supply.
12, 22, 42	DGND	—	GND		Digital GND.
23, 43	DVCC	—	5V (Typ.)		Digital power supply.
5, 60, 66, 70, 75, 79	IGND	—	GND		GND for driver output.
53, 54	NC	—			Open. This pin is not connected with the internal circuits.
21	CLK	I	CMOS		Clock input. Driver operation is synchronized with this clock.
51	XRST	I	CMOS		Reset input. The IC is initialized by inputting low level. However, the memory is not initialized. Input high level during normal operation.
11	MODE	I	CMOS		Output mode switching. Upper/Lower mode for low level input. Upper/Lower/RGB mode for high level input. (See the Description of Operation.)
34 to 41, 44	A0 to 8	I	CMOS		Address input. These pins are used to input the internal RAM (luminance data, brightness data and drive current data RAM) address.
45	A9	I	CMOS		RAM selection. The luminance data RAM is selected when this pin is low, and the drive current data RAM when high.
24 to 33	D0 to 9	I/O	CMOS		Data I/O. These pins are used to input and output data to and from the internal RAM (luminance data, brightness data and drive current data RAM). See Table 1. Read/Write Switching Condition Correspondence Table for the data I/O switching conditions.

Pin No.	Symbol	I/O	Reference voltage level	Equivalent circuit	Description
47	XCS	I	CMOS		Internal RAM chip select. Internal RAM access is enabled by inputting low level. (See Table 1. Read/Write Switching Condition Correspondence Table.)
50	XR/W	I	CMOS		Internal RAM read/write select. Write mode is selected for high level, and read mode for low level. See Table 1. Read/Write Switching Condition Correspondence Table for the actual read/write switching signal input conditions.
48	XWR	I	CMOS		Write clock input. This pin is used to input the clock for writing the luminance, brightness and drive current data. It is not synchronized with CLK.
49	XRD	I	CMOS		Read clock input. This pin is used to input the clock for externally reading the luminance, brightness and drive current data. It is not synchronized with CLK.
46	DLDI	I	CMOS		Trigger signal input for luminance data RAM (A)/(B) switching and PWM output start. (See the Timing Charts.)
10	VPD	—	5V (Typ.)		Voltage supply terminal for cathode of positive protection diode which connected to drivers (IOUTO to IOUT23) and REXT (55pin). Normally,connect to LED DC supply. However ,when the LED DC supply voltage exceeds 10V,VPD must be set 10V or less.

Pin No.	Symbol	I/O	Reference voltage level	Equivalent circuit	Description
13	RDY	O	CMOS		READY signal output. This indicates the drive current data RAM access enabled period. Access is enabled while high level is output. (See the Timing Charts.)
14	DLDO	O	CMOS		DLDI signal output. This outputs the DLDI signal synchronized with CLK.
15	WALL	O	CMOS		Write ALL signal output. One pulse (= high level signal with a width of 1 clock) is output synchronized with the rising edge of the next CLK after the final address*1 of the currently selected mode is input. Note that both the final address must be input and the XCS and XWR input levels must be low at the rising edge of this CLK. (See the Timing Charts for details.) *1 02Fh (Upper/Lower mode) 08Fh (Upper/Lower/RGB mode)
16	XUPR	O	CMOS		Upper signal output. This is used as the LED switching signal. (See the Timing Charts and Application Circuits for details.)
17	TEST_O	O	CMOS		Test signal output. This pin is unrelated to the functions of this IC. Do not connect anything; leave this pin open.
18	XB	O	CMOS		Blue signal output. This is used as the LED switching signal. (See the Timing Charts and Application Circuits for details.)
19	XR	O	CMOS		Red signal output. This is used as the LED switching signal. (See the Timing Charts and Application Circuits for details.)
20	XG	O	CMOS		Green signal output. This is used as the LED switching signal. (See the Timing Charts and Application Circuits for details.)
52	XTAO	O	CMOS		Thermal Alarm Out signal output. This pin normally outputs high level, but it outputs low level when the internal temperature rises to an abnormally high level.

Pin No.	Symbol	I/O	Reference voltage level	Equivalent circuit	Description
55	REXT	O			Drive current setting. Connect a resistor between this pin and GND. The drive current is proportional to the current flowing to this resistor. (See Table 2. Drive Current Setting and Power Consumption.)
1 to 4, 6, 7, 58, 59, 61 to 65, 67 to 69, 71 to 74, 76 to 78, 80	IOUT0 to 23	O			Drivers. These pins drive the LED.

XCS [I]	XR/W [I]	A9 [I]	Luminance		Drive current		D0 to 9 [I/O]
			Write	Read	Write	Read	
L	L	L	Disable	Enable	Disable	Disable	Output
		H	Disable	Disable	Disable	Enable	Output
	H	L	Enable	Disable	Disable	Disable	Input
		H	Disable	Disable	Enable	Disable	Input
H	L	L	Disable	Disable	Disable	Disable	Hi-Z
		H	Disable	Disable	Disable	Disable	Hi-Z
	H	L	Disable	Disable	Disable	Disable	Hi-Z
		H	Disable	Disable	Disable	Disable	Hi-Z

Table 1. Read/Write Switching Condition Correspondence Table

Rext [kΩ]	D9	D8	Io (FFh) [mA]	Istb [mA]	Pstb [W]	Po (max) [W]
2.0	0	0	21.7	22.3	0.111	1.39
2.0	0	1	43.3	38.1	0.190	1.31
2.0	1	0	65.0	53.8	0.269	1.23
2.0	1	1	86.7 *1	69.6	0.348	1.15
2.5	0	0	17.3	18.4	0.092	1.41
2.5	0	1	34.7	31.1	0.155	1.34
2.5	1	0	52.0	43.7	0.218	1.28
2.5	1	1	69.3	56.3	0.281	1.22
3.0	0	0	14.4	15.9	0.079	1.42
3.0	0	1	28.9	26.4	0.132	1.37
3.0	1	0	43.3	36.9	0.184	1.32
3.0	1	1	57.8	47.4	0.237	1.26
3.5	0	0	12.4	14.0	0.070	1.43
3.5	0	1	24.8	23.1	0.115	1.38
3.5	1	0	37.1	32.1	0.160	1.34
3.5	1	1	49.5	41.1	0.205	1.29
4.0	0	0	10.8	12.7	0.063	1.44
4.0	0	1	21.7	20.6	0.103	1.40
4.0	1	0	32.5	28.4	0.142	1.36
4.0	1	1	43.3	36.3	0.182	1.32

*1 Absolute maximum rating exceeded.

Table 2. Drive Current Setting and Power Consumption (when D0 to D7 = FFh)

Rext : External resistor that sets the DAC reference current (Iref)
D9, D8 : Data that sets the maximum drive current (Io (FFh))
Iref : DAC reference current
Iref [mA] = 1.3 [V]/Rext [kΩ]/24
Io (FFh) : Maximum drive current that can be set by D0 to D7
Io (FFh) [mA] = Iref × (2 × D9 + D8 + 1) × 800
Istb : Standby current (Internal current consumption excluding the driver block)
Istb [mA] = 3.06 + 24 × Iref × (16/3 + 24.25 × (2 × D9 + D8 + 1))
Pstb : Standby power (Internal power consumption excluding the driver block, Vcc = 5 V)
Pstb [W] = 5 [V] × Istb [mA]/1000
Po (max) : Maximum power that can be consumed by the driver block
Po (max) [W] = 1.5 [W] – Pstb [W]

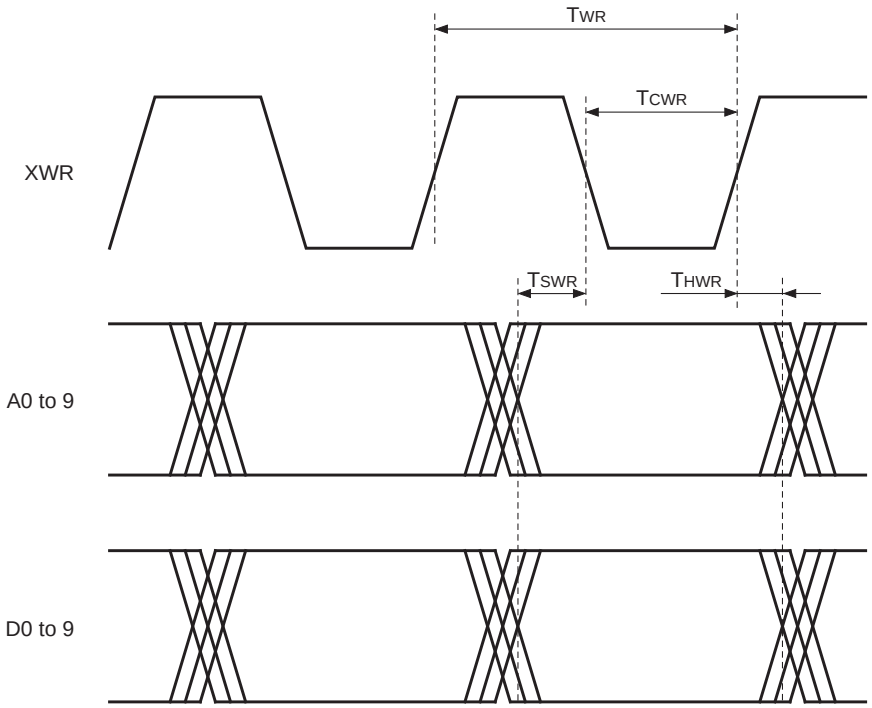
Note) Istb, Pstb and Po (max) are the values when D0 to D7 = 11111111 (FFh).
In addition, these values assume the case where all channels are set to the same drive current.

Electrical Characteristics (AVCC, DVCC = +5V, VPD = +10V, AGND, DGND, IGND = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Driver block						
PWM reference clock frequency	f_{CLK}				15	MHz
REXT pin voltage	V_{REXT}	Rext = 2kΩ	1235	1300	1365	mV
REXT pin voltage Supply voltage dependency	ΔV_{REXT}	V_{REXT} (@AVCC = 5.25V) – V_{REXT} (@AVCC = 4.75V)	0		20	mV
Standby supply current	I_{CC}	Rext = 2kΩ, D8 = D9 = 0 **Note)** Excluding the driver block	20		30	mA
PWM output resolution				10		bit
Drive current setting resolution						
Coarse Adj.				2		bit
Fine Adj.				8		bit
DC characteristics Differential linearity error	DLE	Io (FFh) = 60mA (D0 [LSB] to D7 [MSB] = FFh)			±0.8	LSB
Output current	I_{OUT}				70	mA
Output compliance voltage	Vcmp	Io = 0 to 70mA	1		VPD + 0.3	V
Logic block						
Digital input current (I, I/O)						
(H)	I_{IH}	V_{IN} = 5V	–5		5	µA
(L)	I_{IL}	V_{IN} = 0V	–5		5	µA
Digital input voltage (I, I/O)						
(H)	V_{IH}		0.7DVCC		DVCC + 0.3	V
(L)	V_{IL}		–0.3		0.3DVCC	V
Digital output voltage (O)						
(H)	V_{OH}	DVCC = 5V, I_{OH} = –2mA	4			V
(L)	V_{OL}	DVCC = 5V, I_{OL} = 4mA			0.4	V
Digital output voltage (I/O)						
(H)	V_{OZH}	DVCC = 5V, I_{OH} = –2mA	3.7			V
(L)	V_{OZL}	DVCC = 5V, I_{OL} = 4mA			0.4	V
RAM write mode						
Write cycle	T_{WR}		133.3			ns
Write pulse width	T_{CWR}		55			ns
Setup time	T_{SWR}		10			ns
Hold time	T_{HWR}		10			ns
RAM read mode						
Read cycle	T_{RD}		133.3			ns
Read pulse width	T_{CRD}		55			ns
Setup time	T_{SRD}		10			ns
Hold time	T_{HRD}		10			ns
Output delay time	T_{PDD}	Output load 50pF or less			100	ns

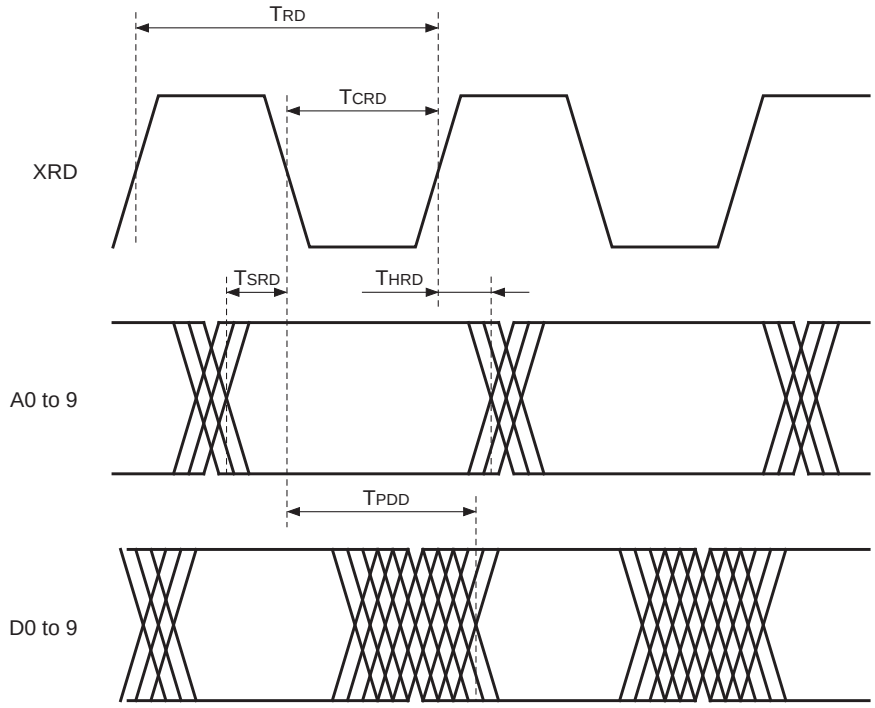
Timing Charts (RAM)

(1) Write mode (XR/W = H)



Note) The address is not latched internally, so do not change the address while XWR is low.

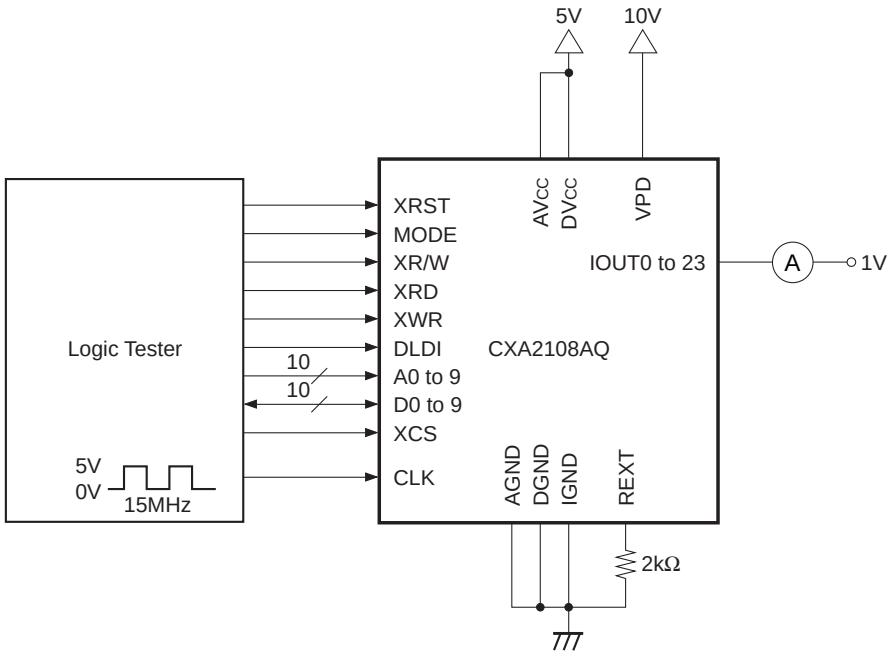
(1) Read mode (XR/W = L)



Note) The address is not latched internally, so do not change the address while XRD is low.

Electrical Characteristics Measurement Circuit

DC Characteristics Measurement Circuit



Description of Operation

1. Description

The CXA2108AQ is an LED driver for full color LED displays. The RGB luminance which becomes the video data is controlled by pulse width modulation (PWM), and the luminance variance of each LED is corrected by the drive current. The basic PWM clock width can be set in 16 steps from 1× to 16× by the brightness data, making it possible to adjust the brightness of the entire screen. There are 24 driver outputs, and time division allows driving of either two or six LEDs per output by adding an external FET or other switch.
The luminance (pulse width), drive current and brightness are set by writing data to the internal memory according to the memory map. The luminance and drive current can be set independently for each LED.

2. Relationship between the luminance data (PWM data: Dv), brightness data (Db) and the LED emitting duty

The CXA2108AQ adjusts the LED luminance which becomes the video data by changing the LED emitting time duty through PWM of the luminance data. The luminance consists of luminance data and brightness data. The luminance data (Dv) has an accuracy of 10 bits (= 1,024 steps: 0 to 1,023) and can be set independently for each LED. The brightness data (Db) controls the basic PWM clock width with 4 bits (= 16 steps: 1× to 16×), and is common data for all outputs. The brightness data is normally used when adjusting the brightness of the entire screen.
Labeling the LED emitting cycle as Ts and the CLK cycle as T_{CLK} , this relationship is given by the following formula.

$$Ts = 1{,}024 \times 16 \times T_{CLK}$$

The LED emitting time Tv within this Ts time is:

$$Tv = Dv \times Db \times T_{CLK}$$

Therefore, the emitting duty is:

$$Tv/Ts \times 100 = (Dv \times Db)/(1{,}024 \times 16) \times 100\ [\%]$$

The drive current waveform and the relationship between the luminance data, brightness data and the emitting duty are shown below.

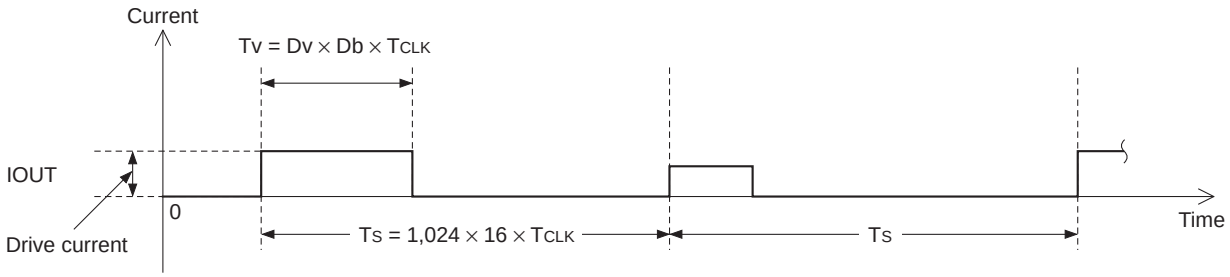


Fig. 1. Drive Current Waveform

Luminance data (Dv) D9 to 0 D9 D0	Nv*1 and emitting duty							
	Brightness (D3 to 0) = 0000			Brightness (D3 to 0) = 0111			Brightness (D3 to 0) = 1111	
	Nv	Emitting duty [%]		Nv	Emitting duty [%]		Nv	Emitting duty [%]
0000000000	0	0		0	0		0	0
0000000001	1	0.006		8	0.049		16	0.098
0000000010	2	0.012		16	0.098		32	0.195
:	:	:	. .	:	:	. .	:	:
1000000000	512	3.125		4096	25.00		8192	50.00
:	:	:		:	:		:	:
1111111111	1023	6.244		8184	49.95		16368	99.90

*1 $Nv = Tv/T_{CLK} = Dv \times Db$

Table 3. Relationship Between Luminance Data, Brightness Data and Emitting Duty

3. Drive current data (Dd)

Even when driving LEDs of the same color with the same current value, individual differences in characteristics result in an uneven emitting intensity. In addition, the required current value also differs according to the emitting color (RGB). That is to say, the necessary current differs for each LED. This drive current IOUT corresponds to the amplitude of the IOUT output PWM waveform as shown in Fig. 1. The CXA2108AQ can set this current independently for each LED using Coarse Adj. (2 bits: D8, D9) and Fine Adj. (8 bits: D0 to D7). The maximum values of the drive current (Io (FFh): IOUT @ D0 to D7 = FFh) are varied in 4 levels by Coarse Adj. (2 bits: D8, D9). The minimum drive current (Io (00h): IOUT @ D0 to D7 = 00h) is approximately 0mA,regardless of the Coarse Adj. range. The range from the minimum to the maximum drive current can be set at an accuracy of 8 bits (D0 to D7 = 256 steps).

Note that this drive current is generated using the Iref described in 6. as the reference.

The relationship between the Fine Adj. (8 bits: D0 to D7) data and the drive current, and the drive current data (D0 to D9) to drive current correspondence table are shown below.

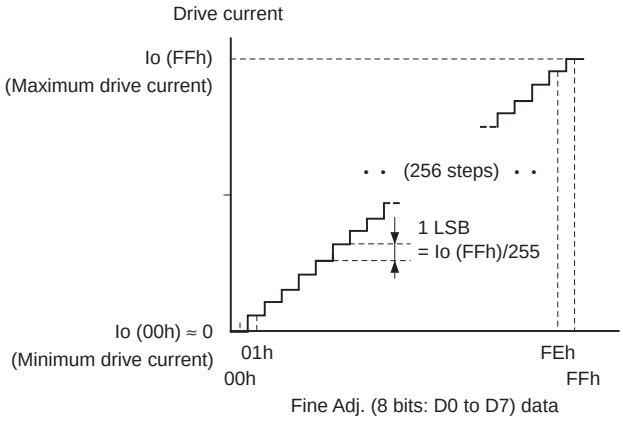


Fig. 2. Relationship Between Fine Adj. (8 bits: D0 to D7) Data and Drive Current

Drive current data (Dd) D7 to 0 D7 D0	Drive current				
	D9 D8 0 0	D9 D8 0 1	D9 D8 1 0	D9 D8 1 1	
00000000 (00h)	0	0	0	0	Minimum drive current Io (00h)
:	:	:	:	:	
10000000 (80h)	400 × Iref	800 × Iref	1200 × Iref	1600 × Iref	
:	:	:	:	:	
11111111 (FFh)	800 × Iref	1600 × Iref	2400 × Iref	3200 × Iref	Maximum drive current Io (FFh)

Table 4. Drive Current Data (D0 to D9) to Drive Current Correspondence Table

4. Operating modes (Upper/Lower, Upper/Lower/RGB)

The CXA2108AQ has the following two operation modes which are set by the MODE pin.

4-1. Upper/Lower mode (MODE = low)

In this mode, two LEDs are driven by time division for each IOUT output.

First, PWM waveform output starts triggered by the DLDI input signal. In this mode, two kinds of luminance data are output by time division for each output. Labeling these data as U and L, the driver outputs the data in the order of U → L → U → L → U → and so on. The XUPR pin output voltage switches in sync with the LED emitting cycle Ts in the order of L → H → L → and so on, so this can be used as the FET or other switch signal for switching the LED. (See Fig. 6. Timing Chart 2-1 and Fig. 11. Application Circuit (1) for details.)

New PWM data is output when the next DLDI signal is input.

4-2. Upper/Lower/RGB mode (MODE = high)

In this mode, six LEDs can be driven by time division for each IOUT output.

PWM waveform output starts triggered by the DLDI input signal. In this mode, six kinds of luminance data are output by time division for each output. Labeling these data as UB, UR, UG, LB, LR and LG, the driver switches the output in the order of UB → UR → UG → LB → LR → LG → UB → and so on. Like Upper/Lower mode, the XUPR and also the XB, XR and XG output voltages switch in sync with Ts, so these can be used as the FET or other switch signals for switching the LEDs. The output voltages at this time are: XUPR = low for U∗, XUPR = high for L∗, XB = low (XR = XG = high) for ∗B, XR = low (XB = XG = high) for ∗R, and XG = low (XB = XR = high) for ∗G. (See Fig. 7. Timing Chart 2-2 and Fig. 12. Application Circuit (2) for details.)

New PWM data is output when the next DLDI signal is input.

5. Luminance data memory and DLDI signal

The CXA2108AQ uses two sets of 6-word × 24-channel × 10-bit RAM (RAM (A), RAM (B)) as luminance data memories, and switches these memories. While the data in one memory is being loaded internally and PWM output is being performed, the next luminance data can be written to the other memory from an external source. Memory switching is performed by inputting a trigger signal to the DLDI pin. The read/write enabled memory alternates from A → B → A → and so on, and the memory used for PWM output alternates from B → A → B → and so on each time the signal is input to DLDI. The DLDI signal switches the memory, and at the same time functions as the PWM output start trigger pulse. See the Timing Charts for details.

6. Reference current (Iref)

The drive current is generated using the current flowing to an external resistor as the reference. This resistor Rext is connected between the REXT pin and GND. The REXT pin voltage is designed to be unaffected by supply voltage, temperature or other fluctuations, and is always a constant voltage (approximately 1.3V). Therefore, a constant current can be realized by using a resistor that does not have temperature characteristics. The current obtained by dividing this current value by the number of IOUT outputs (24) is defined as Iref.

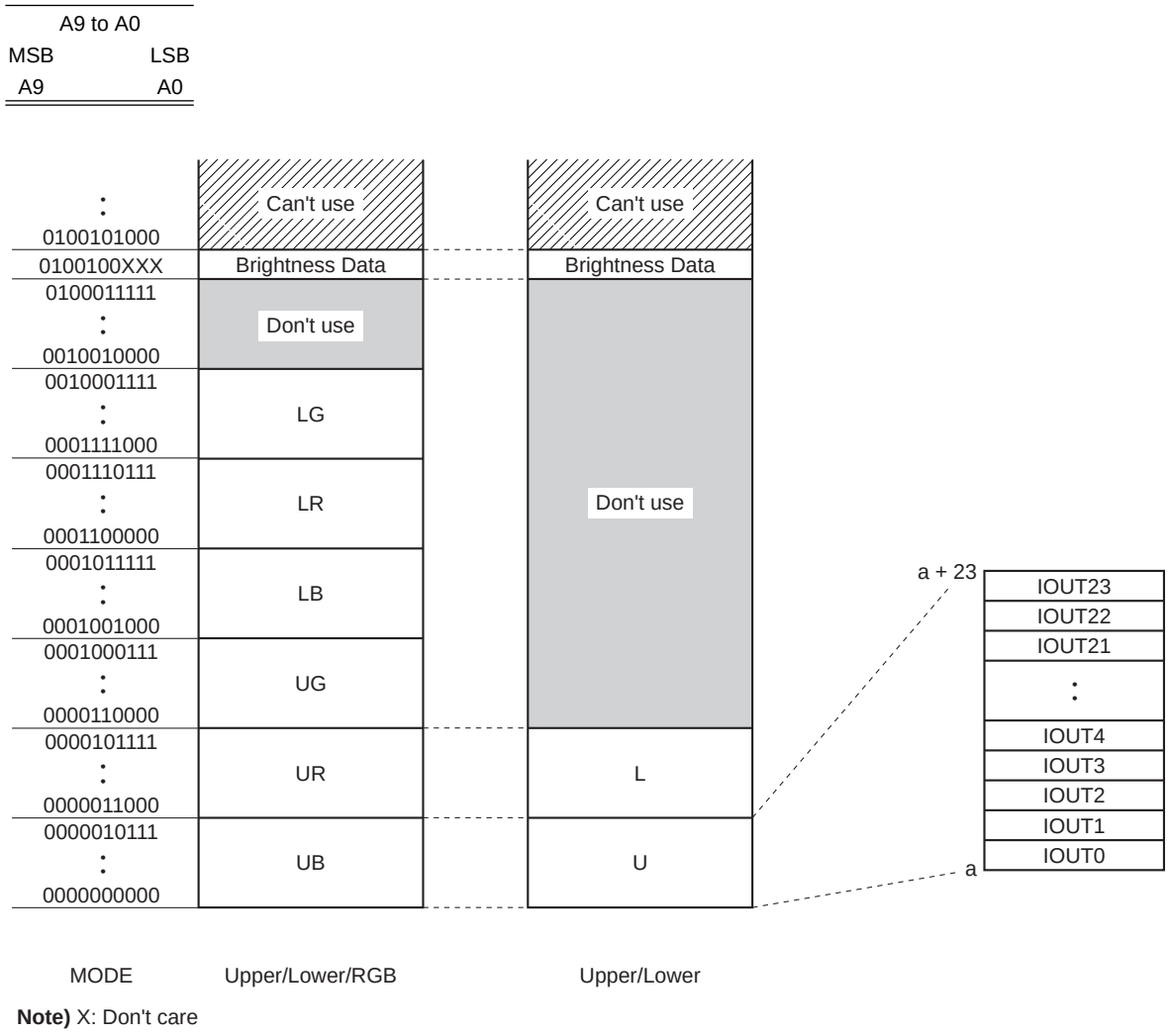
$$Iref = (1.3/Rext)/24$$

The maximum drive current value can be changed by varying the resistance value. See Table 2. Drive Current Setting and Power Consumption for details.

7. Data setting

The above mentioned luminance data Dv, brightness data Db and drive current data Dd are set using address input pins A0 to A9 and data I/O pins D0 to D9. See the Timing Charts for the memory read/write enabled period, and Table 1. Read/Write Switching Condition Correspondence Table for the pin setting conditions. The address, data, XWR and XRD setup, hold and other timings should be as stated in the Electrical Characteristics. See Tables 5. and 6. LED Driver Memory Map with respect to the memory address of each IOUT output pin (IOUT0 to IOUT23).

The relationship between the data and the memory address is as follows.



Note) X: Don't care

Fig. 3. Relationship Between Memory Address and Data (Luminance Data Dv, Brightness Data Db)

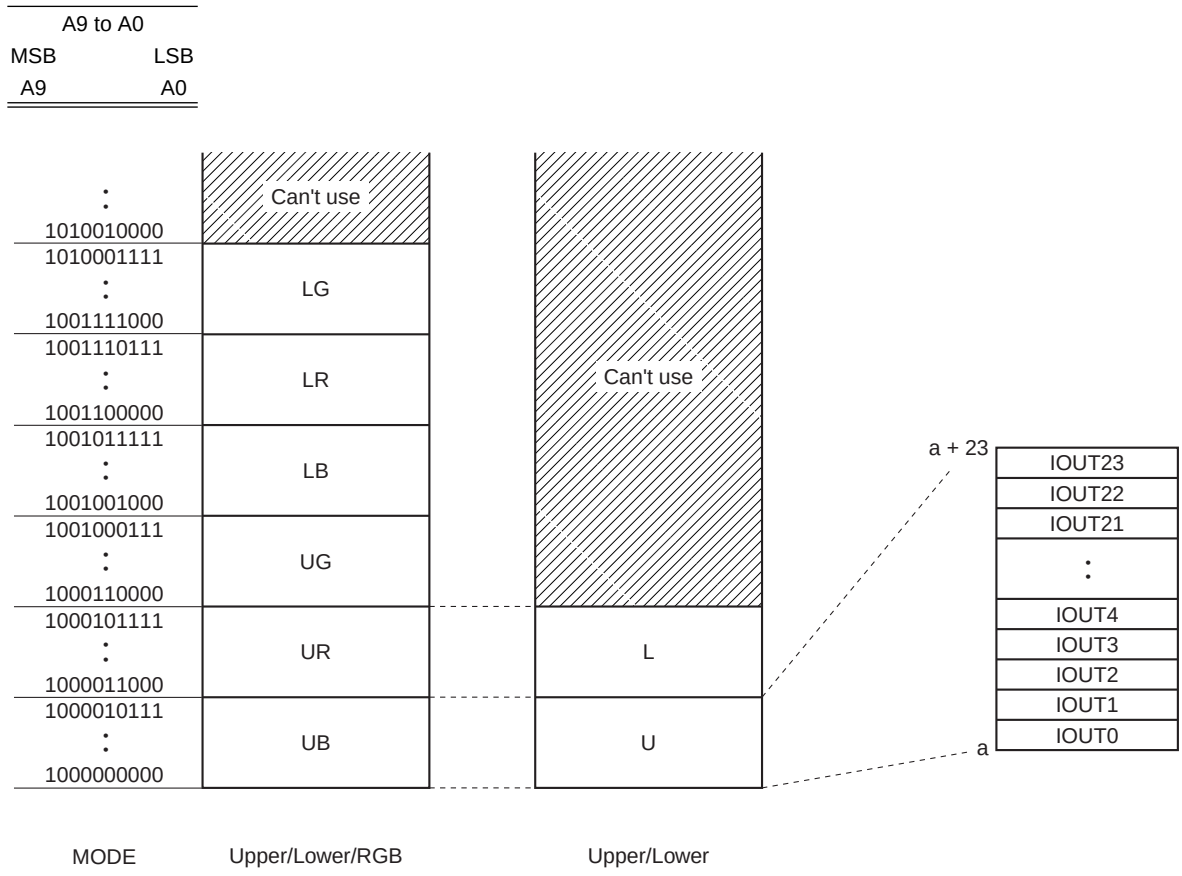


Fig. 4. Relationship Between Memory Address and Data (Drive Current Data Dd)

Luminance Data

		A9 to A3																	
		UPPER (U)			LOWER (L)														
		0000000	0000001	0000010	0000011	0000100	0000101	0000110	0000111	0001000	0001001	0001010	0001011	0001100	0001101	0001110	0001111	0010000	0010001
A2 to A0	000	IOUT0	IOUT8	IOUT16	IOUT0	IOUT8	IOUT16												
	001	IOUT1	IOUT9	IOUT17	IOUT1	IOUT9	IOUT17												
	010	IOUT2	IOUT10	IOUT18	IOUT2	IOUT10	IOUT18												
	011	IOUT3	IOUT11	IOUT19	IOUT3	IOUT11	IOUT19												
	100	IOUT4	IOUT12	IOUT20	IOUT4	IOUT12	IOUT20												
	101	IOUT5	IOUT13	IOUT21	IOUT5	IOUT13	IOUT21												
	110	IOUT6	IOUT14	IOUT22	IOUT6	IOUT14	IOUT22												
	111	IOUT7	IOUT15	IOUT23	IOUT7	IOUT15	IOUT23												

Drive Current Data

		UPPER (U)			LOWER (L)														
		1000000	1000001	1000010	1000011	1000100	1000101	1000110	1000111	1001000	1001001	1001010	1001011	1001100	1001101	1001110	1001111	1010000	1010001
A2 to A0	000	IOUT0	IOUT8	IOUT16	IOUT0	IOUT8	IOUT16												
	001	IOUT1	IOUT9	IOUT17	IOUT1	IOUT9	IOUT17												
	010	IOUT2	IOUT10	IOUT18	IOUT2	IOUT10	IOUT18												
	011	IOUT3	IOUT11	IOUT19	IOUT3	IOUT11	IOUT19												
	100	IOUT4	IOUT12	IOUT20	IOUT4	IOUT12	IOUT20												
	101	IOUT5	IOUT13	IOUT21	IOUT5	IOUT13	IOUT21												
	110	IOUT6	IOUT14	IOUT22	IOUT6	IOUT14	IOUT22												
	111	IOUT7	IOUT15	IOUT23	IOUT7	IOUT15	IOUT23												

Brightness data: A9 to A3 = 0100100b (24h) A2 to A0 = Don't care

Table 5. LED Driver Memory Map (Upper/Lower mode)

Luminance Data

		A9 to A3																	
		UPPER									LOWER								
		B		(UB)	R		(UR)	G		(UG)	B		(LB)	R		(LR)	G		(LG)
		0000000	0000001	0000010	0000011	0000100	0000101	0000110	0000111	0001000	0001001	0001010	0001011	0001100	0001101	0001110	0001111	0010000	0010001
A2 to A0	000	IOUT0	IOUT8	IOUT16	IOUT0	IOUT8	IOUT16	IOUT0	IOUT8	IOUT16	IOUT0	IOUT8	IOUT16	IOUT0	IOUT8	IOUT16	IOUT0	IOUT8	IOUT16
	001	IOUT1	IOUT9	IOUT17	IOUT1	IOUT9	IOUT17	IOUT1	IOUT9	IOUT17	IOUT1	IOUT9	IOUT17	IOUT1	IOUT9	IOUT17	IOUT1	IOUT9	IOUT17
	010	IOUT2	IOUT10	IOUT18	IOUT2	IOUT10	IOUT18	IOUT2	IOUT10	IOUT18	IOUT2	IOUT10	IOUT18	IOUT2	IOUT10	IOUT18	IOUT2	IOUT10	IOUT18
	011	IOUT3	IOUT11	IOUT19	IOUT3	IOUT11	IOUT19	IOUT3	IOUT11	IOUT19	IOUT3	IOUT11	IOUT19	IOUT3	IOUT11	IOUT19	IOUT3	IOUT11	IOUT19
	100	IOUT4	IOUT12	IOUT20	IOUT4	IOUT12	IOUT20	IOUT4	IOUT12	IOUT20	IOUT4	IOUT12	IOUT20	IOUT4	IOUT12	IOUT20	IOUT4	IOUT12	IOUT20
	101	IOUT5	IOUT13	IOUT21	IOUT5	IOUT13	IOUT21	IOUT5	IOUT13	IOUT21	IOUT5	IOUT13	IOUT21	IOUT5	IOUT13	IOUT21	IOUT5	IOUT13	IOUT21
	110	IOUT6	IOUT14	IOUT22	IOUT6	IOUT14	IOUT22	IOUT6	IOUT14	IOUT22	IOUT6	IOUT14	IOUT22	IOUT6	IOUT14	IOUT22	IOUT6	IOUT14	IOUT22
	111	IOUT7	IOUT15	IOUT23	IOUT7	IOUT15	IOUT23	IOUT7	IOUT15	IOUT23	IOUT7	IOUT15	IOUT23	IOUT7	IOUT15	IOUT23	IOUT7	IOUT15	IOUT23

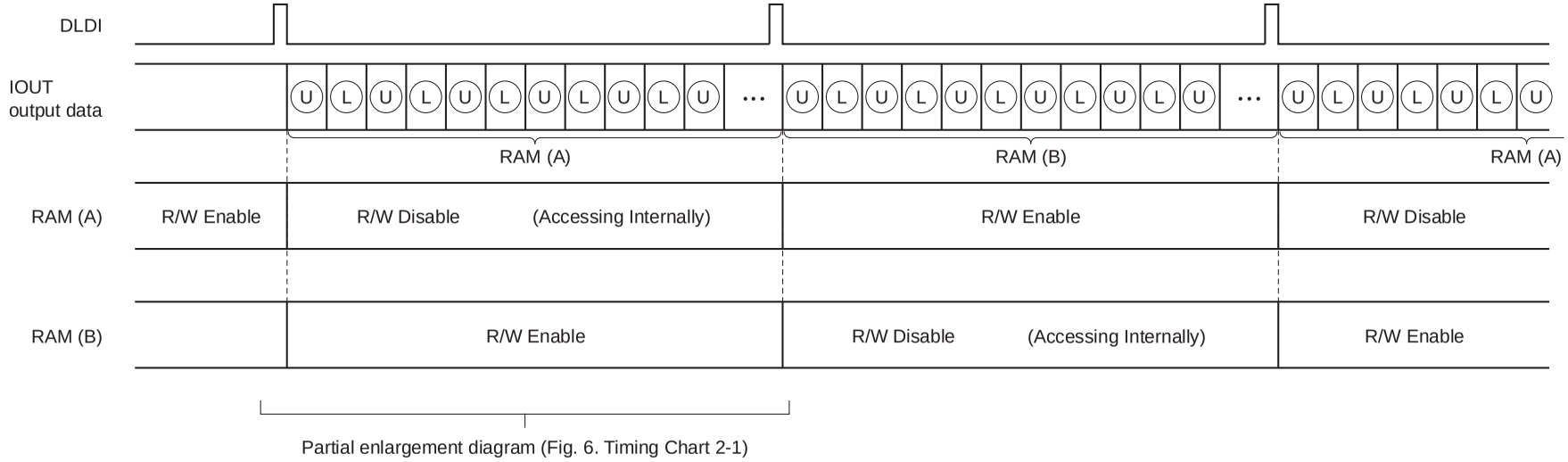
Drive Current Data

		UPPER									LOWER								
		B		(UB)	R		(UR)	G		(UG)	B		(LB)	R		(LR)	G		(LG)
		1000000	1000001	1000010	1000011	1000100	1000101	1000110	1000111	1001000	1001001	1001010	1001011	1001100	1001101	1001110	1001111	1010000	1010001
A2 to A0	000	IOUT0	IOUT8	IOUT16	IOUT0	IOUT8	IOUT16	IOUT0	IOUT8	IOUT16	IOUT0	IOUT8	IOUT16	IOUT0	IOUT8	IOUT16	IOUT0	IOUT8	IOUT16
	001	IOUT1	IOUT9	IOUT17	IOUT1	IOUT9	IOUT17	IOUT1	IOUT9	IOUT17	IOUT1	IOUT9	IOUT17	IOUT1	IOUT9	IOUT17	IOUT1	IOUT9	IOUT17
	010	IOUT2	IOUT10	IOUT18	IOUT2	IOUT10	IOUT18	IOUT2	IOUT10	IOUT18	IOUT2	IOUT10	IOUT18	IOUT2	IOUT10	IOUT18	IOUT2	IOUT10	IOUT18
	011	IOUT3	IOUT11	IOUT19	IOUT3	IOUT11	IOUT19	IOUT3	IOUT11	IOUT19	IOUT3	IOUT11	IOUT19	IOUT3	IOUT11	IOUT19	IOUT3	IOUT11	IOUT19
	100	IOUT4	IOUT12	IOUT20	IOUT4	IOUT12	IOUT20	IOUT4	IOUT12	IOUT20	IOUT4	IOUT12	IOUT20	IOUT4	IOUT12	IOUT20	IOUT4	IOUT12	IOUT20
	101	IOUT5	IOUT13	IOUT21	IOUT5	IOUT13	IOUT21	IOUT5	IOUT13	IOUT21	IOUT5	IOUT13	IOUT21	IOUT5	IOUT13	IOUT21	IOUT5	IOUT13	IOUT21
	110	IOUT6	IOUT14	IOUT22	IOUT6	IOUT14	IOUT22	IOUT6	IOUT14	IOUT22	IOUT6	IOUT14	IOUT22	IOUT6	IOUT14	IOUT22	IOUT6	IOUT14	IOUT22
	111	IOUT7	IOUT15	IOUT23	IOUT7	IOUT15	IOUT23	IOUT7	IOUT15	IOUT23	IOUT7	IOUT15	IOUT23	IOUT7	IOUT15	IOUT23	IOUT7	IOUT15	IOUT23

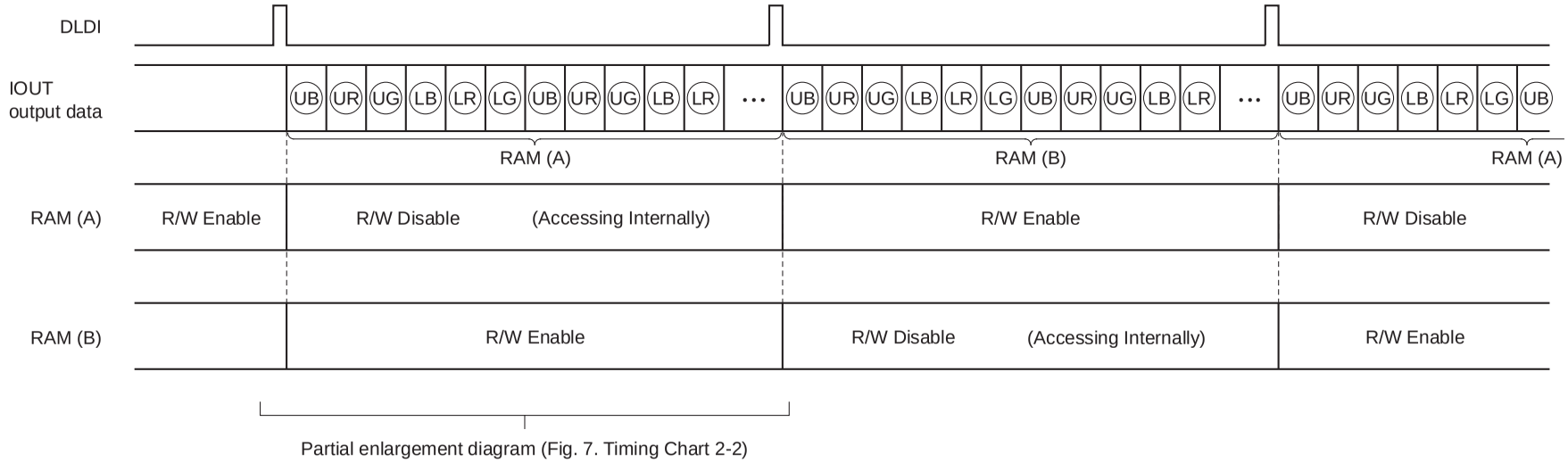
Brightness data: A9 to A3 = 0100100b (24h) A2 to A0 = Don't care

Table 6. LED Driver Memory Map (Upper/Lower/RGB mode)

Case 1: Upper/Lower mode

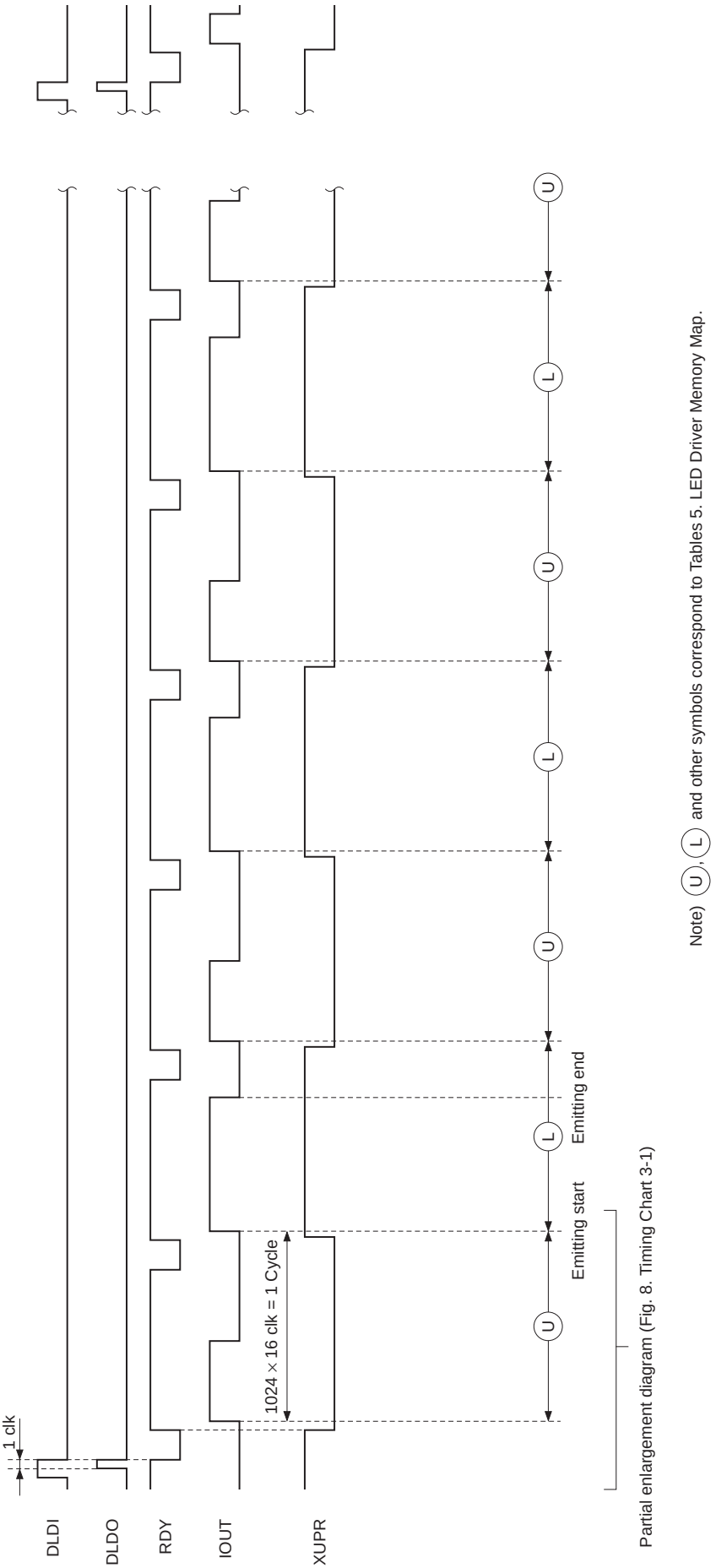


Case 2: Upper/Lower/RGB mode



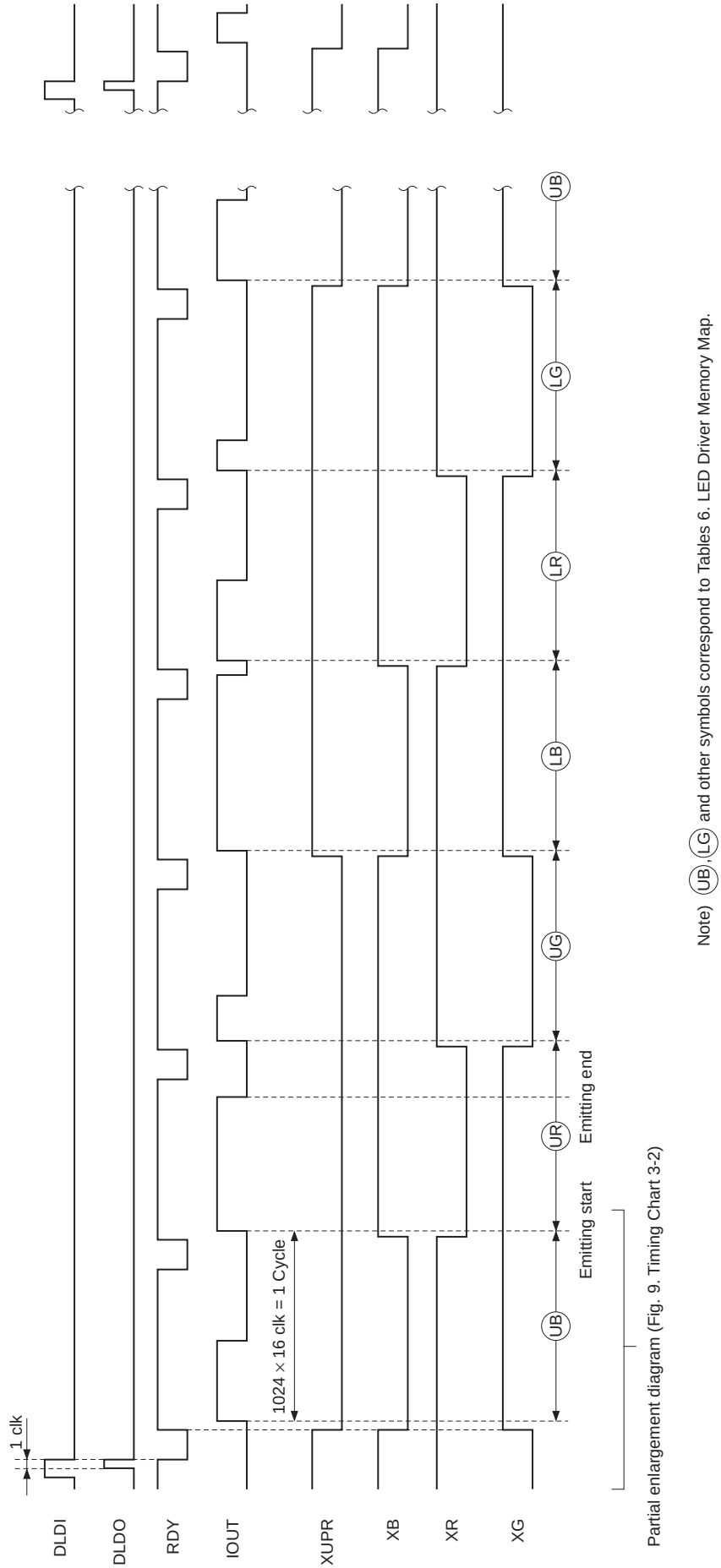
Note) (U), (L) and other symbols correspond to Tables 5. and 6. LED Driver Memory Map.

Fig. 5. Timing Chart 1. Relationship between PWM waveform output and luminance RAM (A)/(B) with respect to DLDI input pulse



Note) (U), (L) and other symbols correspond to Tables 5. LED Driver Memory Map.

Fig. 6. Timing Chart 2-1. DLDI input to IOUT output (Upper/Lower mode)



Note) (UB), (LG) and other symbols correspond to Tables 6. LED Driver Memory Map.

Fig. 7. Timing Chart 2-2. DLDI input to IOUT output (Upper/Lower/RGB mode)

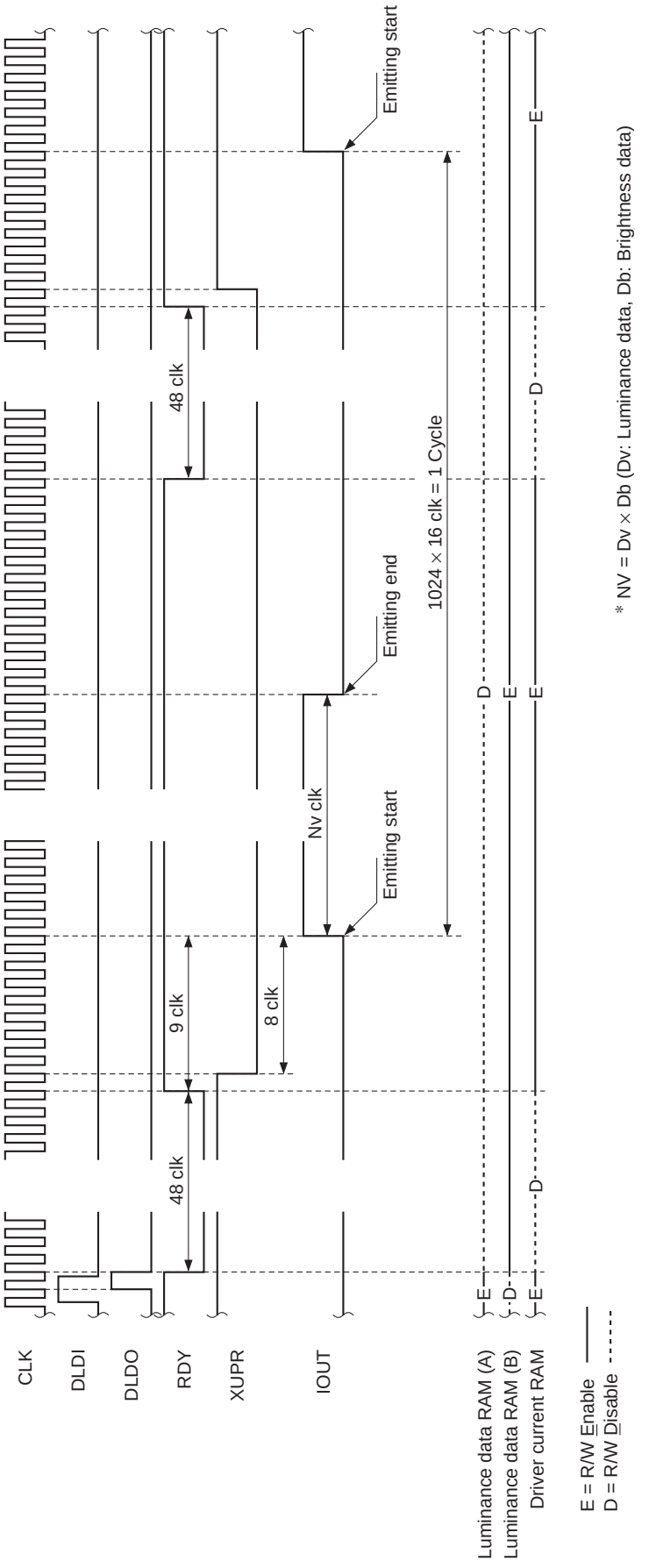


Fig. 8. Timing Chart 3-1. DLDI input to IOUT output (1 cycle) example (Upper/Lower mode)

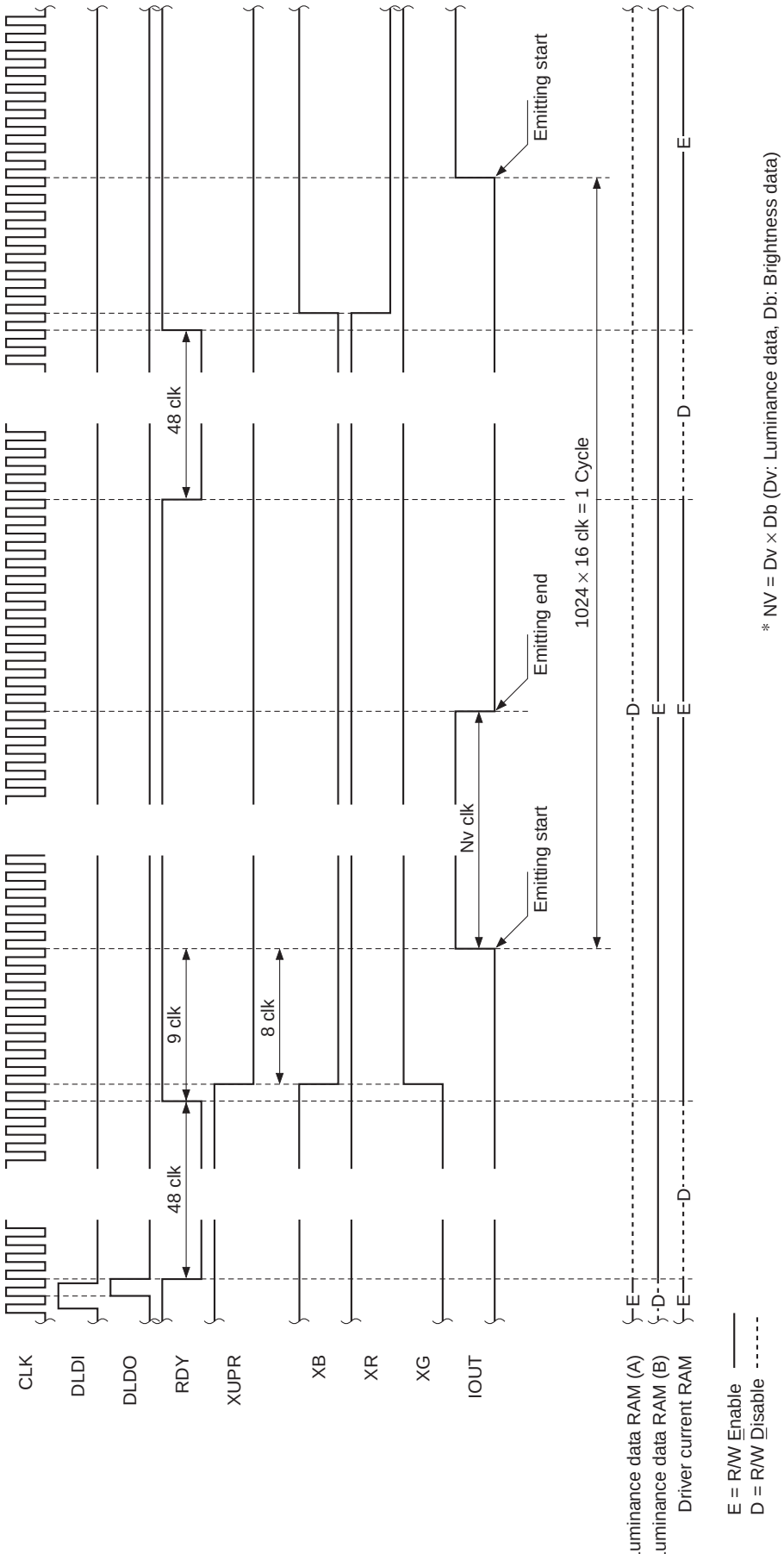


Fig. 9. Timing Chart 3-2. DLDI input to IOUT output (1 cycle) example (Upper/Lower/RGB mode)

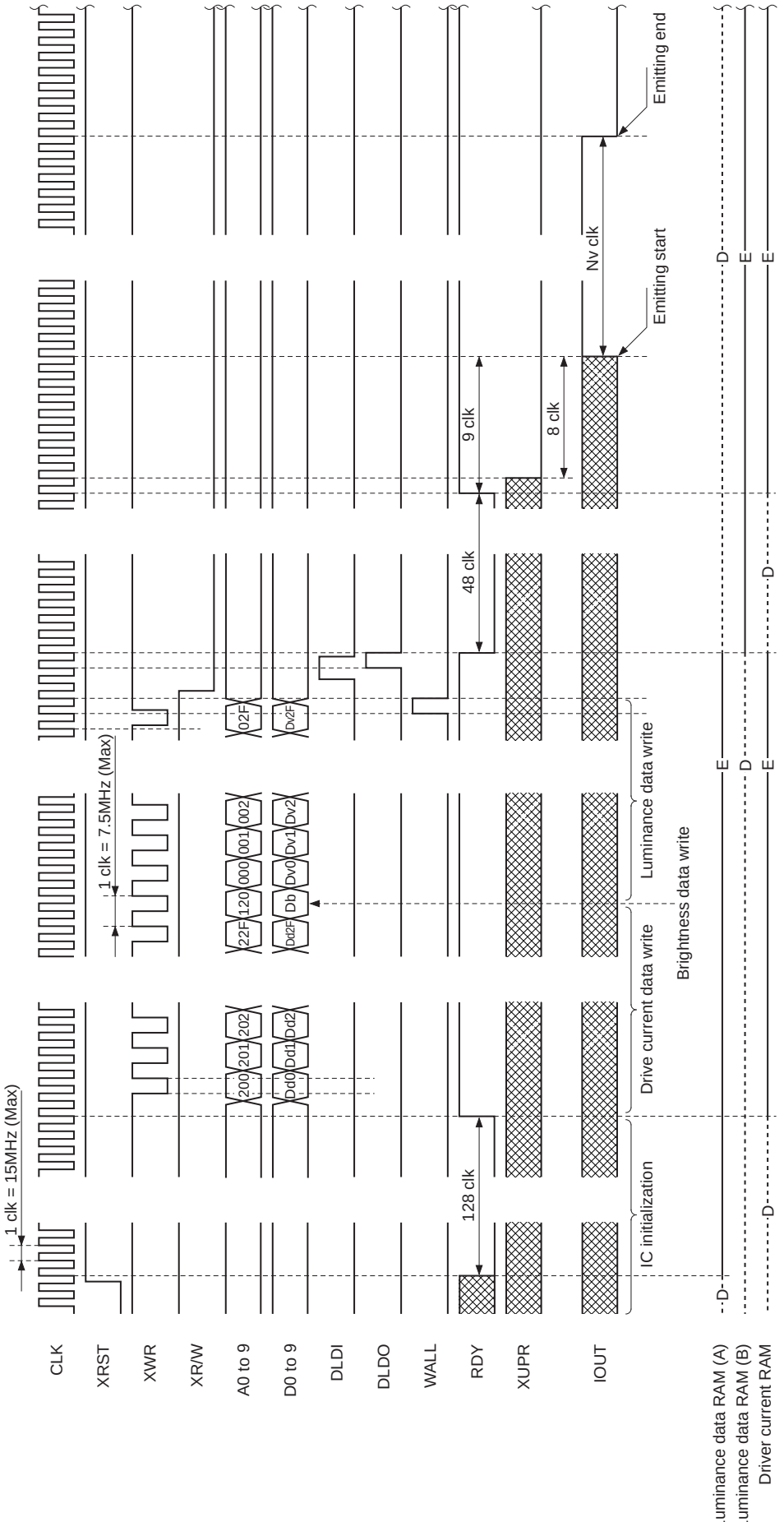
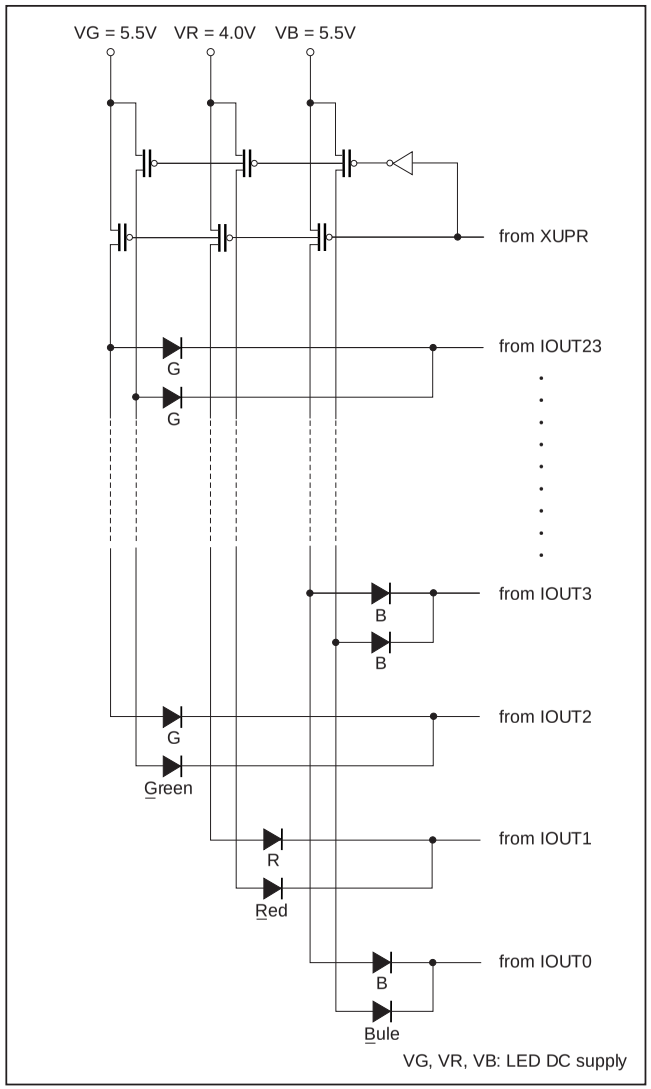
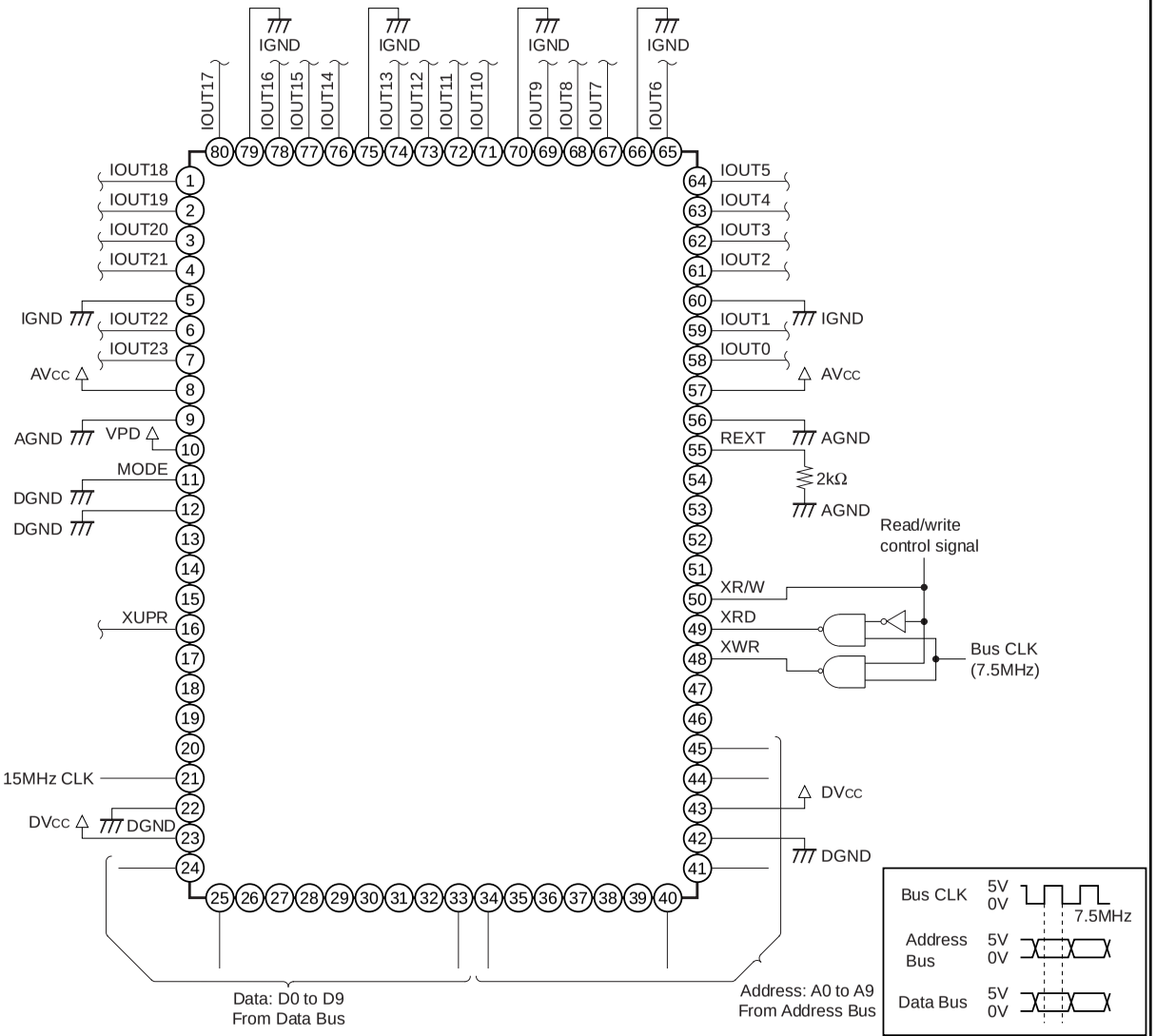


Fig. 10. Timing Chart 4. XRST input to IOUT output example (Upper/Lower mode)

Application Circuit

UPPER/LOWER mode

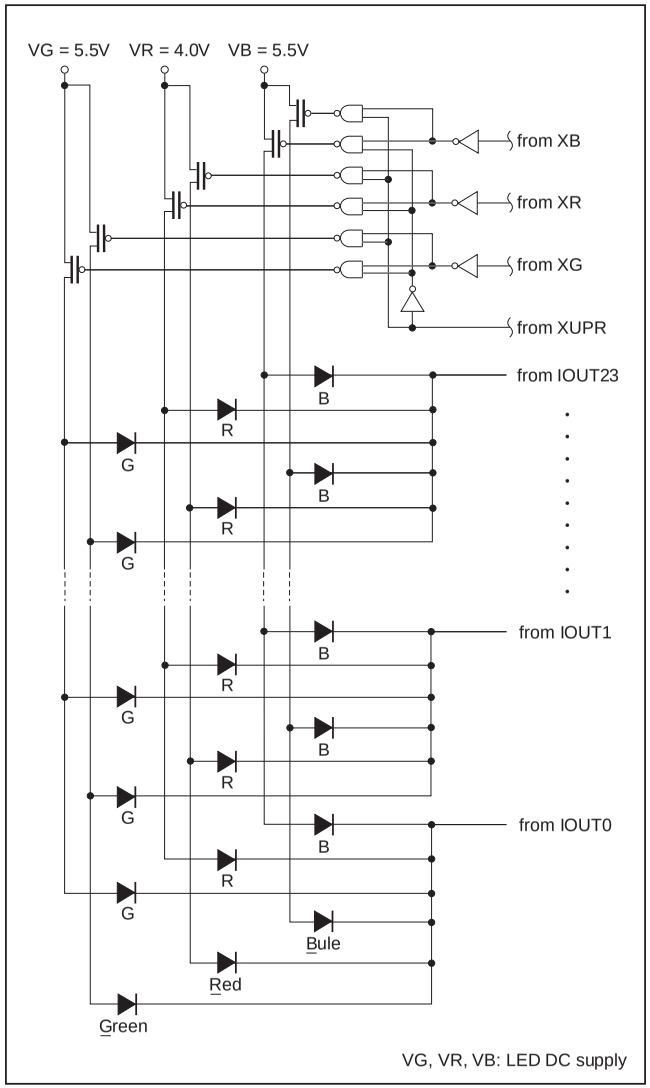


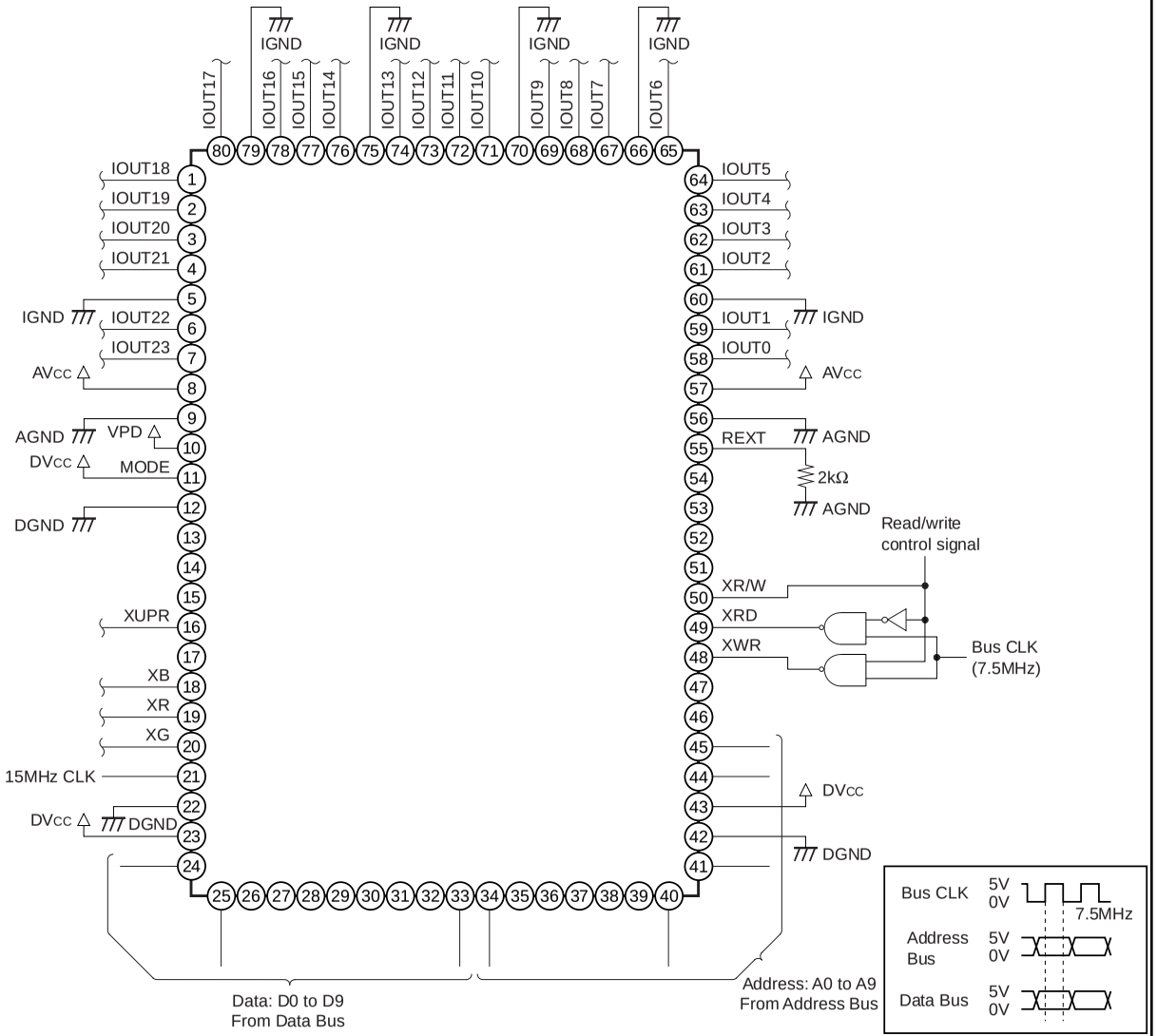


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Fig. 11. Application Circuit (1)

UPPER/LOWER/RGB mode



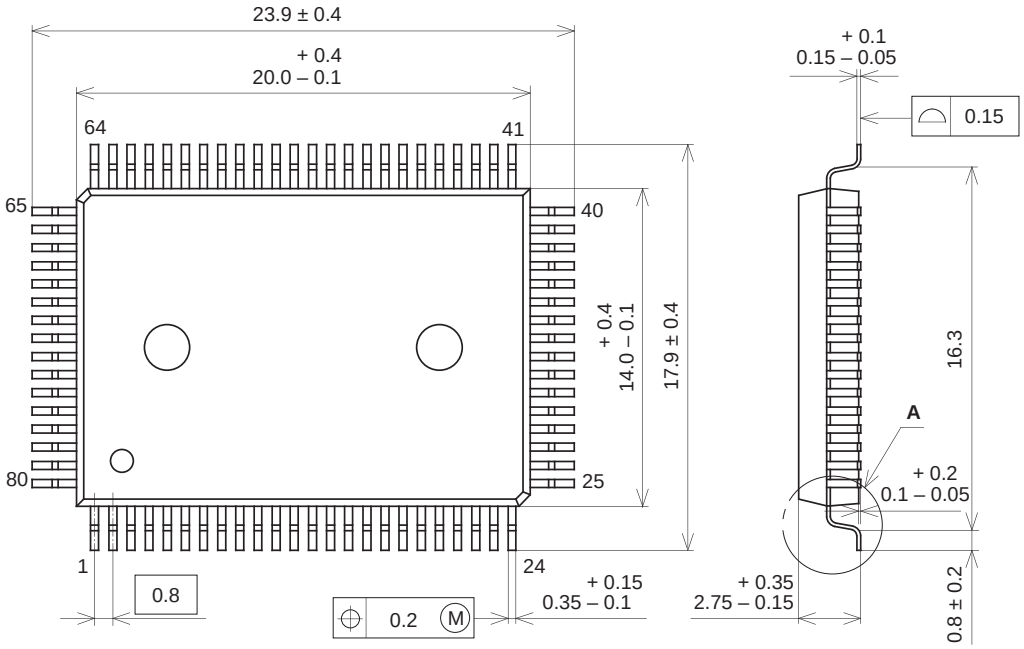


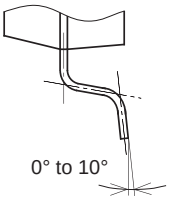
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Fig. 12. Application Circuit (2)

Package Outline Unit: mm

80PIN QFP (PLASTIC)





DETAIL **A**

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g