TOYOCOM

Crystal Clock Oscillator

TCO-743TH7

FULL DIP Double-Sealed TTL

Features

- TTL logic output
- DIP-14 pin package compatible
- Tight stability (±10 ppm)
- Enable/Disable feature

Absolute Maximum Ratings

Parameter	Symbol	Rating
Supply voltage	V_{CC}	-0.5 to +7.0 V
Input voltage	V_{IN}	-0.5 to V_{CC}+0.5 V
Output voltage	V_O	-0.5 to V_{CC}+0.5 V
Input current	I_{IN}	±10 mA
Output current	I_O	±25 mA
Storage temperature	T_{stg}	-40 to +80 °C

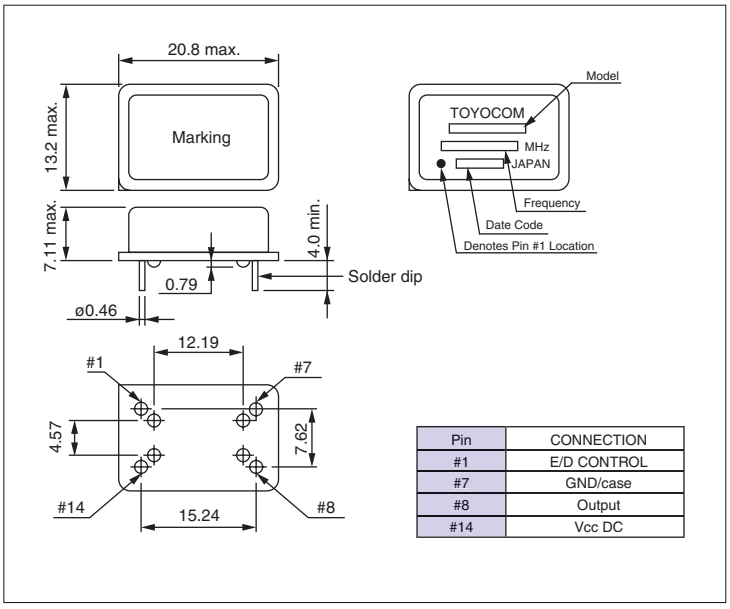
Specifications

Parameter		TCO-743TH7	Conditions
Frequency	fo	1.5 to 60 MHz	
Frequency Stability	Δf/fo	±10 ppm max.	(*1)
Operating Temperature	Topr	0 °C to +70 °C	
Supply Voltage	Vcc	+5.0 V ±10 %	DC
Supply Current	Icc	See Table A (max.)	Vcc=+5.5V
Input Voltage	V_{IH} V_{IL}	V_{IH}=+3.5 V min. / V_{IL}=+1.5 V max.	#1:V_{IH} or OPEN ··· Enable #1:V_{IL} or GND ··· Disable
Output Voltage	V_{OH} V_{OL}	V_{OH}=+4.0 V min. / V_{OL}=+0.4 V max.	I_{OH}=-4mA, I_{OL}=+16mA
Symmetry	SYM	45 to 55 %	at +1.4V
Rise/Fall time	tr/tf	See Table A (max.)	at +0.4 to +2.4V
Fanout	n	10 max.	1.6mA/gate
Start-up time	tst	4 ms max. 10 ms max.	1.5 ≤ fo ≤ 26 MHz (*2) 26 < fo ≤ 60 MHz (*2)

*1 Inclusive of calibration tolerance at +25°C, operating temperature.

*2 Rise time (0 to +4.5V) of Vcc >150μs

Package Outlines [Dimensions in mm]



Pin	CONNECTION
#1	E/D CONTROL
#7	GND/case
#8	Output
#14	Vcc DC

Table A

Freq. (MHz)	1.5 ≤ fo ≤ 10	10 < fo ≤ 26	26 < fo ≤ 60
Icc (mA)	15	20	40
tr,tf (ns)	5	5	5

Test Circuit

See Test Circuit page TEST-2

(2001. 2.)