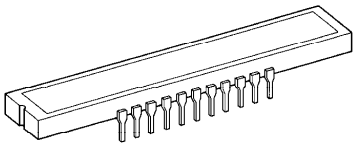
TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

TCD1500C

The TCD1500C is a high sensitive and low dark current 5340-elements linear image sensor. The sensor can be used for facsimile, imagescanner and OCR. The signal pre-processing circuit which is composed of Sample and Hold circuit and Pre-amplifier circuit. The device contains a row of 5340 photodiodes, which provide a 16 lines / mm (400DPI) across a A3 size paper and besides 24 lines / mm (600DPI) across a A4 size paper.



WDIP22-C-400-2.54B

Weight : 5.4g (Typ.)

FEATURES

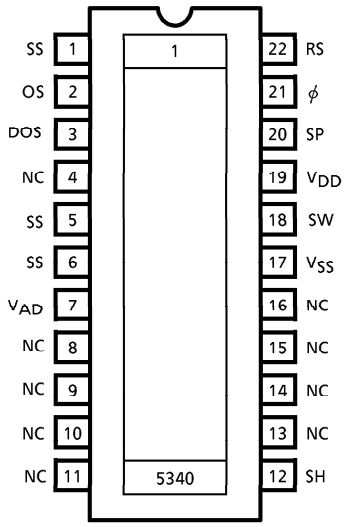
- Number of Image Sensing Elements : 5340
- Image Sensing Element Size : 7μm by 7μm on 7μm centers
- Photo Sensing Region : High sensitive pn photodiode
- Clock : 2 phase
- Internal Circuit : S / H circuit, Pre-Amplifier circuit
- Package : 22 pin cerdip

MAXIMUM RATINGS (Note 1)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	V_ϕ	−0.3~15	V
Shift Pulse Voltage	V_{SH}		V
Reset Pulse Voltage	V_{RS}		V
Sample and Hold Pulse Voltage	V_{SP}		V
Power Supply Voltage (Analog)	V_{AD}		V
Power Supply Voltage (Driver)	V_{DD}		V
Operating Temperature	T_{opr}	−25~60	°C
Storage Temperature	T_{stg}	−40~100	°C

(Note 1) All voltage are with respect to SS and V_{SS} terminals (Ground).

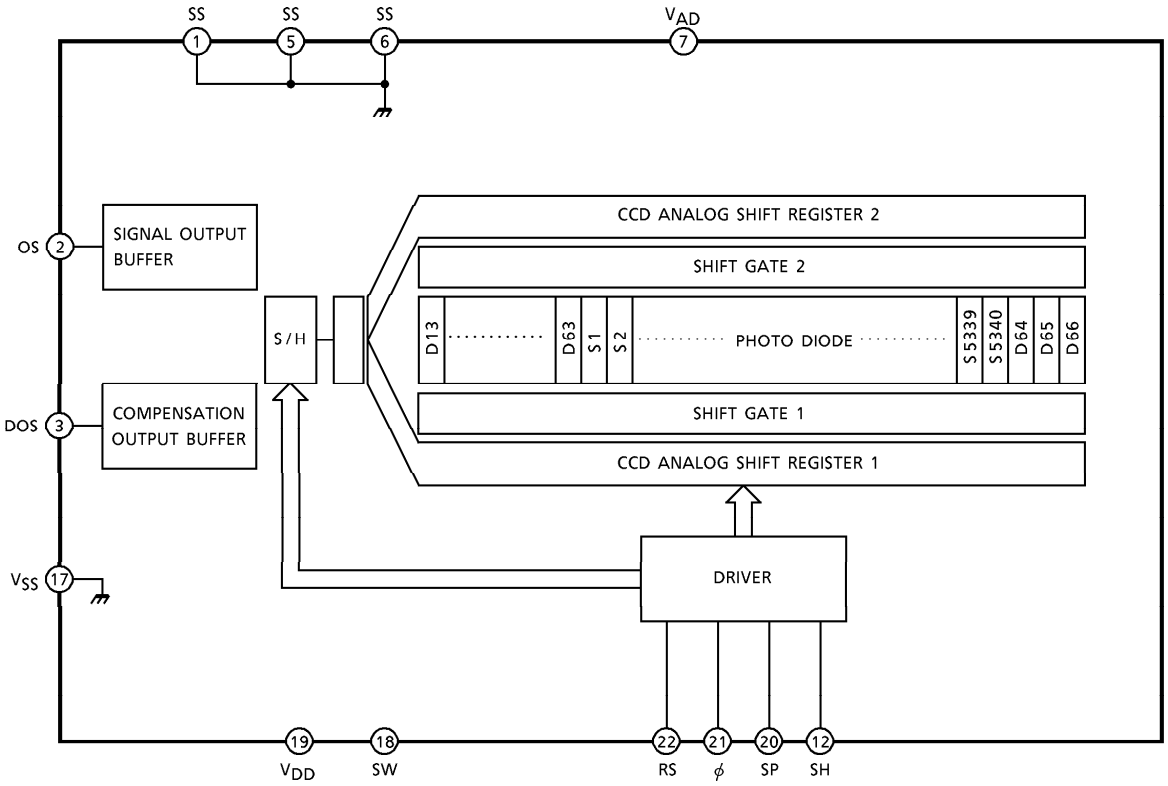
PIN CONNECTIONS



(TOP VIEW)

961001EBA2

CIRCUIT DIAGRAM



PIN NAMES

ϕ	Clock
SH	Shift Gate
RS	Reset Gate
SP	Sample Hold Gate
OS	Signal Output
DOS	Compensation Output
V_{AD}	Power (Analog)
V_{DD}	Power (Driver)
SS	Ground (Analog)
V_{SS}	Ground (Driver)
SW	Final Clock Select Switch
NC	Non Connection

OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{AD} = 12V, V_{DD} = 12V, $V\phi = V_{SH} = V_{RS}$ = 5V (PULSE), $f\phi$ = 0.5MHz, f_{RS} = 1MHz, t_{INT} (INTEGRATION TIME) = 10ms, LIGHT SOURCE = DAYLGIHT FLUORESCENT LAMP)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Sensitivity	R	3.8	4.8	5.8	V / lx·s	
Photo Response Non Uniformity	PRNU	—	—	10	%	(Note 2)
	PRNU (3)	—	3	8	mV	(Note 3)
Register Imbalance	RI	—	—	3	%	(Note 4)
Saturation Output Voltage	V_{SAT}	1.0	1.5	—	V	(Note 5)
Saturation Exposure	SE	0.17	0.3	—	lx·s	(Note 6)
Dark Signal Voltage	V_{DRK}	—	—	2	mV	(Note 7)
Dark Signal Non Uniformity	DSNU	—	—	3	mV	(Note 7)
Analog Current Dissipation	I_{AD}	—	—	20	mA	
Driver Current Dissipation	I_{DD}	—	—	10	mA	
Total Transfer Efficiency	TTE	92	—	—	%	
Output Impedance	Z_O	—	0.5	1	kΩ	
Dynamic Range	DR	—	1500	—		(Note 8)
DC Signal Output Voltage	V_{OS}	3.5	4.5	6.0	V	(Note 9)
DC Compensation Output Voltage	V_{DOS}	3.5	4.5	6.0	V	(Note 9)
DC Mismatch Voltage	$\lvert V_{OS}-V_{DOS}\rvert$	—	—	100	mV	

(Note 2) Measured at 50% of SE (Typ.)

Definition of PRNU : $PRNU = \frac{\Delta\chi}{\overline{\chi}} \times 100\,(\%)$

Where $\overline{\chi}$ is average of total signal outputs and $\Delta\chi$ is the maximum deviation from $\overline{\chi}$ under uniform illumination.

(Note 3) PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (Typ.)

(Note 4) Measured at 50% of SE (Typ.)
RI is defined as follows:

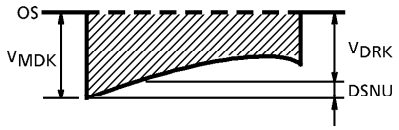
$$RI = \frac{\sum_{n=1}^{5339} \lvert \chi n - \chi n+1 \rvert}{5339 \times \overline{\chi}} \times 100\,(\%)$$

Where χn and $\chi n+1$ are signal outputs of each pixel. $\overline{\chi}$ is average of total signal outputs.

(Note 5) V_{SAT} is defined as minimum saturation output voltage of all effective pixels.

(Note 6) Definition of SE : $SE = \frac{V_{SAT}}{R}$ (lx·s)

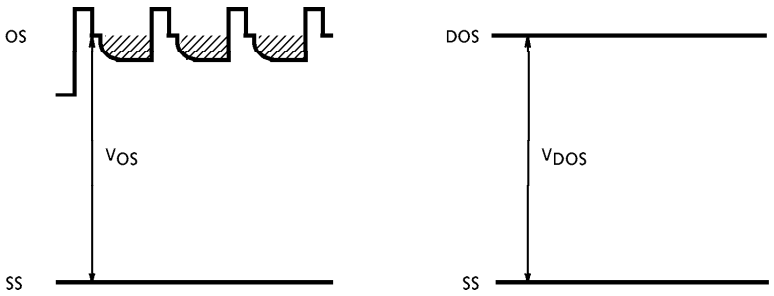
(Note 7) V_{DRK} is defined as average dark signal voltage of all effective pixels.
DSNU is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.



(Note 8) Definition of DR : $DR = \frac{V_{SAT}}{V_{DRK}}$

V_{DRK} is proportional to t_{INT} (Integration Time).
So the shorter t_{INT} condition makes wider DR value.

(Note 9) DC signal output voltage and DC compensation output voltage are defined as follows:



OPERATING CONDITION

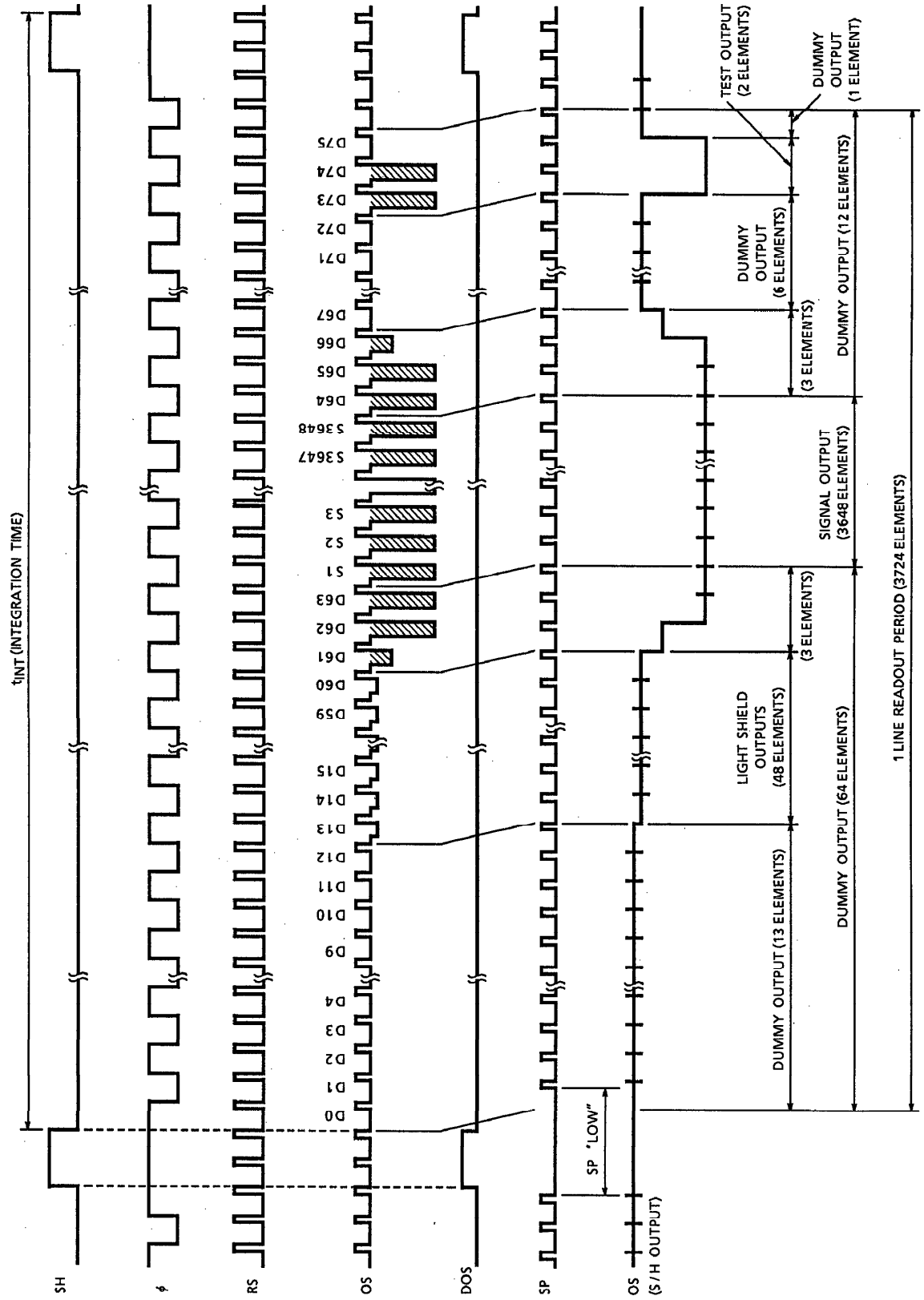
CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Voltage	"H" Level	V_{ϕ}	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Shift Pulse Voltage	"H" Level	V_{SH}	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Reset Pulse Voltage	"H" Level	V_{RS}	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Sample and Hold Pulse Voltage (Note 9)	"H" Level	V_{SP}	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Switch Voltage	"H" Level	V_{SW}	4.5	5.0	5.5	V
	"L" Level		0	—	0.5	
Power Supply Voltage (Analog)		V_{AD}	11.4	12	13	V
Power Supply Voltage ((Driver)		V_{DD}	11	12	13	V

(Note 9) Supply "H" level to SP terminal when sample-and-hold circuitry is not used.

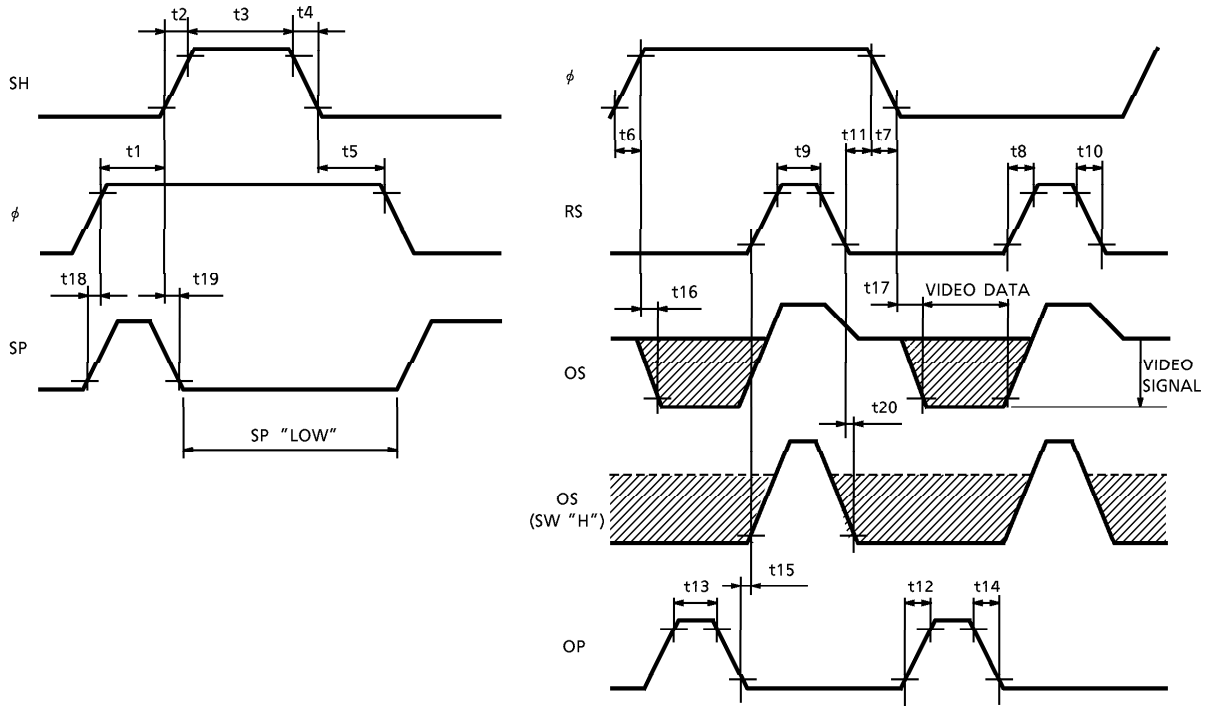
CLOCK CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	f_{ϕ}	—	0.5	4.0	MHz
Reset Pulse Frequency	f_{RS}	—	1	8.0	MHz
Sample and Hold Pulse Frequency	f_{SP}	—	1	8.0	MHz
Clock Capacitance	C_{ϕ}	—	—	10	pF
Final Stage Clock Capacitance	C_{ϕ}	—	—	10	pF
Shift Gate Capacitance	C_{SH}	—	—	10	pF
Sample and Hold Gate Capacitance	C_{SP}	—	—	10	pF
Switch Capacitance	C_{SW}	—	—	10	pF

TIMING CHART



TIMING REQUIREMENTS

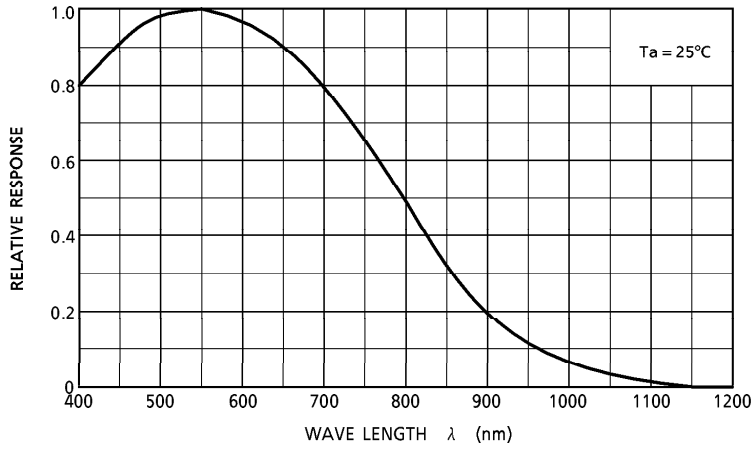


CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 10)	MAX.	UNIT
Pulse Timing of SH and ϕ1	t1, t5	60 (Note 12)	1000	—	ns
SH Pulse Rise Time, Fall Time	t2, t4	0	50	—	ns
SH Pulse Width	t3	500	1000	—	ns
ϕ Rise Time, Fall Time	t6, t7	0	50	—	ns
RS Rise Time, Fall Time	t8, t10	0	20	—	ns
RS Pulse Width	t9	20	250	—	ns
Pulse Timing of ϕ and RS	t11	0	100	—	ns
SP Rise Time, Fall Time	t12, t14	10	100	—	ns
SP Pulse Width	t13	20	100	—	ns
Pulse Timing of SP and RS	t15	0	50	—	ns
Video Data Delay Time (Note 11)	t16, t17	—	75	90	ns
	t20	—	65	75	ns
Pulse Timing of ϕ and SP	t18	0	250	—	ns
Pulse Timing of SH and SP	t19	20	250	—	ns

(Note 10) TYP. is the case of f_{RS} = 1MHz.
(Note 11) Load Resistance is 100kΩ.
(Note 12) MIN. is 0ns, when DOS is not used.

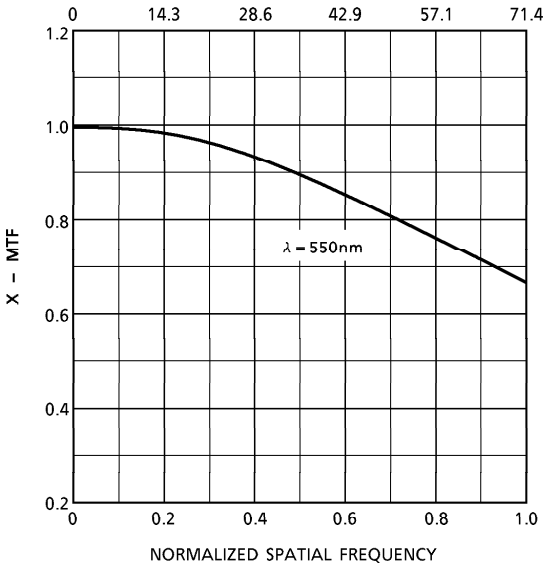
TYPICAL PERFORMANCE CURVES

SPECTRAL RESPONSE



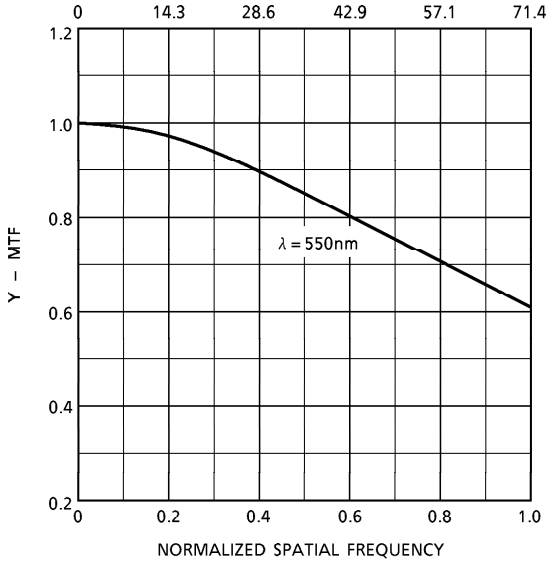
MODULATION TRANSFER FUNCTION
OF X-DIRECTION

SPATIAL FREQUENCY (Cycles / mm)



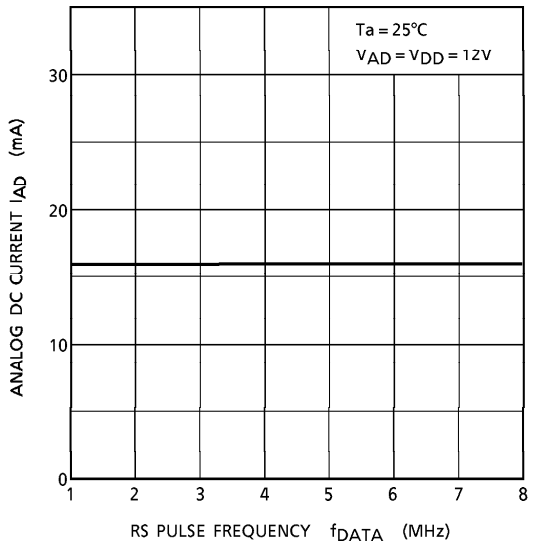
MODULATION TRANSFER FUNCTION
OF Y-DIRECTION

SPATIAL FREQUENCY (Cycles / mm)

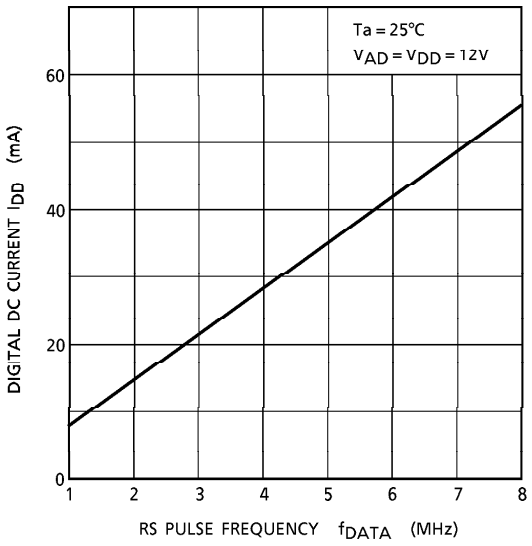


TYPICAL PERFORMANCE CURVES (Cont'd)

RS PULSE FREQUENCY – ANALOG DC CURRENT

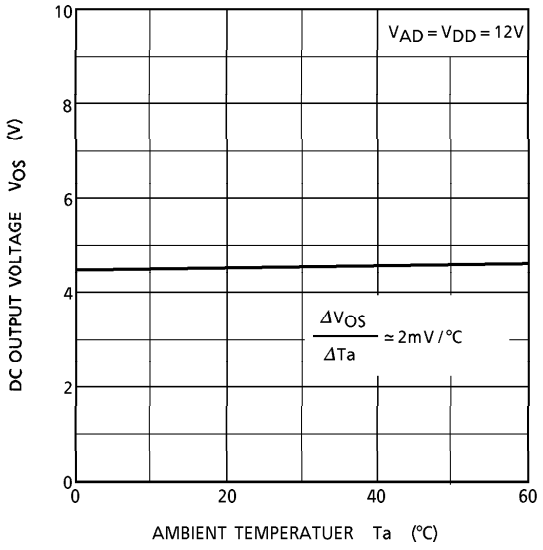


RS PULSE FREQUENCY – DIGITAL DC CURRENT

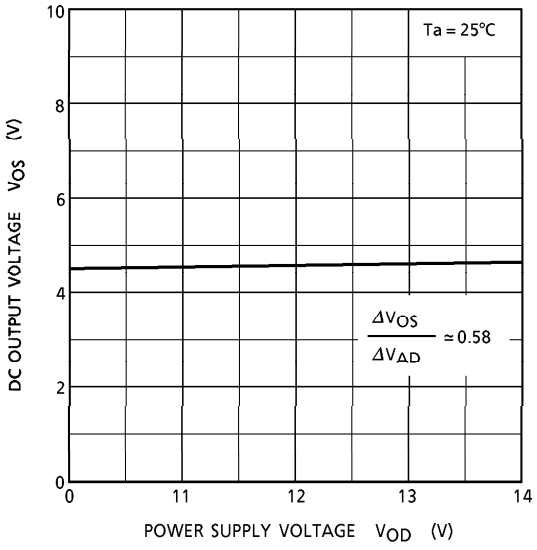


TYPICAL PERFORMANCE CURVES (Cont'd)

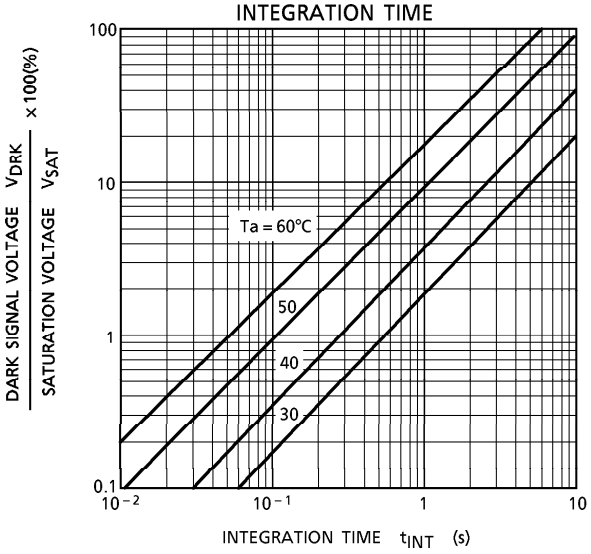
DC OUTPUT VOLTAGE – AMBIENT TEMPERATUER



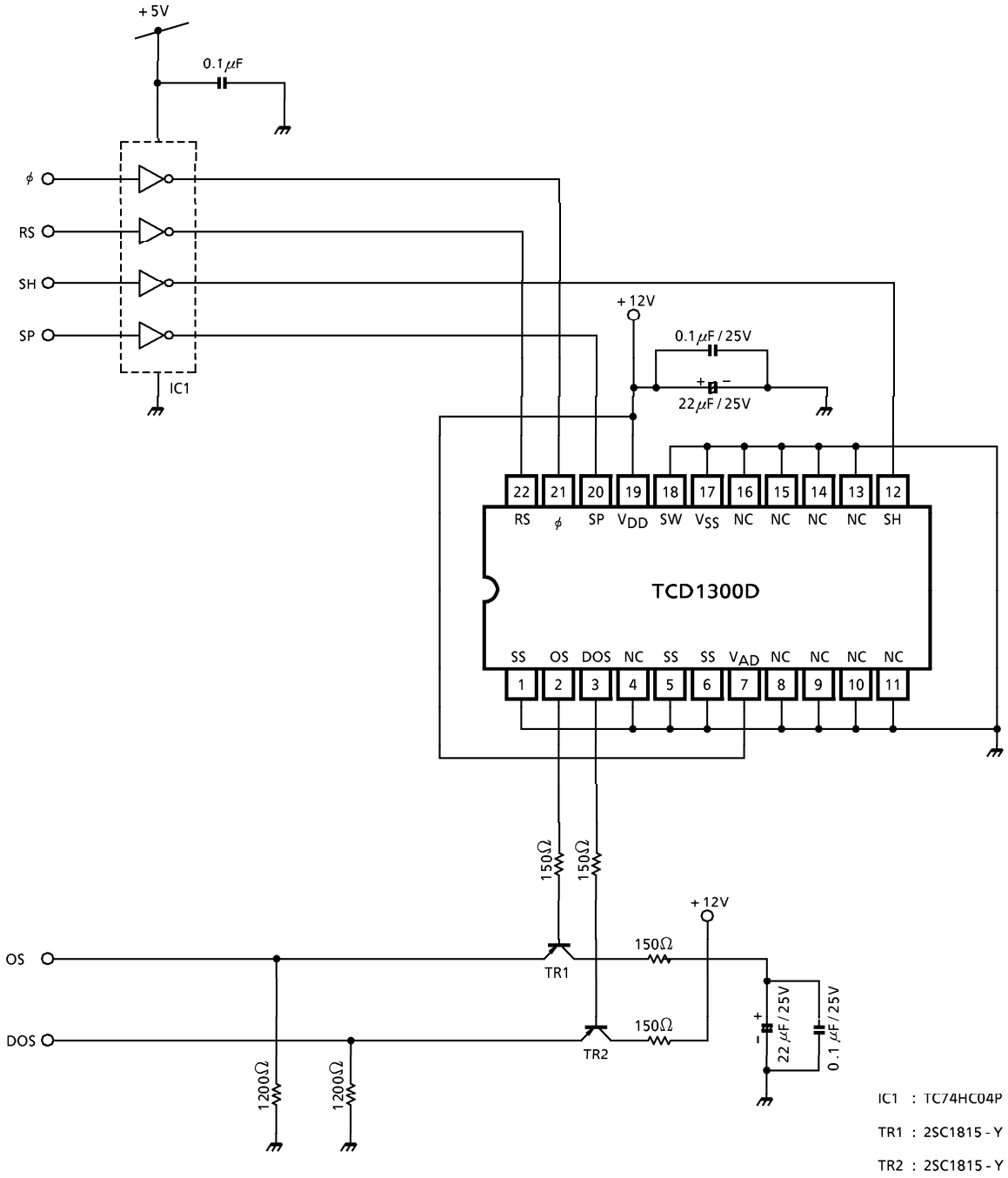
DC OUTPUT VOLTAGE – POWER SUPPLY VOLTAGE



DARK SIGNAL VOLTAGE – INTEGRATION TIME



TYPICAL DRIVE CIRCUIT



CAUTION

1. Window Glass

   The dust and stain on the glass window of the package degrade optical performance of CCD sensor.
   Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N_2.
   Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

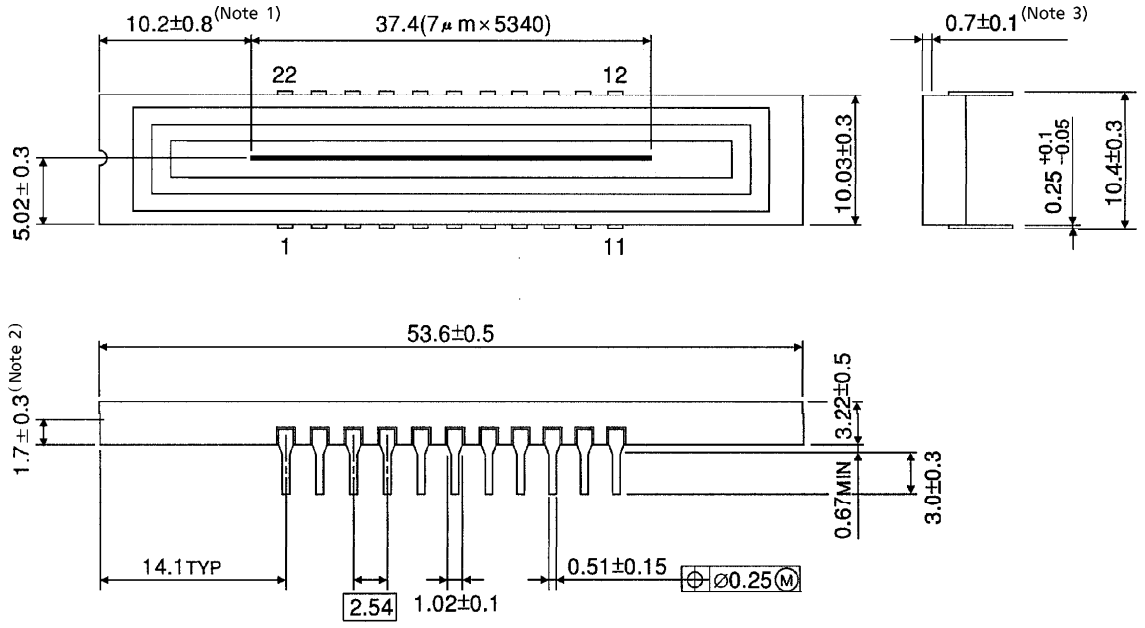
   Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

   CCD sensor is sensitive to infrared light.
   Note that infrared light component degrades resolution and PRNU of CCD sensor.

OUTLINE DRAWING

WDIP22-C-400-2.54B (C) Unit : mm



(Note 1) No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.
(Note 2) TOP OF CHIP TO BOTTOM OF PACKAGE.
(Note 3) GLASS THICKNES (n = 1.5)

Weight : 5.4g (Typ.)