TOSHIBA TB62716F

TENTATIVE

TOSHIBA BI-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62716F

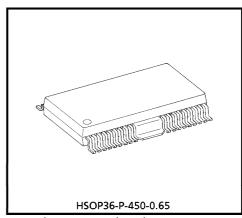
16 BIT SHIFT REGISTER, LATCHES & CONSTANT CURRENT DRIVERS

The TB62716F is specifically designed for LED and LED DISPLAY constant current drivers.

This constant current output circuits is able to set up external resistor ($I_{OUT} = 5 \sim 150 \text{ mA}$).

This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.

The devices consist of 16 bit shift register, latch, AND-GATE and Constant Current Drivers.



Weight: 1.22 g (Typ.)

FEATURES

 Constant Current Output : Can set up all output current with one resister for 5 to 150 mA.

Constant Output Current Matching :

		•				
HIGH/L	/LOW OUTPUT-GND VOLTAGE		CURRENT MATCHING (BIT)	CURRENT MATCHING (LOT)	OUTPUT CURRENT (MAX.)	
"L"		≧ 0.7 V	± 6.0%	± 15.0%	2~70 mA	
"H"		≥ 1.0 V	± 6.0%	± 15.0%	50~150 mA	

- Maximum Clock Frequency : f_{CLK} = 15 MHz (Cascade Connected Operate, T_{opr} = 25°C)
- 5 V C-MOS Compatible Input
- Package: HSOP36-P-375-0.80~0.8mmPitch~

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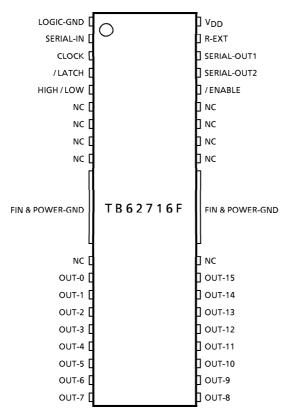
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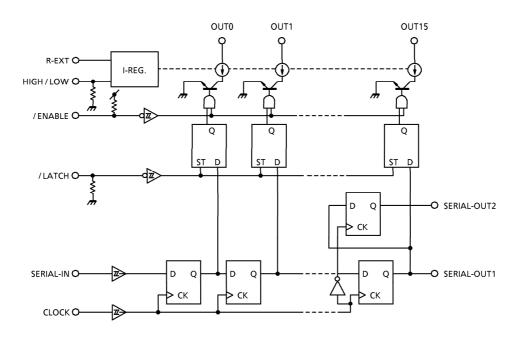
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PIN CONNECTION (Top view)



BLOCK DIAGRAM



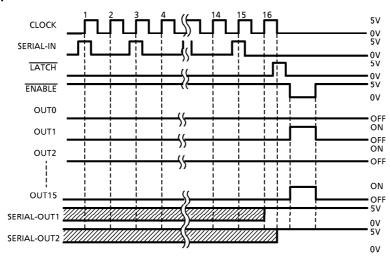
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CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0 ··· OUT5 ··· OUT7	SERIAL-OUT
UP	Н	L	D _n	D _n D _{n-7} D _{n-15}	D _{n-15}
UP	L	L	D _n + 1	No Change	D _{n-14}
UP	Н	L	D _n + 2	D _n + 2 ··· D _{n-5} ··· D _{n-13}	D _{n-13}
DOWN	Х	L	D _n + 3	D _n + 2 ··· D _{n-5} ··· D _{n-13}	D _{n-13}
DOWN	Х	Н	D _n + 3	Off	D _{n-13}

(Note) OUT0 \sim 15 = on in case of D_n = H level and OUT0 \sim 15 = off in case of D_n = L level.

A resistor is connected with R-EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

TIMING DIAGRAM



(Note) Latches are level sensitive, not rising edge sensitive and not syncronus CLOCK. Input of LATCH-terminal to H level, data passes latches, and input to L level, data hold latches.

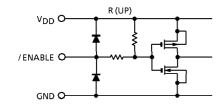
Input of ENABLE-terminal to H level, all output (OUT0~15) do off.

TERMINAL DISCRIPTION

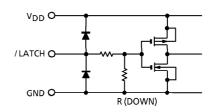
PIN No.	PIN NAME	FUNCTION
5	HIGH / LOW	It is the terminal which does switching for the big current/low current.
FIN	POWER-GND	GND terminal for current output.
1	LOGIC-GND	GND terminal for control logic.
2	SERIAL-IN	Input terminal of a serial-data shift-register.
3	CLOCK	Input terminal of a clock for data shift to up-edge.
4	/ LATCH	Input terminal of a data strobe. Latches passes data with "H" level input of LATCH-terminal, and hold data with "L" level input.
11~18 19~26	OUT0~15	Output terminals.
32	/ ENABLE	Input terminal of output enable. All outputs (OUT0~7) do off with "H" level input of ENABLE-termnal, and do on with "L" level input.
34	SERIAL-OUT	Output terminal of a serial-data for next SERIAL-IN terminal.
35	R-EXT	Input terminal of connects with a resister for to set up all output current.
36	V_{DD}	5 V Supply voltage terminal.

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

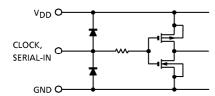
1. ENABLE terminal



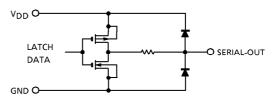
2. LATCH terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT	
Supply Voltage	V_{DD}	0~7.0	V	
Input Voltage	VIN	-0.4~V _{DD} + 0.4	V	
Output Compant	Laure	+ 150 (HIGH / LOW = "H")	A /l.	
Output Current	IOUT	+ 70 (HIGH / LOW = "L")	mA / ch	
Output Voltage	Vout	- 0.5~17.0	V	
Clock Frequency	fCLK	15	MHz	
GND Terminal Current	IGND	1200	mA	
Bayyar Dissination	P _{D1}	1.08 (FREE AIR, Ta = 25°C)	w	
Power Dissipation	P _{D2}	1.92 (ON PCB, Ta = 25°C)] vv	
Thermal Resistance	R _{th} (j-a)	120 (Free Air) / 65 (On PCB)	°C/W	
Thermal Resistance	R _{th} (j-c)	12		
Operating Temperature	T _{opr}	- 40∼ + 85	°C	
Storage Temperature	T _{stg}	− 55~ + 150	°C	

(Note) Ambient temperature delated above 25°C in the proportion of 15.4 mW/°C (On PCB)

RECOMMENDED OPERATING CONDITION (Ta = 25°C unless otherwise noted)

CHARACTERISTIC	CHARACTERISTIC SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	_	4.5	5.0	5.5	V
Output Voltage	Vout	_	_	_	15.0	V
	lOUT1	DC 1 circuit (HIGH/LOW = "H")	50	_	130	mA mA
Output Current	IOUT2	DC 1 circuit (HIGH / LOW = "L")	2	_	60	
Output Current	ІОН	SERIAL-OUT1, 2	_	_	- 1.0	
	lOL	SERIAL-OUT1, 2	_	_	1.0	ША
	V _{IH}		0.7	l _	V _{DD}	
Input Voltage			V_{DD}		+ 0.3	V
	VIL		- 0.3	—	0.3 V _{DD}	
LATCH Pulse Width	t _W /LATCH		100	_	_	ns
CLOCK Pulse Width	t _W CLOCK	V _{DD} = 4.5~5.5 V	50	_		
ENABLE Pulse Width	t _W /ENABLE		1000	_		
Set-up Time for DATA	t _{setup} (D)	1		_	_	
Hold Time for DATA	thold (D)		20	_	_	
Set-up Time for LATCH	t _{setup} (L)	1		_	_	
Hold Time for ENABLE thol			60	_	_	
Clock Frequency	fCLK	Cascade operation	10.0		_	MHz
Power Dissipation	PD	Ta = 85°C (FN-type On PCB)			1.00	W

ELECTRICAL CHARACTERISTICS (Ta = 25°C unless otherwise noted)

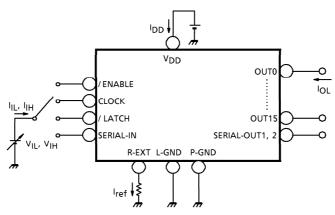
СНАР	RACTERISTIC	SYMBOL	TEST CIR- CUIT	COI	NDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" level	V _{IH}			0.7 V _{DD}	-	V _{DD}	\ \	
	"L" level	V _{IL}			_	GND	_	0.3 V _{DD}	
Output L	eakage Current	ОН		V _{OH} = 15.0 V				10	μ A
Output	SERIAL	V_{OL}		$I_{OL} = +1.0 \text{ mA}$				0.4	\ \
Voltage	-OUT1, 2	V _{OH}		$I_{OH} = -1.0 \text{ mA}$		4.6		_	\ \ \
Output C	urrent 1	l _{OL1}] - - 1	VOUT = 0.7 V	$R_{EXT} = 520 \Omega$,	34.3	40.3	46.8	mA
	Current Skew	⊿l _{OL1}			HIGH / LOW = "L"		± 1.5	± 6.0	%
Output C	urrent 2	l _{OL2}		Vou= - 10V	$R_{EXT} = 160 \Omega$,	107.1	126.0	144.9	mA
Current Skew		⊿l _{OL2}		VOUT = 1.0 V	HIGH/LOW = "H"	_	± 1.5	± 6.0	%
	Supply Voltage Regulation			Ta = −40~85	°C	_	1.5	5.0	% / V
Pull-up R	esistor	R _{IN} (up)			_	100	200	400	kΩ
Pull-dow	n Resistor	R _{IN} (down)		_		100	200	400	kΩ
		IDD (off) 1		R _{EXT} = OPEN, OUT0~8 = off		_	1.0	2.0	
Cupply	"OFF"	IDD (off) 2		$R_{EXT} = 500 \Omega$, OUT0~8 = off		7.0	12.0	16.0	
Supply Current		IDD (off) 3		$R_{EXT} = 160 \Omega$, OUT0~8 = off		13.0	20.0	30.0	mA
Current	"ON"	IDD (on) 1		$R_{EXT} = 500 \Omega$	_	23.1	40.5		
	ON	IDD (on) 2		$R_{EXT} = 160 \Omega$	_	33.0	62.1		

SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

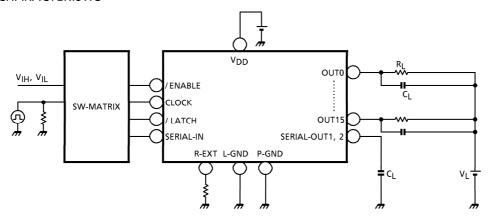
CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT
Duna a matica	CLK-OUTn				_	500	1000	ns
Propagation	LATCH-OUTn	.			_	500	1000	
Delay Time ("L" to "H")	ENABLE-OUTn	^t pLH	-		_	500	1000	ns
(CLK-SOUT			$V_{DD} = 5.0 V$	_	30	70	
Dunanakina	SIN-OUTn			V _{CE} = 1.0 V	_	500	1000	ns
Propagation	LATCH-OUTn	^t pHL		$\begin{aligned} &\text{V}_{IH} = \text{V}_{DD} \\ &\text{V}_{IL} = \text{GND} \\ &\text{R}_{EXT} = 160 \ \Omega, \\ &\text{I}_{OUT} = 126 \ \text{mA}, \\ &\text{V}_{L} = 3.0 \ \text{V} \\ &\text{R}_{L} = 32 \ \Omega \\ &\text{C}_{L} = 10.5 \ \text{pF} \\ &\text{tor} : \ 10\% \ \text{to} \ 90\% \end{aligned}$	_	500	1000	
Delay Time ("H" to "L")	ENABLE-OUTn				_	500	1000	
(CLK-SOUT				_	30	70	
Pulse Width	CLK	tw CLK, CLK	_		_	20	30	ns
Pulse Width	LATCH	t _{w LAT} , LAT	_		_	10	25	ns
Set-up Time	L-H	^t setupLAT			_	25	50	ns
for LATCH/SIN	H-L	/SIN	-		_	25	50	ns
Hold Time	L-H	^t hold		tof : 90% to 10%	_	0	15	ns
for LATCH/SIN	H-L	LAT/SIN	_	t _{pLH} : 50% to 10%	_	0	15	ns
Maximum CLOCK Rise Time		t _r	_	t _{pHL} : 50% to 90%	_	_	10	
Maximum CLOCK Fall Time		t _f	_		_	_	10	μ s
Output Rise Time		tor	_		300	600	1000	ns
Output Fall Time	9	t _{of}	_		300	600	1000	113

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TEST CIRCUIT DC CHARACTERISTIC



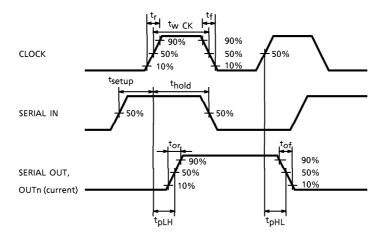
AC CHARACTERISTIC



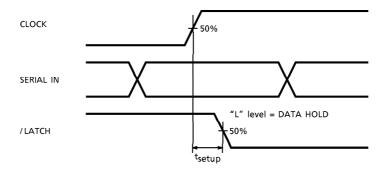
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TIMING WAVEFORM

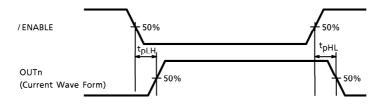
1. CLOCK-SERIAL OUT, OUTn

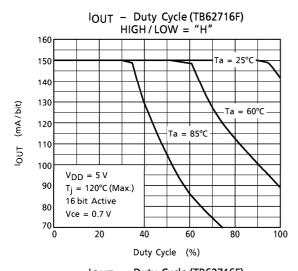


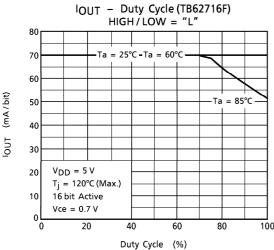
2. CLOCK-/LATCH

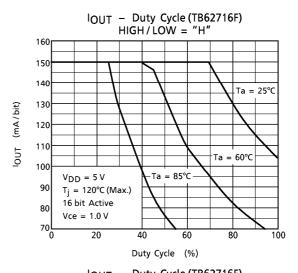


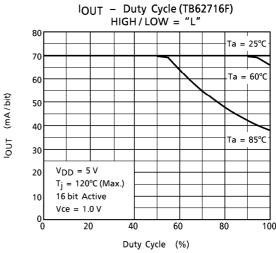
3. ENABLE-OUTn

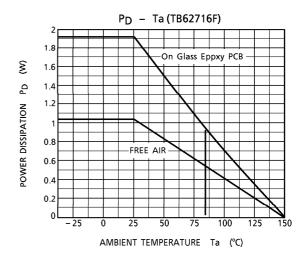




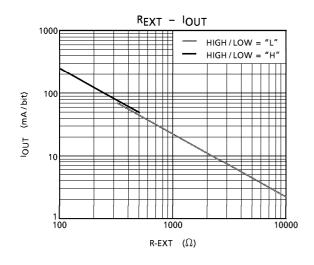


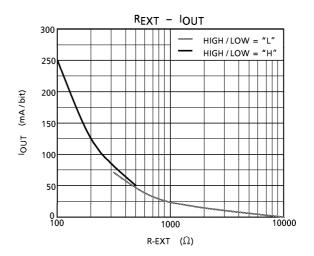






LED DRIVER TB6270X SERIES APPLICATION NOTE





Total supply voltage (V_{LED})

This device can operate 0.7~1.0 V (VO).

When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to power dissipation.

In order to minimize power dissipation and loss, we would like to recommend to set the total supply voltage as shown below,

 V_{LED} (total supply voltage) = V_{CE} ($T_r V_{sat}$) + V_f (LED Forward voltage) + V_O (I_C supply voltage)

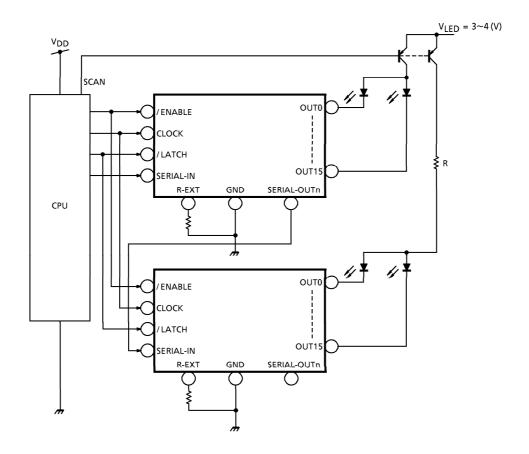
When the total supply is too high considering the power dissipation of this device, an additional R can decrease the supply voltage.

Pattern Layout

This device owns only one ground pin that means signal ground pin and power ground pin are common.

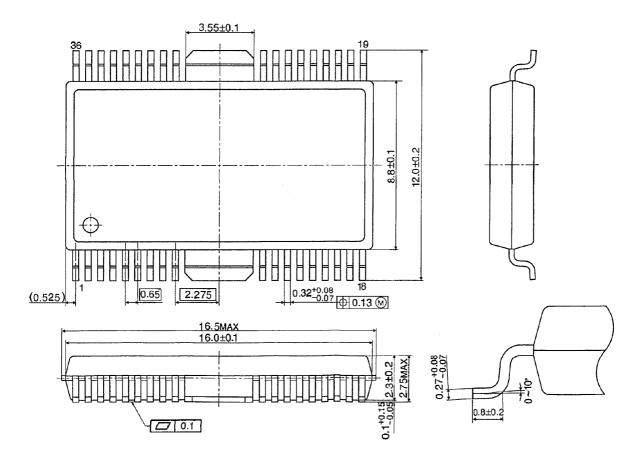
If ground pattern layout contains large inductance and impedance, and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5 V by switching noise in operation, this device may miss-operate.

So we would like you to pay attention pattern layout to minimize inductance.



OUTLINE DRAWING

HSOP36-P-450-0.65 Unit: mm



Weight: 1.22 g (Typ.)