TOSHIBA TB62715FN

TENTATIVE

TOSHIBA BI-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62715FN

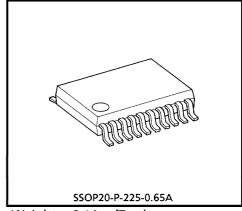
8 BIT SHIFT REGISTER, LATCHES & CONSTANT CURRENT DRIVERS

The TB62715FN is specifically designed for LED and LED DISPLAY constant current drivers.

This constant current output circuits is able to set up external resistor ($I_{OUT} = 70 \sim 150 \text{ mA}$).

This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.

The devices consist of 8 bit shift register, latch, AND-GATE & Constant Current Drivers.



Weight: 0.14 g (Typ.)

FEATURES

 Constant Current Output: Can set up all output current with one resistor for 80 to 150 mA.

Constant Output Current Matching :

HIGH / LOW	OUTPUT-GND VOLTAGE	CURRENT MATCHING (BIT)	CURRENT MATCHING (LOT)	OUTPUT CURRENT (MAX.)
"L"	≧ 0.7 V	± 6.0%	± 15.0%	2~70 mA
"H"	≧ 1.0 V	± 6.0%	± 15.0%	50~150 mA

Maximum Clock Frequency : f_{CLK} = 15 MHz

(Cascade Connected Operate, Topr = 25°C)

5 V C-MOS Compatible Input

Package: SSOP20-P-225-0.65A

980910EBA1

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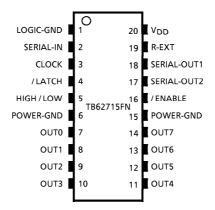
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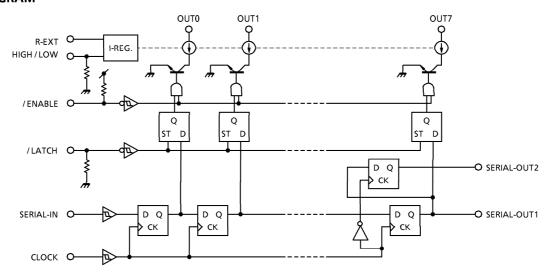
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PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM

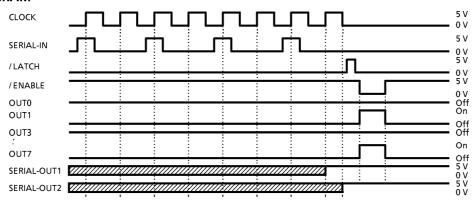


TRUTH TABLE

CLOCK	/LATCH	/ ENABLE	SERIAL-IN	OUT0 ··· OUT5 ··· OUT7	SERIAL-OUT
UP	Н	L	D _n	D _n D _{n - 5} D _{n - 7}	D _{n - 7}
UP	L	L	D _{n + 1}	No Change	D _{n - 6}
UP	Н	L	D _{n + 2}	$D_{n+2} \cdots D_{n-3} \cdots D_{n-5}$	D _{n - 5}
DOWN	Х	L	D _{n + 3}	$D_{n+2} \cdots D_{n-3} \cdots D_{n-5}$	D _{n - 5}
DOWN	Х	Н	D _{n + 3}	Off	D _{n - 5}

(Note) OUT0 \sim OUT7 = on in case of D_n = H level and OUT0 \sim 7 = off in case of D_n = level. A resistor is connected with R-EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

TIMING DIAGRAM



(Note) Latches are level sensitive, not rising edge sensitive and not syncronus CLOCK.

Input of LATCH-terminal to H Level, data passes latches, and input to L level, data hold latches.

Input of ENABLE-terminal to H level, all output (OUT0~7) do off.

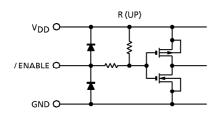
TERMINAL DISCRIPTION

PIN No.	PIN NAME	FUNCTION
5	HIGH / LOW	It is the terminal which does switching for the big current/low current.
6, 15	POWER-GND	GND terminal for current output.
1	LOGIC-GND	GND terminal for control logic.
2	SERIAL-IN	Input terminal of a serial-data for shift-register.
3	CLOCK	Input terminal of a clock for data shift to up-edge.
4	/ LATCH	Input terminal of a data strobe. Latches passes data with "H" level input of LATCH-terminal, and hold data with "L" level input.
7~10, 11~14	OUT0~7	Output terminals.
16	/ ENABLE	Input terminal of output enable. All outputs (OUT0~7) do off with "H" level input of ENABLE-terminal, and do on with "L" level input.
18	SERIAL-OUT1	シリアルデータの出力端子です。
17	SERIAL-OUT2	Output terminal of a serial-data for next SERIAL-IN terminal.
19	R-EXT	Input terminal of connects with a resister for to set up all output current.
20	V_{DD}	5 V Supply voltage terminal.

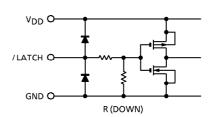
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EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

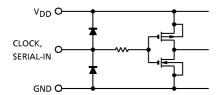
1. / ENABLE terminal



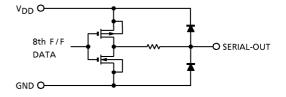
2. / LATCH terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT		
Supply Voltage	V_{DD}	0~ + 7.0	V		
Input Voltage	VIN	-0.4~V _{DD} + 0.4	V		
Output Current	1	+ 150 (HIGH/LOW = "H")	A / -l-		
Output Current	IOUT	+70 (HIGH/LOW = "L")	mA / ch		
Output Voltage	Vout	-0.5~ + 17.0	V		
Clock Frequency	fCLK	15	MHz		
GND Terminal Current	I _{GND}	1200	mA		
Bower Dissination	P _{D1}	FN-type : 0.71 (FREE AIR, Ta = 25° C)	۱۸/		
Power Dissipation	P _{D2}	FN-type : 0.96 (ON PCB, Ta = 25°C)	- W		
The march Desisters of	R _{th} (j-a) 1	175 (FREE AIR)	°C /\A/		
Thermal Resistance	Rth (j-a) 2	130 (ON PCB)	°C/W		
Operating Temperature	T _{opr}	-40∼+85	°C		
Storage Temperature	T _{stg}	- 55∼ + 150	°C		

(Note) FN type : Ambient temperature delated above 25°C in the proportion of 7.69 mW/°C Condition = On PCB ($50 \times 50 \times 1.6$ mm Cu = 40%)

RECOMMENDED OPERATING CONDITION (Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply Voltage	$V_{ m DD}$		4.5	5.0	5.5	V	
Output Voltage	VOUT		_	_	15.0	V	
Output Current	lOUT1	DC 1 circuit (HIGH/LOW = "H")	50	_	130	m A / sh	
	^I OUT2	DC 1 circuit (HIGH/LOW = "L")	2 _ 60		60	mA / ch	
	IOH	SERIAL-OUT1, 2	_	_	- 1.0	mA	
	lol	SERIAL-OUT1, 2	_	1	1.0	IIIA	
land Valtage	V_{IH}		0.7V _{DD}		V _{DD} + 0.3	V	
Input Voltage	V_{IL}		- 0.3	_	0.3V _{DD}		
LATCH Pulse Width	tw LAT		100	_	_	ns	
CLOCK Pulse Width	^t w CLK		50	_	_	ns	
ENABLE Pulse Width	^t w EN	V _{DD} = 4.5~5.5 V	1000	_	_	ns	
Set-up Time for DATA	t _{setup} (D)		60	_	_	ns	
Hold Time for DATA	^t hold (D)		20	_	_	ns	
Set-up Time for LATCH	t _{setup (L)}		100	_	_	ns	
Hold Time for ENABLE	^t hold (L)		60	_	_	ns	
Clock Frequency	fCLK	V _{DD} = 4.5~5.5 V, Cascade Operation	10.0	_	_	MHz	
Power Dissipation	P_{D}	Ta = 85°C (FN-type On PCB)	_	_	0.50	W	

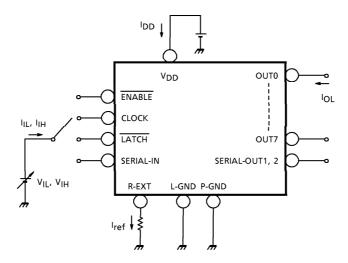
ELECTRICAL CHARACTERISTICS (Ta = 25°C unless otherwise noted)

CHARA	CTERISTIC	SYMBOL	TEST CIR- CUIT	CONDITION		MIN.	TYP.	MAX.	UNIT	
Input	"H" Level	V_{IH}	1	_		0.7V _{DD}		V_{DD}	V	
Voltage	"L" Level	V_{IL}	1		GND	_	0.3V _{DD}	V		
Output l Current	-eakage	Іон	1	V _{OH} = 15.0 V		_	_	10	μ A	
Output	SERIAL	Voн	1	$I_{OH} = -1.0 \text{ m}$	nA	_	_	0.4	V	
Voltage	-OUT1, 2	VOL	1	$I_{OL} = + 1.0 \text{ m}$	A	4.6	_	_	V	
Output (Current 1	lOL1	1	V _{CE} = 0.7 V	$R_{EXT} = 520 \Omega$,	31.7	37.5	43.1	mA	
		dl _{OL1}] '	VCE = 0.7 V	HIGH/LOW = "L"	_	± 1.5	± 6.0	%	
Output Current 2		lOL2	1	V _{CE} = 1.0 V	$R_{EXT} = 160 \Omega$,	104.0	123.0	141.4	mA	
1		dl _{OL2}] '	vCF = 1.0 v	HIGH/LOW = "H"	_	± 1.5	± 6.0	%	
	Supply Voltage Regulation % / \		1	Ta = −40~ +85°C		_	+ 1.5	+ 5.0	% / V	
Pull-up F	Resistor	R _{IN (up)}	1			100	200	400	kO.	
Pull-dow	n Resistor	RIN (down)	ı			100	200	400	$\mathbf{k}Ω$	
		IDD (off) 1		R _{EXT} = OPEN	_	1.0	2.0			
Cupply	"OFF"	IDD (off) 2		$R_{EXT} = 260 \Omega$	_	10.0	15.0			
Supply Current		IDD (off) 3	1	$R_{EXT} = 160 \Omega$	$OUT0\sim7 = off$	_	16.0	21.0	mA	
Current	"ON"	I _{DD} (on) 1		$R_{EXT} = 260 \Omega$	OUT0~7 = on		23.1	40.5		
ON		I _{DD} (on) 2		$R_{EXT} = 160 \Omega$	$OUT0\sim7 = on$		33.0	62.1		

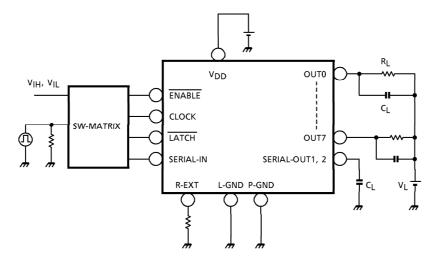
SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR- CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT
D	SIN-OUTn		2		_	500	1000	
Propagation	LATCH-OUTn	.			_	500	1000	ns
Delay Time ("L" To "H")	ENABLE-OUTn	t _{pLH}	~		_	500	1000	
(L 10 H)	CLK-SOUTn				_	30	70	
Duamanatian	SIN-OUTn			$V_{DD} = 5.0 V$	_	500	1000	00 00 ns
Propagation	LATCH-OUTn	4	١,	$V_{CE} = 1.0 \text{ V}$ $V_{IH} = V_{DD}$, $V_{IL} = GND$ $R_{EXT} = 260 \Omega$, $R_{L} = 32 \Omega$	_	500	1000	
Delay Time ("H" To "L")	ENABLE-OUTn	t _{pHL}	2		_	500	1000	
(10 L)	CLK-SOUTn				_	30	70	
Pulse Width	CLK	tw CLK, /CLK tw LAT, /LAT	2		_	20	30	
Puise width	LATCH			I _{OUT} = 125 mA,	_	10	25	ns
Set-Up Time for	L-H	t _{setupLAT}	2	$C_{l} = 10.5 \text{ pF}$	_	25	50	
LATCH / SIN	H-L	& SIN	2	t _{or} : 10% to 90%	_	25	50	ns
Hold Time for	L-H	t _{hold}	2	t _{of} : 90% to 10%	_	0	15	ne
LATCH / SIN	H-L	LAT / SIN	~	t _{pLH} : 50% to 10%	_	0	15	ns
Maximum CLOCK Rise Time		t _r	2	t _{pHL} : 50% to 90%	_	_	10	μ s
Maximum CLOCK Fall Time		t _f	2		_ _	_	10	μs
Output Rise Time		tor	2		300	600	1000	ns
Output Fall Time		t _{of}	2		300	600	1000	ns

TEST CIRCUITDC characteristic



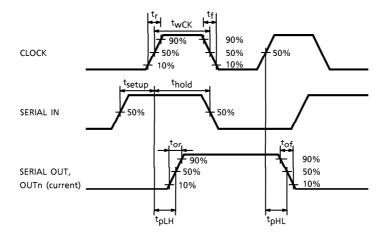
AC characteristic



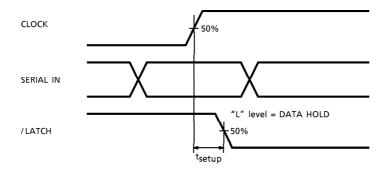
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TIMING WAVEFORM

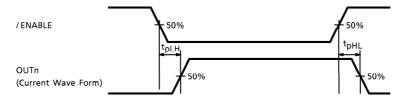
1. CLOCK-SERIAL OUT, OUTn

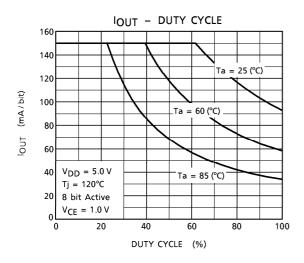


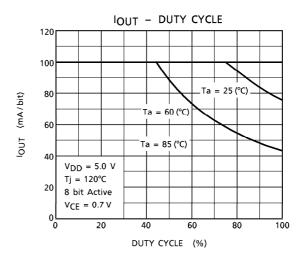
2. CLOCK-/LATCH

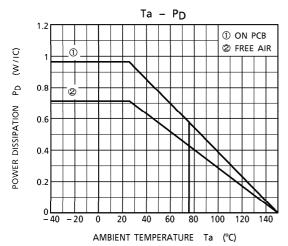


3. / ENABLE-OUTn

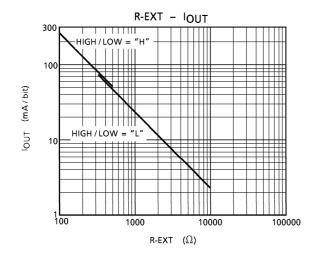


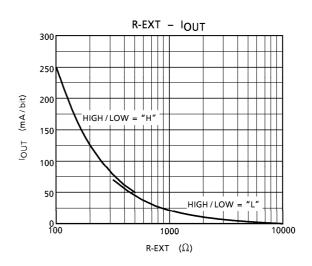






LED DRIVER TB6270X SERIES APPLICATION NOTE





TOTAL SUPPLY VOLTAGE (VLED)

This device can operate 0.7~1.0 V (VO).

When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to power dissipation.

In order to minimize power dissipation and loss, we would like to recommend to set the total supply voltage as shown below,

VLED (total supply voltage) = V_{CE} (Tr V_{sat}) + V_f (LED Forward voltage) + V_O (IC supply voltage)

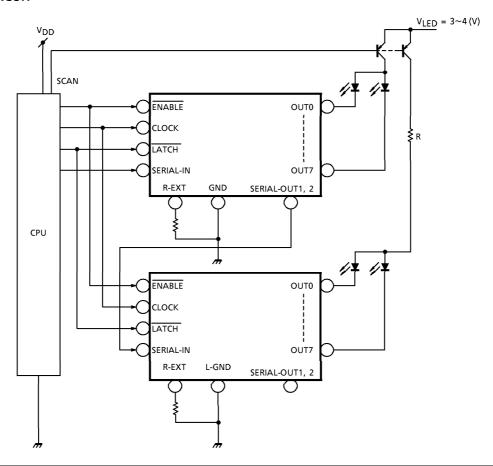
When the total supply is too high considering the power dissipation of this device, an additional R can decrease the supply voltage.

$$R = \frac{V_{LED} - V_{f(LED)} - V_{O}(Min.)}{I_{O}(Max.) \times BIT(Max.)}$$

PATTERN LAYOUT

This device owns only one ground pin that means signal ground pin power ground pin are common. If ground pattern layout contains large inductance and impedance, and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5 V by switching noise in operation, this device may miss-operated. So we would like you to pay attention to pattern layout to minimize inductance.

APPLICATION CIRCUIT

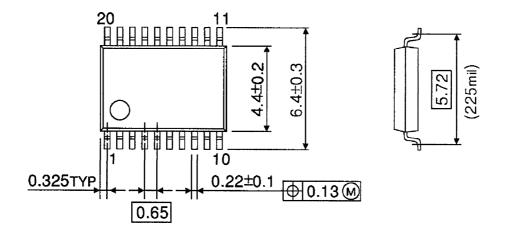


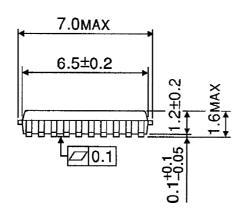
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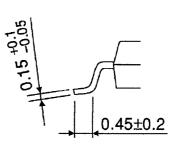
OUTLINE DRAWING

SSOP20-P-225-0.65A

Unit: mm







Weight: 0.14 g (Typ.)