

TENTATIVE

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62710P, TB62710F

8BIT SHIFT REGISTER, LATCHES & CONSTANT CURRENT SOURCE DRIVERS

The TB62710P, TB62710F is specifically designed for LED and LED DISPLAY (Cathode Common) constant current drivers.

This constant current output circuits is able to set up external resistor ($I_{OUT} = 5\sim 90\text{ mA}$).

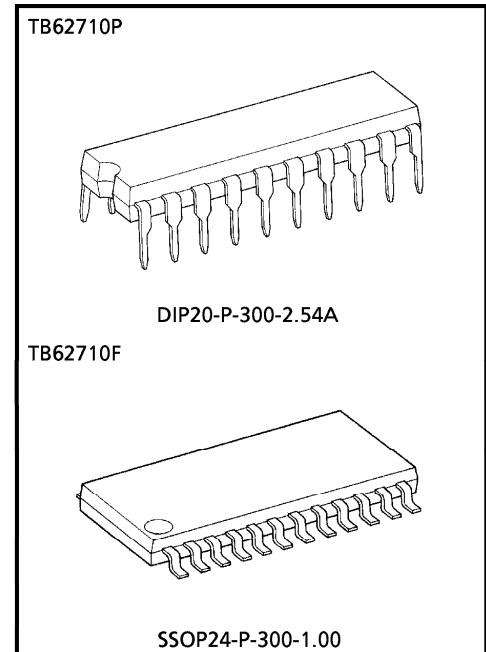
This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.

The devices consist of 8 bit shift register, latch, AND-GATE and Constant Current Drivers.

FEATURES

- Constant Current Output
Can set up all output current with one resistor for -5 to -90 mA .
- Constant Output Current Matching

OUTPUT-GND VOLTAGE	CURRENT MATCHING	OUTPUT CURRENT
$\geq 2.0\text{ V [V]}$	$\pm 6.0\%$	$\sim -50\text{ mA [mA]}$
$\geq 2.0\text{ V [V]}$		$-50\sim -90\text{ mA [mA]}$



Weight
 DIP20-P-300-2.54A : 2.25 g (Typ.)
 SSOP24-P-300-1.00 : 0.32 g (Typ.)

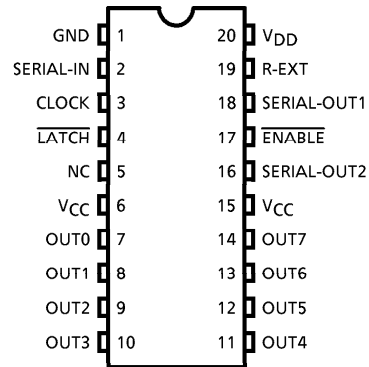
- Maximum Clock Frequency : $f_{CLK} = 15\text{ [MHz]}$ (Cascade Connected Operate, $T_{opr} = 25^\circ\text{C}$)
- 5 V CMOS Compatible Input
- Package : DIP20-P-300 (TB62710P)
SSOP24-P-300 (TB62710F)

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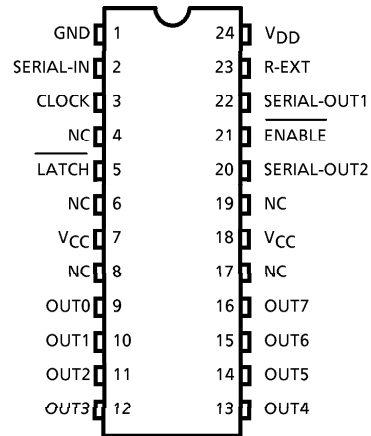
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PIN CONNECTION (Top view)

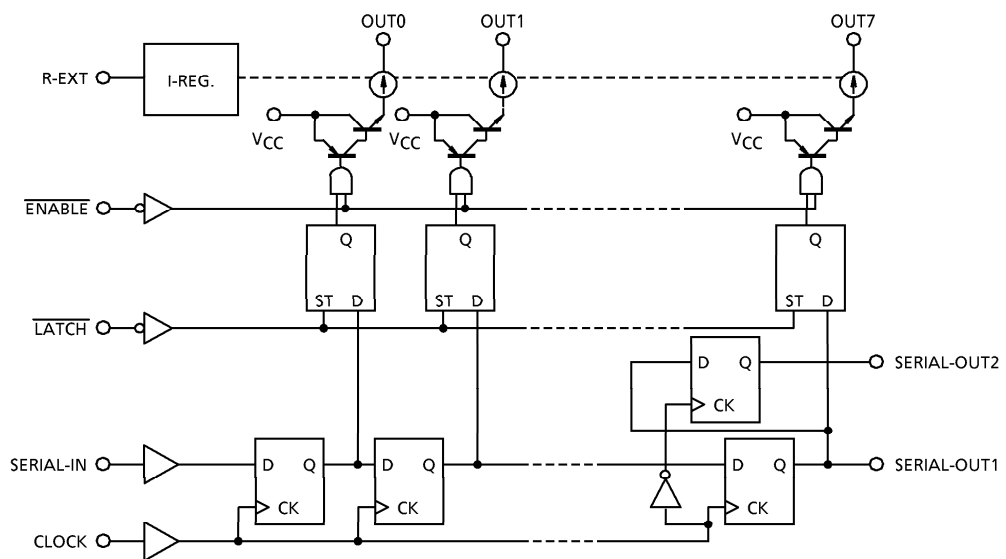
TB62710P



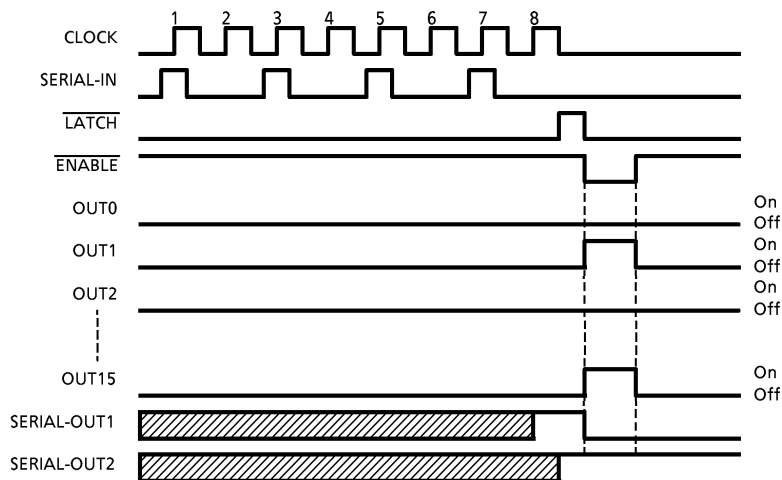
TB62710F



BLOCK DIAGRAM



TIMING DIAGRAM



(Note) : Latches are level sensitive, not rising edge sensitive and not synchronous CLOCK.
 Input of $\overline{\text{LATCH}}$ -terminal to "H" level, data passes latches, and input to "L" level, data hold latches.
 Input of $\overline{\text{ENABLE}}$ -terminal to "H" level, all output (OUT0~7) do off.

TERMINAL DESCRIPTION

PIN No.		PIN NAME	FUNCTION
P-type	F-type		
1	1	GND	GND terminal for control logic.
2	2	SERIAL-IN	Input terminal of a serial-data for shift-register.
3	3	CLOCK	Input terminal of a clock for data shift to up-edge.
4	5	$\overline{\text{LATCH}}$	Input terminal of a data strobe. Latches passes data with "H" level input of $\overline{\text{LATCH}}$ -terminal, and hold data with "L" level input.
7~14	19~16	OUT0~7	Output terminals.
17	21	$\overline{\text{ENABLE}}$	Input terminal of output enable. All outputs (OUT0~7) do off with "H" level input of $\overline{\text{ENABLE}}$ -terminal, and do on with "L" level input.
16	20	SERIAL-OUT2	Output terminal of a serial-data for next SERIAL-IN terminal.
18	22	SERIAL-OUT1	Output terminal of a serial-data for next SERIAL-IN terminal.
19	23	R-EXT	Input terminal of connects with a resister for to set up all output current.
20	24	VDD	5 V Supply voltage terminal
6, 15	7, 18	VCC	0~17 V Supply voltage terminal for LED
5	4, 6, 8, 17, 19	NC	NO CONNECTION

TRUTH TABLE

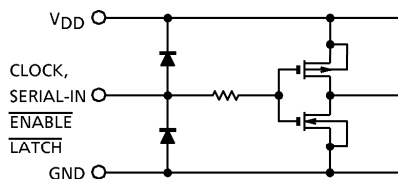
CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL-IN	OUT0 ... OUT3 ... OUT7	SERIAL-OUT1	SERIAL-OUT2
UP	H	L	D_n	$D_n \dots D_{n-3} \dots D_{n-7}$	D_{n-7}	D_{n-8}
DOWN	H	L	D_n	$D_n \dots D_{n-3} \dots D_{n-7}$	No change	D_{n-7}
UP	L	L	D_{n+1}	No change (data hold)	D_{n-6}	No change
DOWN	L	L	D_{n+1}	No change (data hold)	No change	D_{n-6}
No Edge	H	L	D_{n+1}	$D_{n+1} \dots D_{n-2} \dots D_{n-6}$	No change	No change
No Edge	X	H	D_{n+1}	Off	D_{n-6}	No change

(Note) : OUT0~7 = on in case of $D_n = \text{"H"}$ level and OUT0~7 = off in case of $D_n = \text{"L"}$ level.

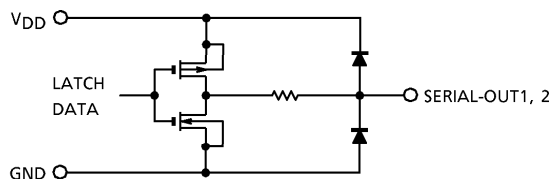
A resistor is connected with R-EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

1. $\overline{\text{ENABLE}}$, $\overline{\text{LATCH}}$, CLOCK & SERIAL-IN terminal



2. SERIAL-OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	0~7.0	V
Supply Voltage for LED	V _{CC}	0~17	V
Input Voltage	V _{IN}	-0.4~V _{DD} + 0.4	V
Output Current	I _{OUT}	-90	mA
Output Voltage	V _{CE}	-0.4~17.0	V
Clock Frequency	f _{CLK}	15	MHz
GND Terminal Current	I _{VCC}	720	mA
Power Dissipation (Note)	P _D	1.47 (P-type : FREE AIR, Ta = 25°C)	W
		0.83 (F-type : ON PCB, Ta = 25°C)	
		0.60 (F-type : FREE AIR, Ta = 25°C)	
Operating Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-55~150	°C

(Note) : P-type : Ambient temperature delated above 25°C in the proportion of 12.5 mW/°C
 F-type : Ambient temperature delated above 25°C in the proportion of 6.7 mW/°C
 On PCB (50 x 50 x 1.6 mm Cu 30%).

RECOMMENDED OPERATING CONDITION (V_{DD} = 5 V, Ta = -40~85°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply Voltage	V _{DD}	—	4.5	5.0	5.5	V	
Supply Voltage for LED	V _{CC}	GND standard	0	—	17	V	
Output Voltage	V _{OUT}	V _{CC} standard	3	—	-17	V	
Output Current	I _{OUT}	OUTn、DC 1 circuit	-5	—	-78	mA	
	I _{OH}	SERIAL-OUT1, 2	—	—	1.0		
	I _{OL}	SERIAL-OUT1, 2	—	—	-1.0		
Input Voltage	V _{IH}	V _{DD} = 4.5~5.5 V	0.7	—	V _{DD} + 0.3	V	
	V _{IL}		-0.3	—	0.3 V _{DD}		
LATCH Pulse Width	t _w LAT		100	—	—	ns	
CLOCK Pulse Width	t _w CLK		50	—	—	ns	
ENABLE Pulse Width	t _w EN		1000	—	—	ns	
Set-Up Time	t _{setup}		100	—	—	ns	
Hold Time	t _{hold}		100	—	—	ns	
Clock Frequency	f _{CLK}		Cascade operation	—	—	10.0	MHz
Power Dissipation	P _D		P-type : ON PCB, Ta = 85°C	—	—	0.76	W
			F-type : ON PCB, Ta = 85°C	—	—	0.39	

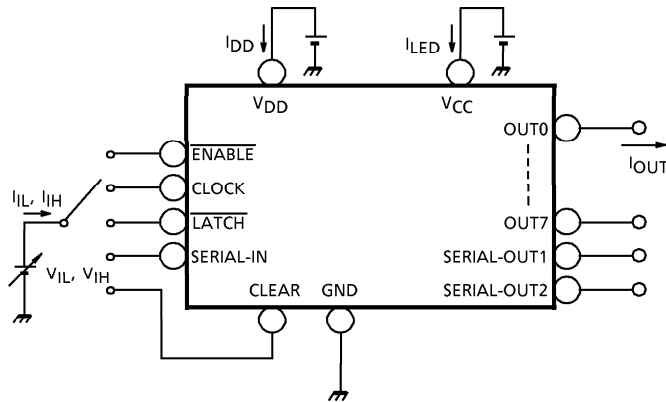
ELECTRICAL CHARACTERISTICS ($V_{CC} = 17\text{ V}$, $V_{DD} = 5\text{ V}$, $T_a = 25^\circ\text{C}$ unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}	—	—	0.7 V_{DD}	—	V_{DD}	V
	"L" Level	V_{IL}	—	—	GND	—	0.3 V_{DD}	
Output Leakage Current		I_{LEAK}	—	$V_{CC} = 17.0\text{ V}$	—	—	- 10	μA
Output Voltage	S-OUT	V_{OL}	—	$I_{OL} = 1.0\text{ mA}$	—	—	0.4	V
		V_{OH}	—	$I_{OH} = -1.0\text{ mA}$	4.6	—	—	
Output Current 1		I_{OL1}	—	$V_{OUT} = -15.0\text{ V}$	- 66.3	- 78.0	- 89.7	mA
Current Skew		ΔI_{OL1}	—	$I_{OL} = -78\text{ mA}$				
Supply Voltage Regulation		% / V_{DD}	—	$R_{EXT} = 360\ \Omega$, $T_a = -40\sim 85^\circ\text{C}$	—	1.5	5.0	% / V
Supply Current 1	"OFF"	$I_{DD}(\text{off})$	—	$R_{EXT} = \text{OPEN}$, $\text{OUT0}\sim 7 = \text{off}$	—	0.6	1.2	mA
	"ON"	$I_{DD}(\text{on})$	—	$R_{EXT} = 360\ \Omega$, $\text{DATA} = \text{"H"}$ $\text{OUT0}\sim 7 = \text{on}$	5.7	7.0	8.3	
Supply Current 2	"OFF"	$I_{CC}(\text{off})$	—	$R_{EXT} = 360\ \Omega$, $\text{ALL DATA} = \text{"L"}$ $\text{OUT0}\sim 7 = \text{off}$	—	0	2	mA
	"ON"	$I_{CC}(\text{on})$	—	$R_{EXT} = 360\ \Omega$, $\text{ALL DATA} = \text{"H"}$ $\text{OUT0}\sim 7 = \text{on}$	600	700	800	

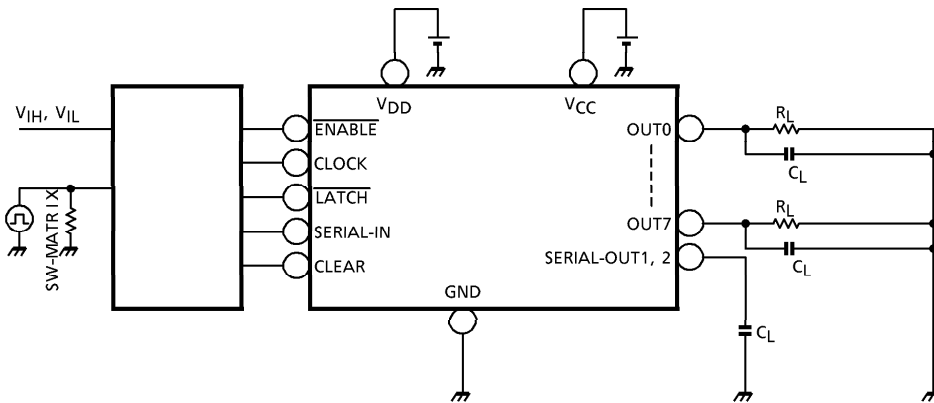
SWITCHING CHARACTERISTICS ($T_a = 25^\circ\text{C}$, unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Propagation Delay Time ("L" to "H")	CLK-OUTn	t_{pLH}	—	{CLK, LATCH & ENABLE to t_{pLH} & t_{pHL} : 50% to 50%} $V_{DD} = 5.0\text{ V}$, $V_{LED} = 17.0\text{ V}$ $V_{OUT} = -15.0\text{ V}$ $V_{IH} = V_{DD}$ $V_{IL} = \text{GND}$ $R_{EXT} = 360\ \Omega$	—	450	—	ns	
	LATCH-OUTn				—	450	—		
	ENABLE-OUTn				—	450	—		
	CLK-SOUT				—	30	70		
Propagation Delay Time ("H" to "L")	CLK-OUTn	t_{pHL}	—		—	200	—	ns	
	LATCH-OUTn				—	200	—		
	ENABLE-OUTn				—	200	—		
	CLK-SOUT				—	30	70		
Pulse Width	CLK	$t_w\ \text{CLK}, \text{CLK}$	—		—	20	30	ns	
	LATCH	$t_w\ \text{LAT}, \text{LAT}$	—		—	10	25		
Set-Up Time for LATCH & CLOCK		t_{setup}	—			—	25	50	ns
Hold Time for LATCH & CLOCK		t_{hold}	—			—	0	30	ns
Maximum CLOCK Rise Time		t_r	—		—	—	10	μs	
Maximum CLOCK Fall Time		t_f	—		—	—	10	μs	
Output Rise Time		t_{or}	—		150	300	600	ns	
Output Fall Time		t_{of}	—		150	300	600	ns	

DC CHARACTERISTICS TEST CIRCUIT

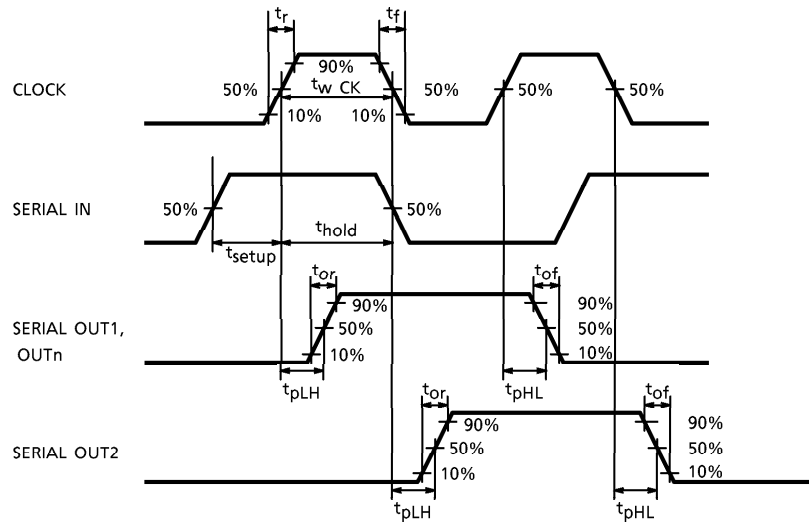


AC CHARACTERISTICS TEST CIRCUIT

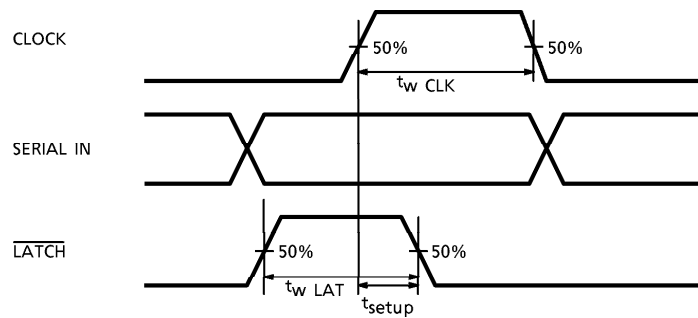


TIMING WAVEFORM

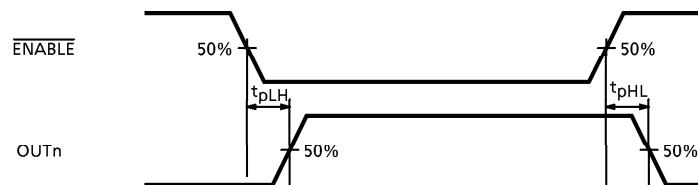
1. CLOCK-SERIAL OUT, OUTn

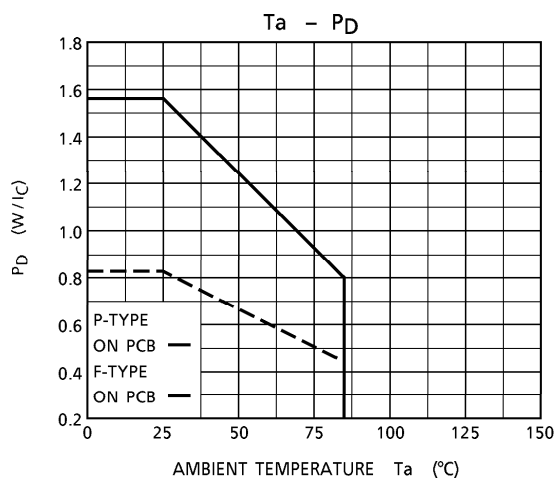
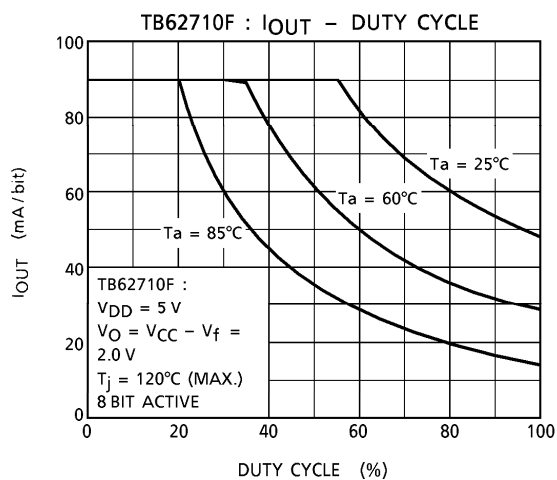
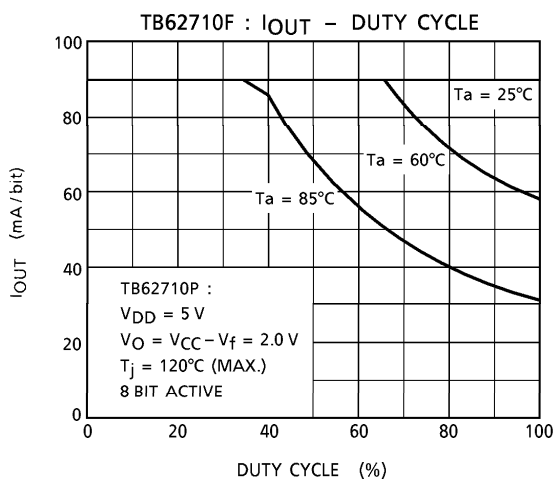


2. CLOCK-LATCH

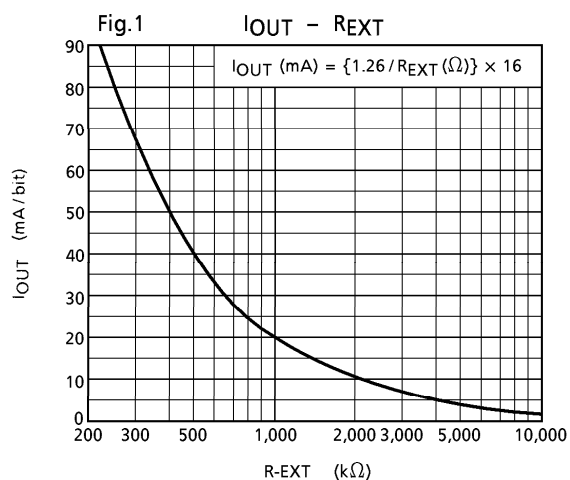


3. ENABLE-OUTn





LED DRIVER TB6270X SERIES APPLICATION NOTE



[1] Output current (I_{OUT})

I_{OUT} is set by the external resistor (R-EXT) as shown in Fig.1.

[2] Total supply voltage (V_{LED})

This device can operate 2.0 V~2.3 V (V_O).

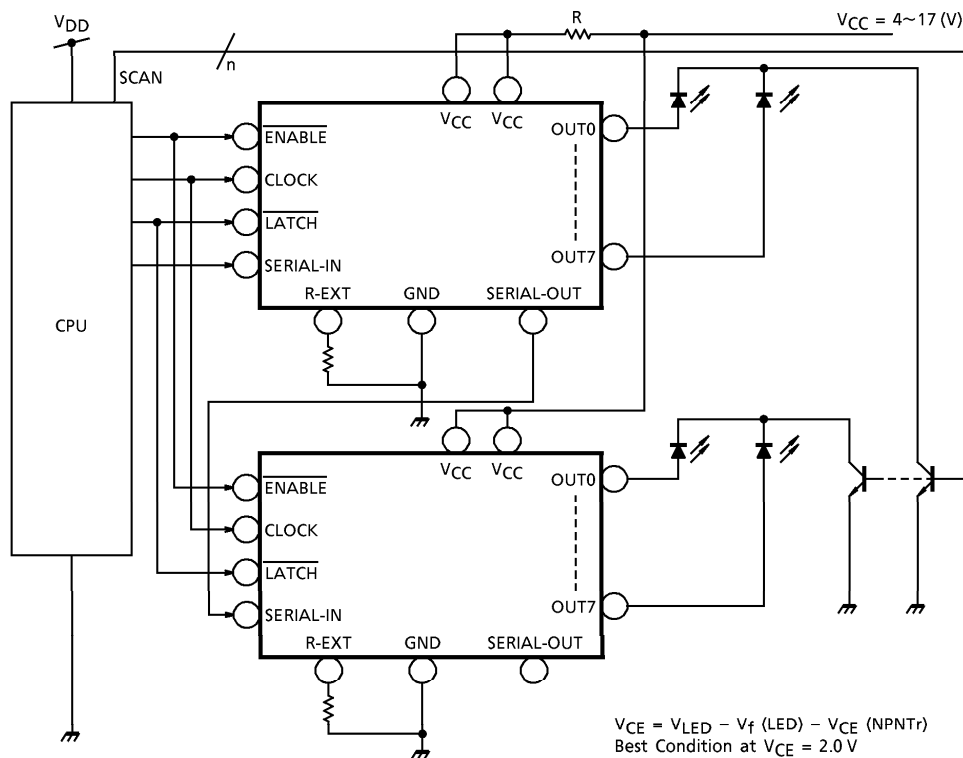
When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to power dissipation.

In order to minimize power dissipation and loss, we would like to recommended to set the total supply voltage as shown below.

$$V_{LED} \text{ (Total supply voltage)} \\ = V_{CE} (\text{Tr } V_{sat}) + V_f \text{ (LED Forward voltage)} + V_O \text{ (IC supply voltage)}$$

When the total supply is too high considering the power dissipation of this device, an additional R can decrease the supply voltage (V_O).

APPLICATION (Example of dynamic lighting circuit)



[3] Pattern layout

This device owns only one ground pin that means signal ground pin and power ground pin are common.

If ground pattern layout contains large inductance and impedance and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5 V by switching noise in operation, this device may misoperate. So we would life you to pay attention to pattern layout to minimize inductance.

PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.