ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
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NTE2987
Logic Level MOSFET
N–Channel, Enhancement Mode
High Speed Switch

Features:
- Avalanche Rugged Technology
- Logic Level Gate Drive
- $R_{DS}(on)$ = 0.09Ω Typ. at V_{GS} = 5V
- +175°C Operating Temperature
- Fast Switching
- Low Gate Charge
- High Current Capability

Absolute Maximum Ratings:

Drain Current, I_D
- Continuous
  - T_C = +25°C 20A
  - T_C = +100°C 14A
- Pulsed (Note 1) 80A

Total Power Dissipation (T_C = +25°C), P_D 105W
- Derate Above 25°C . . . . . 0.7W/°C

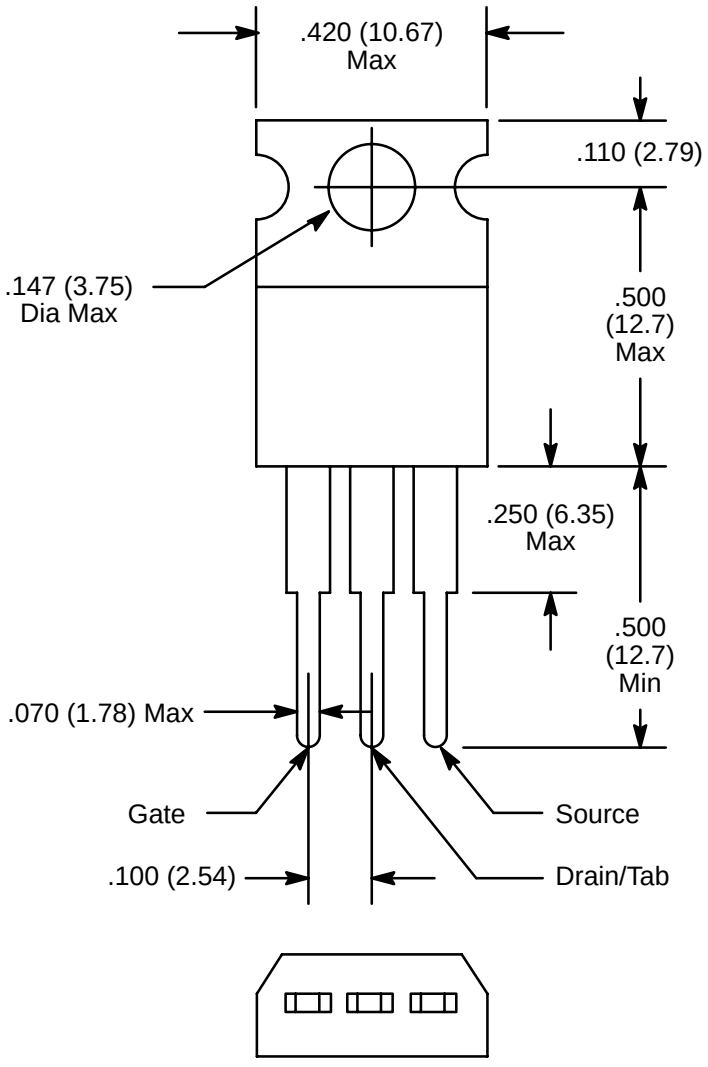
Gate–Source Voltage, V_{GS} . . . . . ±15V
Avalanche Current, Repetitive or Non–Repetitive (Note 2), I_{AR} 20A
Single Pulsed Avalanche Energy (Note 3), E_{AS} 120mJ
Repetitive Avalanche Energy (Note 2), E_{AR} 30mJ
Avalanche Current, Repetitive or Non–Repetitive (Note 4), I_{AR} 14A
Drain–Source Voltage (V_{GS} = 0), V_{DS} 100V
Drain–Gate Voltage (R_{GS} = 20kΩ), V_{DGR} 100V
Operating Junction Temperature, T_J . . . . . +175°C
Storage Temperature Range, T_{stg} . . . . . –65° to +175°C
Maximum Lead Temperature (During Soldering, 1.6mm from case, 10sec), T_L . . . . . +300°C
Thermal Resistance:
- Maximum Junction–to–Case, R_{thJC} . . . . . 1.43°C/W
- Typical Case–to–Sink (Mounting surface flat, smooth, and greased), R_{thCS} . . . . . 0.5°C/W
- Maximum Junction–to–Ambient (Free Air Operation), R_{thJA} . . . . . 62.5°C/W

Note 1. Pulse width limited by safe operating area.
Note 2. Pulse width limited by T_J max, Duty Cycle < 1%.
Note 3. V_{DD} = 25V, $I_D = I_{AR}$, Starting T_J = +175°C.
Note 4. T_C = +100°C, Pulse width limited by T_J max, Duty Cycle < 1%.

Electrical Characteristics: (T_C = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF						
Drain–Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0v, I_D = 250µA	100	–	–	V
Drain–to–Source Leakage Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0	–	–	1	µA
		V_{DS} = 80V, V_{GS} = 0V, , T_C = +150°C	–	–	10	µA
Gate–Source Leakage Forward	I_{GSS}	V_{GS} = 15V	–	–	100	nA
Gate–Source Leakage Reverse	I_{GSS}	V_{GS} = –15V	–	–	–100	nA
ON (Note 5)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	1.0	1.6	2.5	V
Static Drain–Source ON Resistance	$R_{DS(on)}$	V_{GS} = 5V, I_D = 10A	–	0.09	0.12	Ω
On–State Drain Current	$I_{D(on)}$	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$max, V_{GS} = 10V	20	–	–	A
Dynamic						
Forward Transconductance	g_{fs}	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$max, I_D = 10A, Note 5	10	16	–	mhos
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	1200	1500	pF
Output Capacitance	C_{oss}		–	250	350	pF
Reverse Transfer Capacitance	C_{rss}		–	60	90	pF
Switching						
Total Gate Charge	Q_g	V_{GS} = 5V, I_D = 20A, V_{DD} = 80V	–	22	30	nC
Gate–Source Charge	Q_{gs}		–	6	–	nC
Gate–Drain (“Miller”) Charge	Q_{gd}		–	12	–	nC
Turn–On Delay Time	$t_{d(on)}$	V_{DD} = 30V, I_D = 10A, R_G = 50Ω, V_{GS} = 5V	–	50	70	ns
Rise Time	t_r		–	140	200	ns
Turn–Off Delay Time	$t_{d(off)}$	V_{DD} = 80V, I_D = 20A, R_G = 50Ω, V_{GS} = 5V	–	80	110	ns
Fall Time	t_f		–	80	110	ns
Source–Drain Diode Ratings and Characteristics						
Continuous Source Current	I_S	(Body Diode)	–	–	20	A
Pulse Source Current	I_{SM}	(Body Diode) Note 1	–	–	80	A
Diode Forward Voltage	V_{SD}	I_{SD} = 20A, V_{GS} = 0V, Note 5	–	–	1.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, V_{DD} = 50V, I_{SD} = 20A, di/dt = 100A/µs	–	130	–	ns
Reverse Recovery Charge	Q_{rr}		–	0.4	–	µC
Reverse Recovery Current	I_{RRM}		–	6	–	A

Note 1. Pulse width limited by safe operating area.
Note 5. Pulse Test: Pulse Width = 300µs, Duty Cycle = 1.5%.


.420 (10.67)
Max
.110 (2.79)
.147 (3.75)
Dia Max
.500
(12.7)
Max
.250 (6.35)
Max
.500
(12.7)
Min
.070 (1.78) Max
Gate
Source
.100 (2.54)
Drain/Tab