

Modulation PLL for GSM, DCS and PCS Systems

Description

The U2893B is a monolithic integrated circuit. It is realized using TEMIC's advanced silicon bipolar UHF5S technology. The device integrates a mixer, an I/Q modulator, a phase-frequency detector (PFD) with two synchronous-programmable dividers, and a charge pump. The U2893B is designed for cellular phones such as GSM, DCS1800, and PCS1900, applying a transmitter-archi-

ture where the VCO is operated at the TX output frequency.

U2893B exhibits low power consumption, and the power-down function extends battery life.

The IC is available in a shrunk small-outline 28-pin package (SSO28).

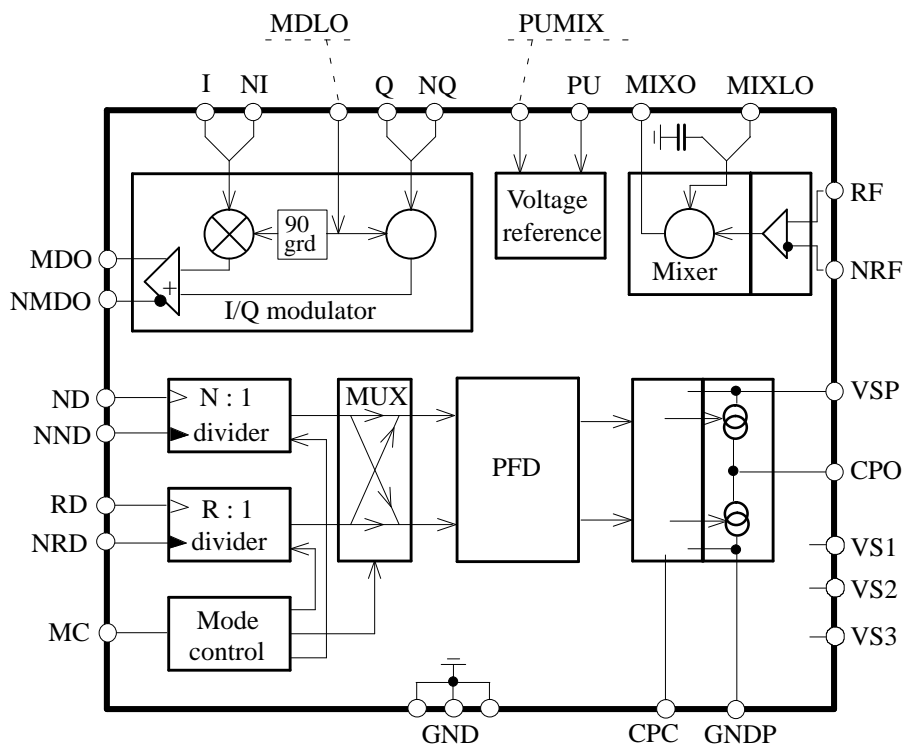
Features

- Supply voltage down to 2.7 V
- Current consumption 40 mA
- Power-down function
- Low-current standby mode
- High-speed PFD and charge pump
- Integrated dividers

Benefits

- High-level RF integration
- TX architecture saves filter costs
- Low external part count
- Small SSO28 package
- One device for various applications

Block Diagram



12494

Figure 1. Block diagram

Pin Description

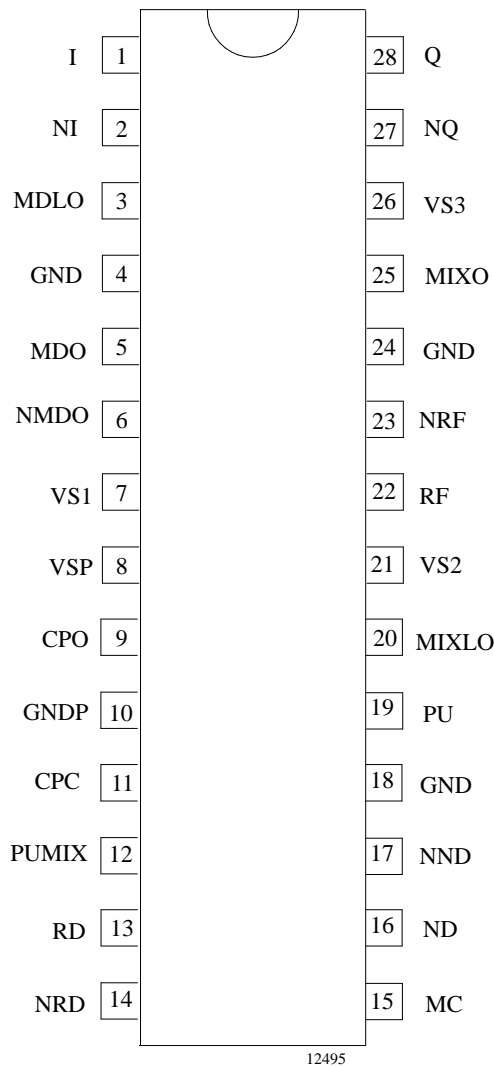


Figure 2. Pinning

Pin	Symbol	Function
1	I	In-phase baseband input
2	NI	Complementary to I
3	MDLO	I/Q-modulator LO input
4	GND ¹⁾	Negative supply
5	MDO	I/Q-modulator output
6	NMDO	Complementary to MDO
7	VS1 ³⁾	Positive supply (I/Q MOD)
8	VSP	Pos. supply charge-pump
9	CPO	Charge-pump output
10	GNDP ²⁾	Neg. supply charge pump
11	CPC	Charge-pump current control (input)
12	PUMIX	Power-up, mixer only
13	RD	R-divider input
14	NRD	Complementary to RD
15	MC	Mode control
16	ND	N-divider input
17	NND	Complementary to ND
18	GND ¹⁾	Negative supply
19	PU	Power-up, whole chip except mixer
20	MIXLO	Mixer LO input
21	VS2 ³⁾	Positive supply (MISC.)
22	RF	Mixer RF-input
23	NRF	Complementary to RF
24	GND ¹⁾	Negative supply
25	MIXO	Mixer output
26	VS3 ³⁾	Positive supply (mixer)
27	NQ	Complementary to Q
28	Q	Quad.-phase baseband input

- 1) All GND pins must be connected to GND potential. No DC voltage between GND pins!
- 2) Max. voltage between GNDP and GND pins ≤ 200 mV
- 3) The maximum permissible voltage difference between pins VS1, VS2 and VS3 is 200 mV.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage VS1, VS2, VS3	V _{VS#}	≤ V _{VSP}	V
Supply voltage charge pump VSP	V _{VSP}	5.5	V
Voltage at any input	V _{Vi#}	-0.5 ≤ V _{VS} + 0.5 ≤ 5.5	V
Current at any input / output pin except CPC	I _{I#} I _{O#}	2	mA
CPC output currents	I _{CPC}	5	mA
Ambient temperature	T _{amb}	-20 to +85	°C
Storage temperature	T _{stg}	-40 to +125	°C

Operating Range

Parameters	Symbol	Value	Unit
Supply voltage	V _{VS#} , V _{VSP}	2.7 to 5.5	V
Ambient temperature	T _{amb}	-20 to +85	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO28	R _{thJA}	130	K/W

Electrical Characteristics: General Data

T_{amb} = 25°C, V_S = 2.7 to 5.5 V

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
DC supply						
Supply voltages VS#	V _{VS1} = V _{VS2} = V _{VS3}	V _{VS#}	2.7		5.5	V
Supply voltage VSP		V _{VSP}	V _{VS#} -0.3		5.5	V
Supply current I _{VS1}	Active (V _{PU} = VS)	I _{VS1A}		16		mA
	Standby (V _{PU} = 0)	I _{VS1Y}			20	μA
Supply current I _{VS2}	Active (V _{PU} = VS)	I _{VS2A}		21		mA
	Standby (V _{PU} = 0)	I _{VS2Y}			20	μA
Supply current I _{VS3}	Active (V _{PUMIX} = VS)	I _{VS3A}		11		mA
	Standby (V _{PUMIX} = 0)	I _{VS3Y}			30	μA
Supply current I _{VSP} ¹⁾	Active (V _{PU} = VS, CPO open)	I _{VSPA}		2)	20	mA
	Standby (V _{PU} = 0)	I _{VSPY}			20	μA
N & R divider inputs ND, NND & RD, NRD						
N:1 divider frequency	50-Ω source	F _{ND}	100		650	MHz
R:1 divider frequency	50-Ω source	F _{RD}	100		400	MHz
Input impedance	Active & standby	Z _{RD} , Z _{ND}	1 kΩ		2 pF	-
Input sensitivity	50-Ω source	V _{RDef} , V _{NDef}	30		200	mV

1) 100-MHz PFD operation, pump current set to 4 mA, zero phase difference (steady state)

2) See chapter "Supply Current of the Charge Pump i(VSP) vs. Time", page 6.

Electrical Characteristics: General Data (continued)

T_{amb} = 25°C, V_S = 2.7 to 5.5 V

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Phase-frequency detector (PFD)						
PFD operation	F _{ND} = 650 MHz, n = 5 F _{RD} = 300 MHz, r = 2	FM _{PFD}	150			MHz
Frequency comparison only	F _{ND} = 650 MHz, n = 5 F _{RD} = 300 MHz, r = 2	FM _{FD}	200			MHz
I/Q modulator baseband inputs I, NI & Q, NQ						
DC voltage	Referred to GND	V _I , V _{NI} , V _Q , V _{NQ}	1.35	VS1/2	VS1/2 + 0.1	V
MD_IQ	Frequency range	FR _{IQ}	DC		1	MHz
AC voltage ³⁾	Referred to GND	AC _I , AC _{NI} , AC _Q , AC _{NQ}		200		mVpp
	Differential (preferres)	AC _{DI} , AC _{DQ}		400		mVpp
I/Q modulator LO input MDLO						
MDLO	Frequency range	F _{MDLO}	50		350	MHz
Input impedance	Active & standby	Z _{MDLO}		250		W
Input level	50-Ω source	P _{MDLO}		-12	-5	dBm
I/Q modulator outputs MDO, NMDO						
DC current	V _{MDO} , V _{NMDO} = VS	I _{MDO} , I _{NMDO}		2.4		mA
Voltage compliance	V _{MDO} , V _{NMDO} = VC	VC _{MDO} , VC _{NMDO}				
MDO output level (differential)	500 Ω to VS ⁴⁾	P _{MDOeff}	120		150	mV
Carrier suppression ⁴⁾		CS _{MDO}	-30	-35		dBc
Sideband suppression ⁴⁾		SS _{MDO}	-35	-40		dBc
IF spurious ⁴⁾	f _{LO} +/- 3 × f _{mod}	SP _{MDO}	-45	-50		dBc
Noise ⁴⁾	@ 400 kHz off carrier	N _{MDO}	-115			dBc/Hz
Frequency range		FR _{MDO}	50		350	MHz
Mixer (900 MHz)						
RF input level	900 MHz	P _{9RF}	tbd	-15		dBm
LO-spurious at RF/NRF port	@ P _{9MIXLO} = -10 dBm @ P _{9RF} = -15 dBm	SP _{9RF}			-40	dBm
MIXLO input level	0.05 to 2 GHz	P _{9MIXLO}	tbd	-10		dBm
MIXO (100-Ω load)	Frequency range	FR _{MIXO}	50		350	MHz
... Output level ⁵⁾	@ P _{9MIXLO} = -15 dBm	P _{9MIXOeff}		70		mV
... Carrier suppression	@ P _{9MIXLO} = -15 dBm	CS _{9MIXO}	-20			dBc

3) Single-ended operation (complementary baseband input is AC-grounded) leads to reduced linearity degrading suppression of odd harmonics

4) With typical drive levels at MDLO- & I/Q-inputs

5) -1 dB compression point (CP-1)

Electrical Characteristics: General Data (continued)

T_{amb} = 25°C, V_S = 2.7 to 5.5 V

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Mixer (1900 MHz)						
RF input level	0.5 to 2 GHz	P19 _{RF}		-17		dBm
LO-spurious at RF/NRF ports	@ P19 _{MIXLO} = -10 dBm @ P19 _{RF} = -15 dBm	SP19 _{RF}			-40	dBm
MIXLO input level	0.05 to 2 GHz	P19 _{MIXLO}		-8		dBm
MIXO (100 Ω load)						
... Output level ⁵⁾	@ P19 _{MIXLO} = -17 dBm	P19 _{MIXO}		55		mV _{eff}
... Carrier suppression	@ P19 _{MIXLO} = -17 dBm	CS19 _{MIXO}	-20			dBc
Charge pump output CPO						
Pump current pulse	CPC open	I _{CPO}	0.8	1	1.2	mA
	2.23 kΩ CPC to GND	I _{CPO 2}	1.6	2	2.4	mA
	760 Ω CPC to GND	I _{CPO 4}	3.6	4	4.4	mA
TK pump current		Tk_ I _{CPC}			15	%/100 k
Mismatch source / sink current	(I _{CPOSI} - I _{CPOSO})/I _{CPOSI} I _{CPOSO} = I _{source} I _{CPOSI} = I _{sink}	M _{I_{CPO}}			10	%
Sensitivity to VSP	$\left \frac{\Delta I_{CPO}}{I_{CPO}} \right \quad / \quad \left \frac{\Delta VSP}{VSP} \right $	S _{I_{CPO}}			0.1	-
Charge pump control input CPC						
Compensation capacitor		C _{CPC}	500			pF
Short circuit current ⁶⁾	CPC grounded	I _{CPC}	2	2.7	3.7	mA
Mode control						
Sink current	V _{MC} = V _S	I _{MC}		20		μA
Power-up input PU (power-up for all functions, except mixer)						
Settling time	Output power within 10% of steady state values	S _{PU}		5	10	μs
High level	Active	V _{PUH}	2.5			V
Low level	Standby	V _{PUL}	0		0.4	V
High-level current	Active, V _{PUH} = 2.7 V	I _{PUH}	0.1		0.6	mA
Low-level current	Standby, V _{PUL} = 0.4 V	I _{PUL}	-10		0	mA
Power-up input PUMIX (power-up for mixer only)						
Settling time	Output power within 10% of steady state values			5	10	μs
High level	Active	V _{PUMIXH}	2.5			V
Low level	Standby	V _{PUMIXL}	0		0.4	V
High-level current	Active, V _{PUMIXH} = 2.7 V	I _{PUMIXH}	0.1		0.6	mA
Low-level current	Standby, V _{PUMIXL} = 0.4 V	I _{PUMIXL}	-10		0	mA

⁶⁾ See figures 6 and 14.

Supply Current of the Charge Pump $i(VSP)$ vs. Time

Due to the pulsed operation of the charge pump, the current into the charge-pump supply pin VSP is not constant. Depending on I (see figure 6) and the phase difference at the phase detector inputs, the current $i(VSP)$ over time varies. Basically, the total current is the sum of the quiescent current, the charge-/discharge current, and – after each phase comparison cycle – a current spike (see figure 3).

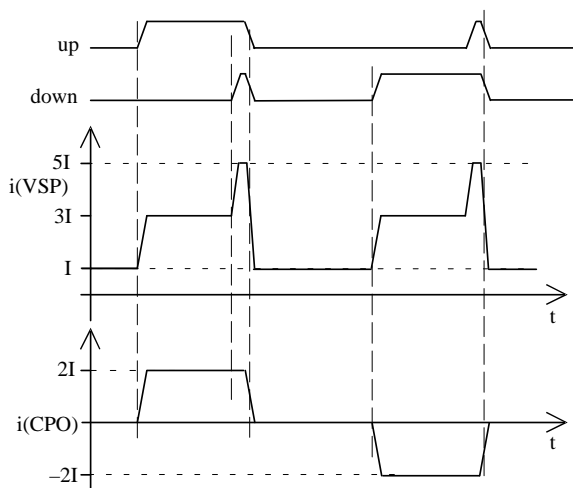


Figure 3. Supply current of the charge pump = $f(t)$

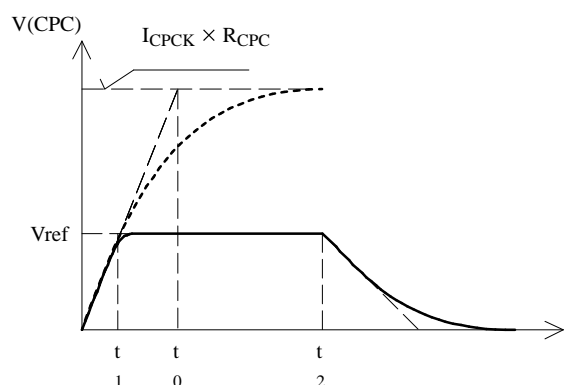
Internal current, I , vs. current out of pin CPC

I vs. $I(CPC)$	I_{CPC}	I
CPC open	0	0.5 mA
2.23 kW to GND	-0.5 mA	1.0 mA
743 W to GND	-1.5 mA	2.0 mA
CPC shorted to GND	I_{CPC}	>2.0 mA

Initial Charge Pump Current after Power-Up

Due to stability reasons, the reference current generator for the charge pump needs an external capacitor (>500 pF from CPC to GND). After power-up, only the on-chip generated current $I = I_{CPC}$ is available for charging the external capacitor. Due to the charge pump's architecture, the charge pump current will be $2 \times I = 2 \times I_{CPC}$ until the voltage on CPC has reached the reference voltage (1.1 V). The following figures illustrate this behavior.

The behavior of $I(CPO)$ after power-up can be very advantageous for a fast settling of the loop. By using larger capacitors (>1 nF), an even longer period with maximum charge pump current is possible.



Time t_1 can be calculated as $t_1 \approx (1.1 \text{ V} \times C_{CPC})/I_{CPC}$
 e.g., $C_{CPC} = 1 \text{ nF}$, $I_{\max} = 3.5 \text{ A} \rightarrow t_1 \approx 0.3 \mu\text{s}$.
 Time t_2 can be calculated as $t_2 \approx (R_{CPC}/2230 \Omega) \times C_{CPC}$
 e.g., $C_{CPC} = 1 \text{ nF}$, $R_{CPC} = 2230 \Omega \rightarrow t_2 \approx 1.1 \mu\text{s}$

Figure 4.

Mode Selection

The device can be programmed to different modes via an external resistor (including short, open) connected between Pin MC and VS2. The mode selection controls the N-, R-divider ratios, and the polarity of the charge pump current.

Mode Selection		N-Divider	R-Divider	CPO Current Polarity		Application
Mode	Resistance between Pin MC and Pin VS2			$f_N < f_R$ ¹⁾	$f_N < f_R$ ¹⁾	
1	0 (<50 Ω)	3:1	5:1	Sink	Source	GSM
2	2.7 kΩ (±5%)	2:1	5:1	Source	Sink	PCS
3	10 kΩ (±5%)	2:1	6:1	Source	Sink	DCS
4	36 kΩ (±5%)	3:1	6:1	Source	Sink	GSM
5	∞ (>1 MΩ)	3:1	6:1	Sink	Source	GSM

1) Frequencies referred to PFD input!

Equivalent Circuits at the IC's Pins

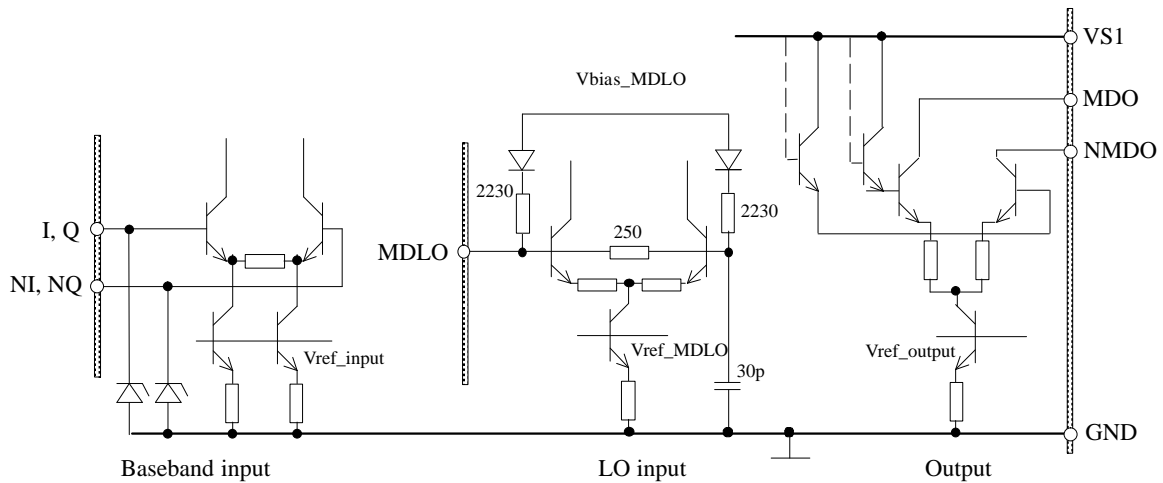


Figure 5. I/Q modulator

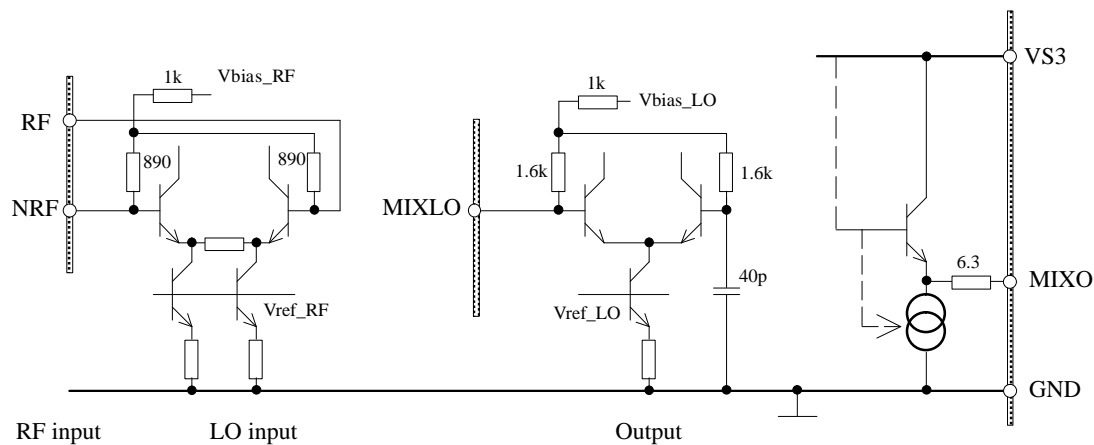


Figure 6. Mixer

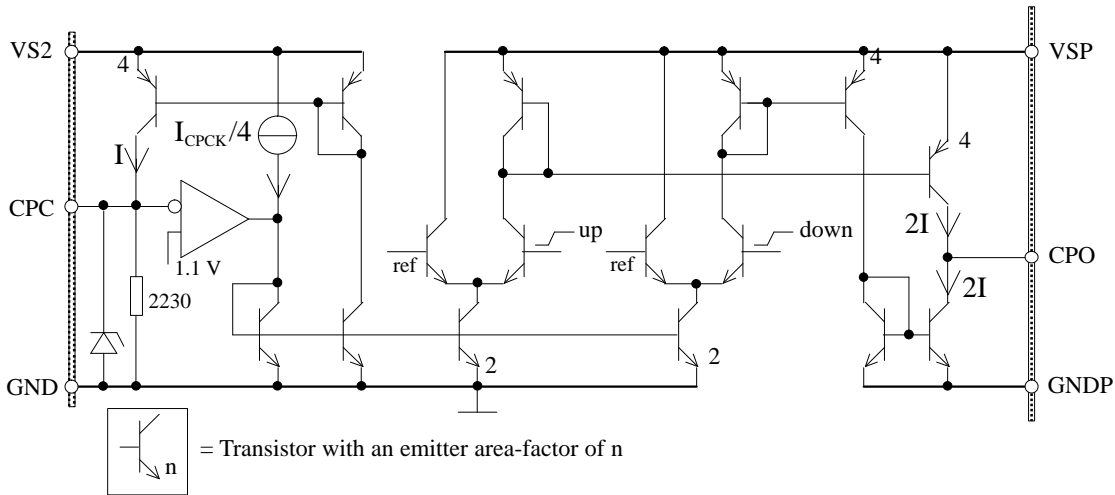


Figure 7. Charge pump

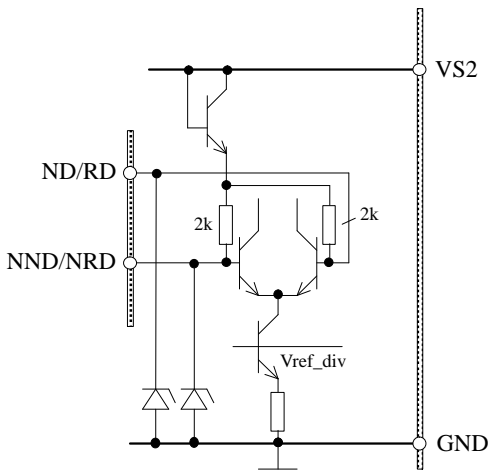


Figure 8. Dividers

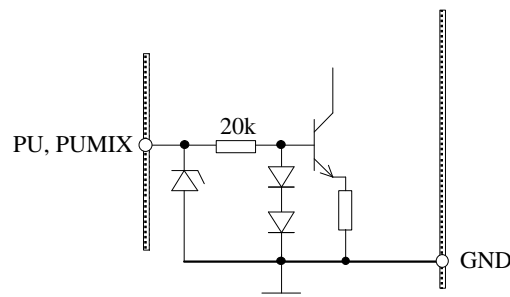


Figure 9. Power-up

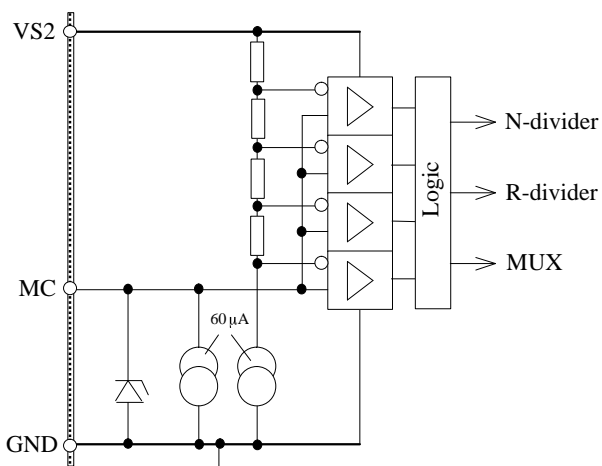


Figure 10. Mode control

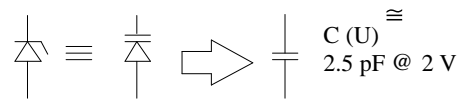


Figure 11. ESD-protection diodes

Application Hints

For some of the baseband ICs it may be necessary to reduce the I/Q voltage swing so that it can be handled by the U2893B. In those cases, the following circuitry can be used.

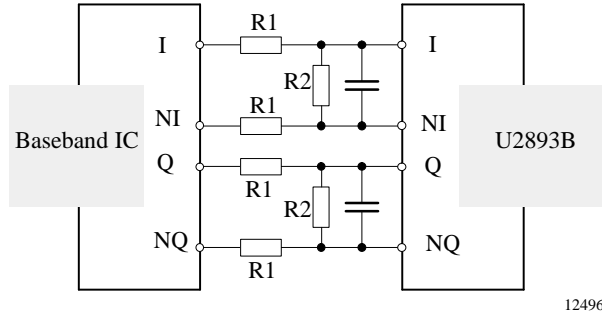


Figure 12. Interfacing the U2893B to I/Q baseband circuits

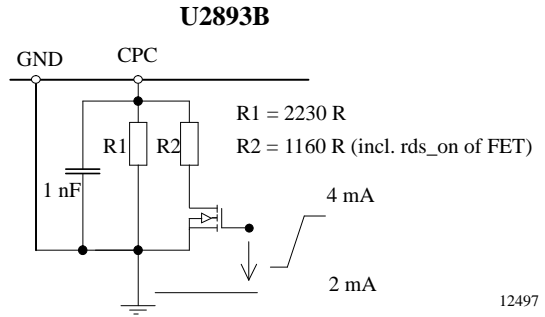


Figure 14. Programming the charge pump current

Application examples for programming different modes.

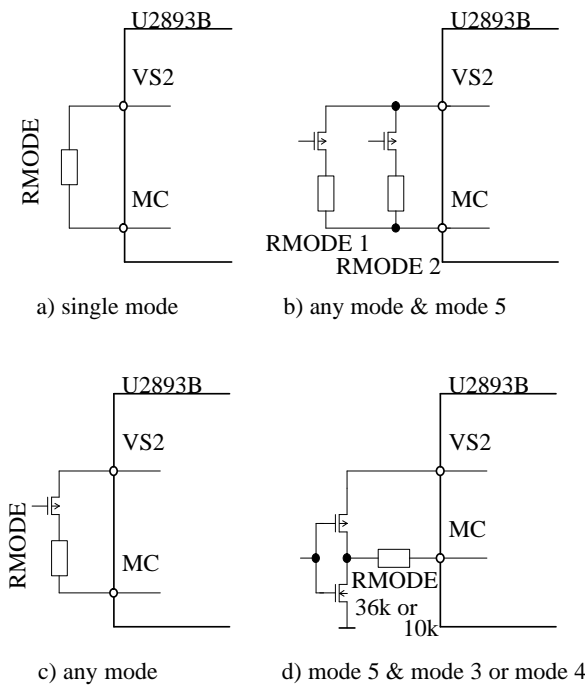
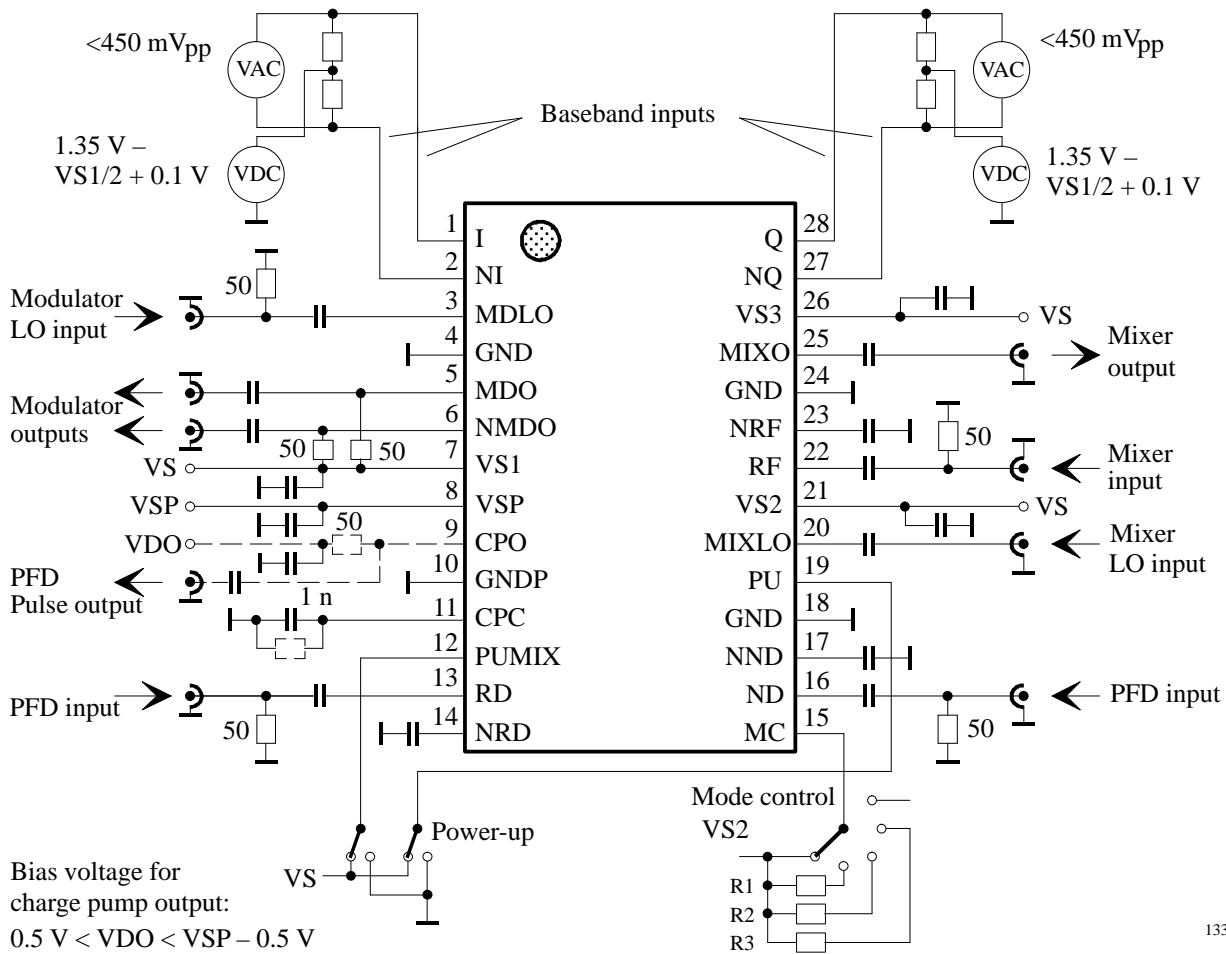


Figure 13. Mode control

Test Circuit



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Figure 15. Test circuit

Application Circuit (900 MHz)

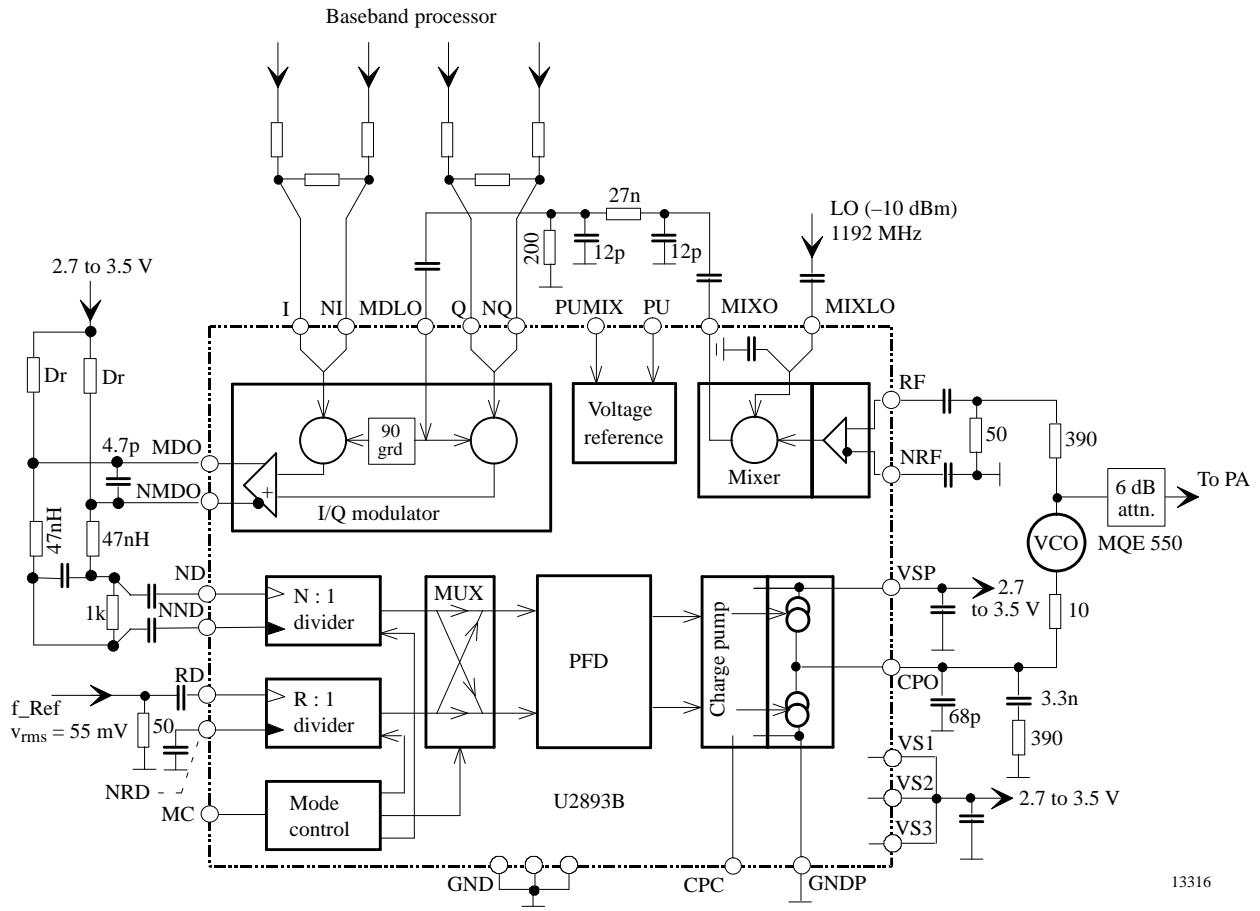
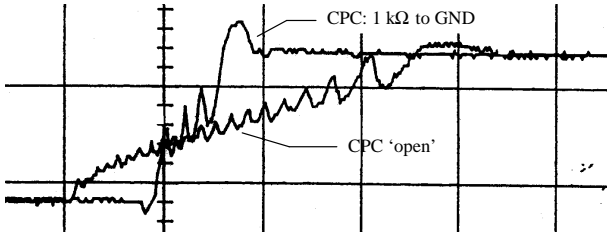


Figure 16. Power-up, charge pump control, and mode control must be connected according to the application used

Measurements

Modulation-Loop Settling Time

As valid for all PLL loops the settling time depends on several factors. The following figure is an extraction from measurements performed in an arrangement like the application circuit. It shows that a loop settling time of a few μs can be achieved.



Vertical: VCO tuning voltage 1 V/Div
Horizontal: Time 1 μs /Div

Figure 17.

Modulation Spectrum & Phase Error

The figure of the TX spectrum and the phase error distribution, respectively, shows the suitability of the modulation-loop concept for GSM.

Vertical: VRef. level = 28.6 dBm, 10 dBm/Div
Horizontal: Center = 900 MHz, VBW, RBW = 30 kHz, 400 kHz/Div

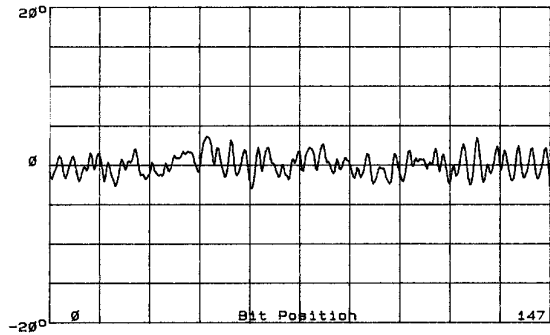


Figure 18.

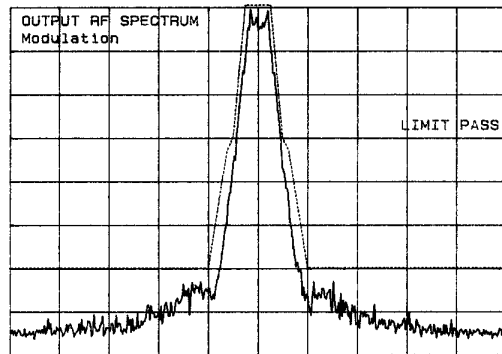
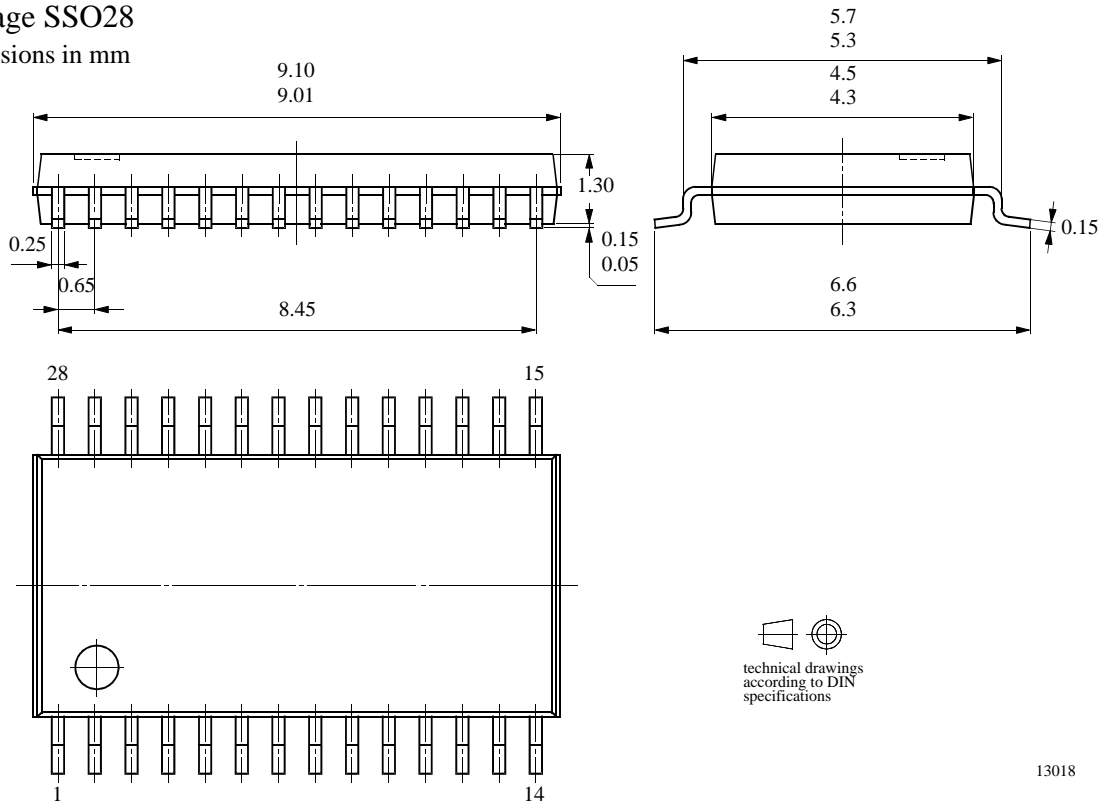


Figure 19.

Package Information

Package SSO28

Dimensions in mm



13018

Ozone Depleting Substances Policy Statement

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1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

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