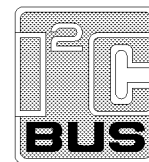


# Radio tuning PLL frequency synthesizers

# TSA6057; TSA6057T

## FEATURES

- On-chip AM and FM prescalers with high input sensitivity
- On-chip high performance one input (two output) tuning voltage amplifier for the AM and FM loop filters
- On-chip 2-level current amplifier (charge pump) to adjust the loop gain
- Only one reference oscillator (4 MHz) for both AM and FM
- High speed tuning due to a powerful digital memory phase detector
- 40 kHz output reference frequency for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100)
- Oscillator frequency ranges of: 512 kHz to 30 MHz and 30 to 150 MHz
- 3 selectable reference frequencies of 1, 10 or 25 kHz for both tuning ranges
- Serial 2-wire I<sup>2</sup>C-bus interface to a microcontroller and one programmable address input
- Software controlled band switch output.



## GENERAL DESCRIPTION

The TSA6057 is a bipolar single chip frequency synthesizer manufactured in SUBILO-N technology (components laterally separated by oxide). It performs all the tuning functions of a PLL radio tuning system. The IC is designed for application in all types of radio receivers.

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TSA6057	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TSA6057T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

## Radio tuning PLL frequency synthesizers

## TSA6057; TSA6057T

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC1}$	supply voltage 1; pin 3		4.5	5.0	5.5	V
$V_{CC2}$	supply voltage 2; pin 16		$V_{CC1}$	8.5	12	V
$I_{CC1}$	supply current 1; pin 3	no outputs loaded	12	20	28	mA
$I_{CC2}$	supply current 2; pin 16	version C1	0.2	0.5	1	mA
		version C8	0.7	1	1.5	mA
$f_{iAM(max)}$	maximum input frequency on $AM_I$		30	–	–	MHz
$f_{iAM(min)}$	minimum input frequency on $AM_I$		–	–	0.512	MHz
$f_{iFM(max)}$	maximum input frequency on $FM_I$		150	–	–	MHz
$f_{iFM(min)}$	minimum input frequency on $FM_I$		–	–	30	MHz
$V_{iAM(rms)}$	input voltage on $AM_I$ (RMS value)	$V_{iFM} = 0$ V	30	–	500	mV
$V_{iFM(rms)}$	input voltage on $FM_I$ (RMS value)	$V_{iAM} = 0$ V	20	–	300	mV
$P_{tot}$	total power dissipation		–	0.14	–	W
$T_{amb}$	operating ambient temperature	version C1	–30	–	+85	°C
		version C8	–40	–	+85	°C

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BLOCK DIAGRAM

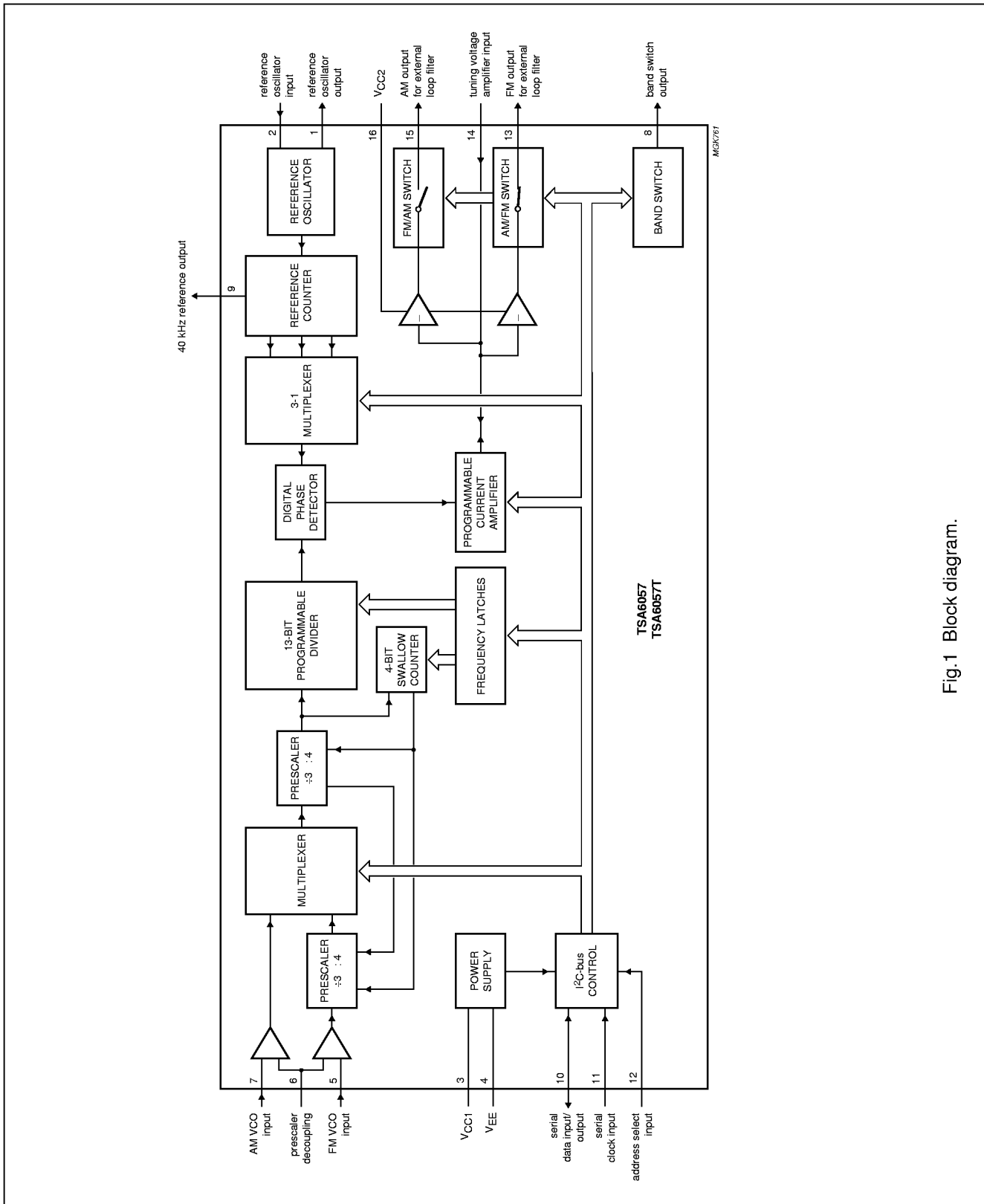


Fig.1 Block diagram.

## Radio tuning PLL frequency synthesizers

## TSA6057; TSA6057T

## PINNING

SYMBOL	PIN	DESCRIPTION
XTAL1	1	reference oscillator output
XTAL2	2	reference oscillator input
V <sub>CC1</sub>	3	positive supply voltage 1
V <sub>EE</sub>	4	ground
FM <sub>I</sub>	5	FM VCO input
DEC	6	prescaler decoupling
AM <sub>I</sub>	7	AM VCO input
BS	8	band switch output
f <sub>ref</sub>	9	40 kHz reference output
SDA	10	serial data input/output; I <sup>2</sup> C-bus
SCL	11	serial clock input; I <sup>2</sup> C-bus
AS	12	address select input; I <sup>2</sup> C-bus
FM <sub>O</sub>	13	FM output for external loop filter
LOOP <sub>I</sub>	14	tuning voltage amplifier input
AM <sub>O</sub>	15	AM output for external loop filter
V <sub>CC2</sub>	16	positive supply voltage 2

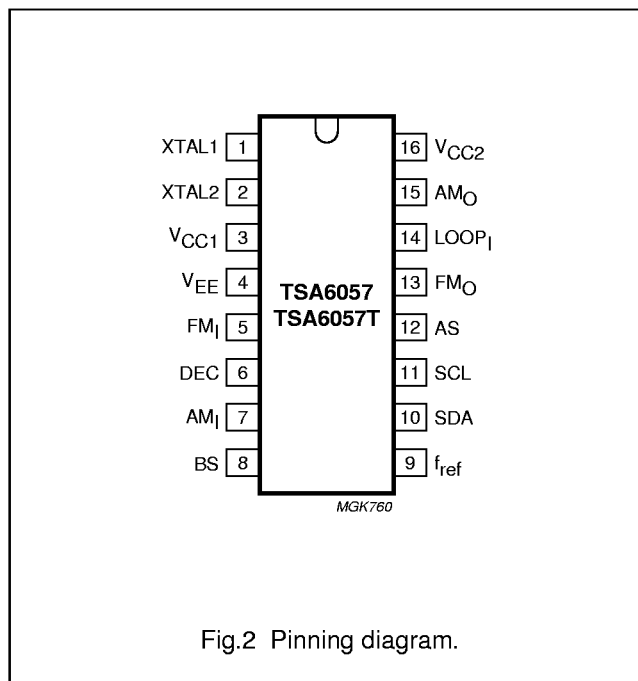


Fig.2 Pinning diagram.

## FUNCTIONAL DESCRIPTION

The TSA6057 contains the following parts and facilities:

- Separate input amplifiers for the AM and FM VCO-signals.
- A prescaler with the divisors 3 : 4 on AM and 15 : 16 on FM, a multiplexer to select AM or FM and a 4-bit, programmable swallow counter.
- A 13-bit programmable counter.
- A digital memory phase detector.
- A reference frequency channel comprised of a 4 MHz crystal oscillator followed by a reference counter. The reference frequency can be 1, 10 or 25 kHz and is applied to the digital memory phase detector. The reference counter also outputs a 40 kHz reference frequency to pin 9 for co-operation with the FM/IF system and microcomputer-based tuning interface IC (TEA6100).
- A programmable current amplifier (charge pump) which consists of a 5 and a 450  $\mu$ A current source. This allows adjustment of loop gain, thus providing high current-high speed tuning and low current-stable tuning.
- A one input, two output tuning voltage amplifier. One output is connected to the external AM loop filter and the other output to the external FM loop filter. Under software control, the AM output is switched to a high impedance state by the FM/AM switch in the FM position

and the FM output is switched to a high impedance state by the AM/FM switch in the AM position. The outputs can deliver a tuning voltage of up to 10.5 V.

- An I<sup>2</sup>C-bus interface with data latches and control logic. The I<sup>2</sup>C-bus is intended for communication between microcontrollers and different ICs or modules. Detailed information on the I<sup>2</sup>C-bus specification is available on request.
- A software-controlled band switch output.

## Controls

The TSA6057 is controlled via the 2-wire I<sup>2</sup>C-bus. For programming there is one module address, a logic 0 R/W bit, a subaddress byte and four data bytes. The subaddress determines which one of the four data bytes is transmitted first. The module address contains a programmable address bit (D1) which with address select input AS (pin 12) makes it possible to operate two TSA6057s in one system.

The auto increment facility of the I<sup>2</sup>C-bus allows programming of the TSA6057 within one transmission (address + subaddress + 4 data bytes).

- The TSA6057 can also be partially programmed. Transmission must then be ended by a STOP condition.

The bit organization of the 4 data bytes is shown in Fig.3 and described in Tables 1 to 5.

## Radio tuning PLL frequency synthesizers

## TSA6057; TSA6057T

**Table 1** The bits S0 to S16 (DB0: D1 to D7; DB1: D0 to D7 and DB2: D0 and D1) together with bit FM/AM (DB2: D5) are used to set the divisor of the input frequency at inputs AM<sub>I</sub> (pin 7) or FM<sub>I</sub> (pin 5). If the system is in lock the following is valid:

FM/AM	INPUT FREQUENCY (f <sub>i</sub> )	INPUT
0	$(S0 \times 2^0 + S1 \times 2^1 + S13 \times 2^{13} + S14 \times 2^{14}) \times f_{ref}$	AM <sub>I</sub> <sup>(1)</sup>
1	$(S0 \times 2^0 + S1 \times 2^1 + S15 \times 2^{15} + S16 \times 2^{16}) \times f_{ref}$	FM <sub>I</sub> <sup>(2)</sup>

**Notes**

1. The minimum dividing ratio for AM mode is  $2^6 = 64$ .
2. The minimum dividing ratio for FM mode is  $2^8 = 256$ .

**Table 2** The bit CP is used to control the charge pump current (DB0: D0)

CP	CURRENT
0	low
1	high

**Table 3** The bits REF1 and REF2 are used to set the reference frequency applied to the phase detector (DB2: D7 and D6)

REF1	REF2	FREQUENCY (kHz)
0	0	1
0	1	10
1	0	25
1	1	none

**Table 4** The bit FM/AM OPAMP controls the switch AM/FM; FM/AM in the tuning voltage amplifier output circuitry (DB2: D4)

FM/AM OPAMP	SWITCH FM/AM	SWITCH AM/FM
1	closed	open
0	open	closed

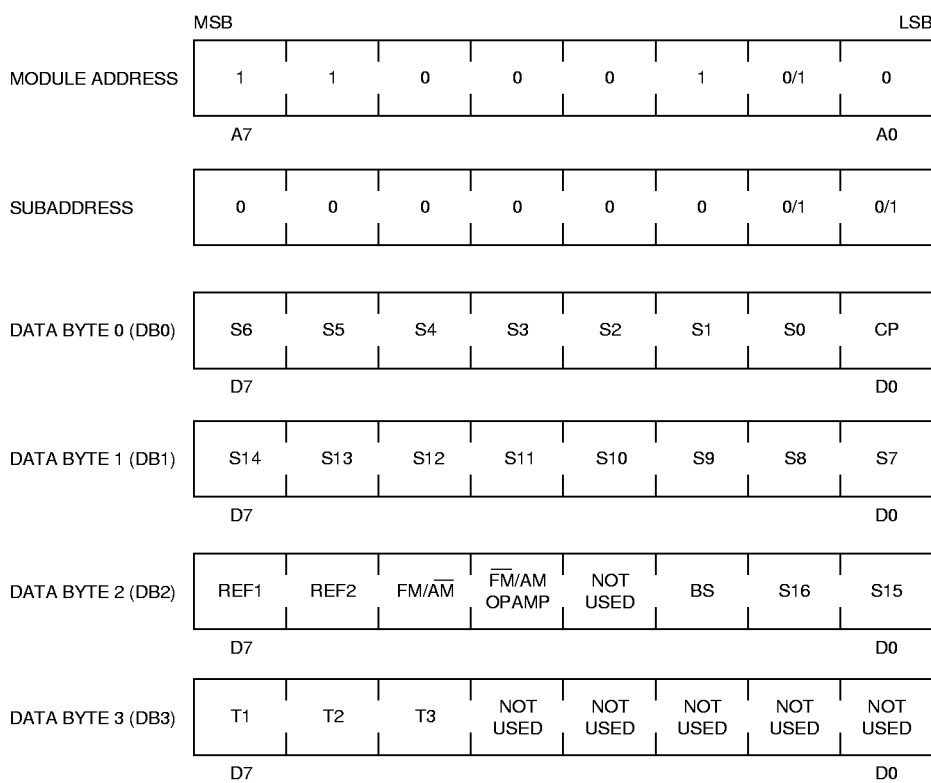
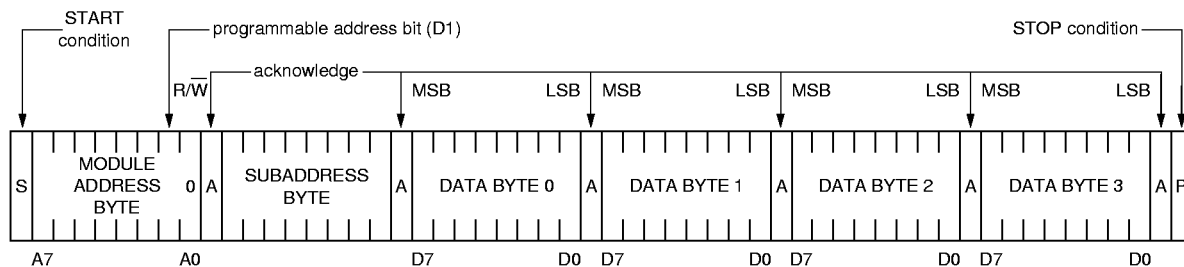
**Table 5** The bit BS controls the open collector band switch output (DB2: D2)

BS	BAND SWITCH OUTPUT
1	sink current
0	floating

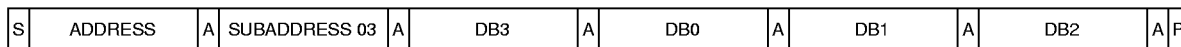
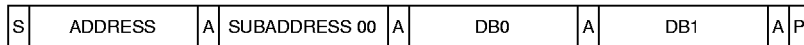
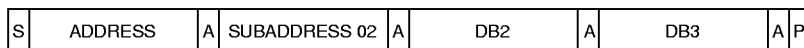
Remark: data byte DB3 must be set to 0000 0000. It is also used for test purposes.

# Radio tuning PLL frequency synthesizers

# TSA6057; TSA6057T



Examples using auto-increment facility



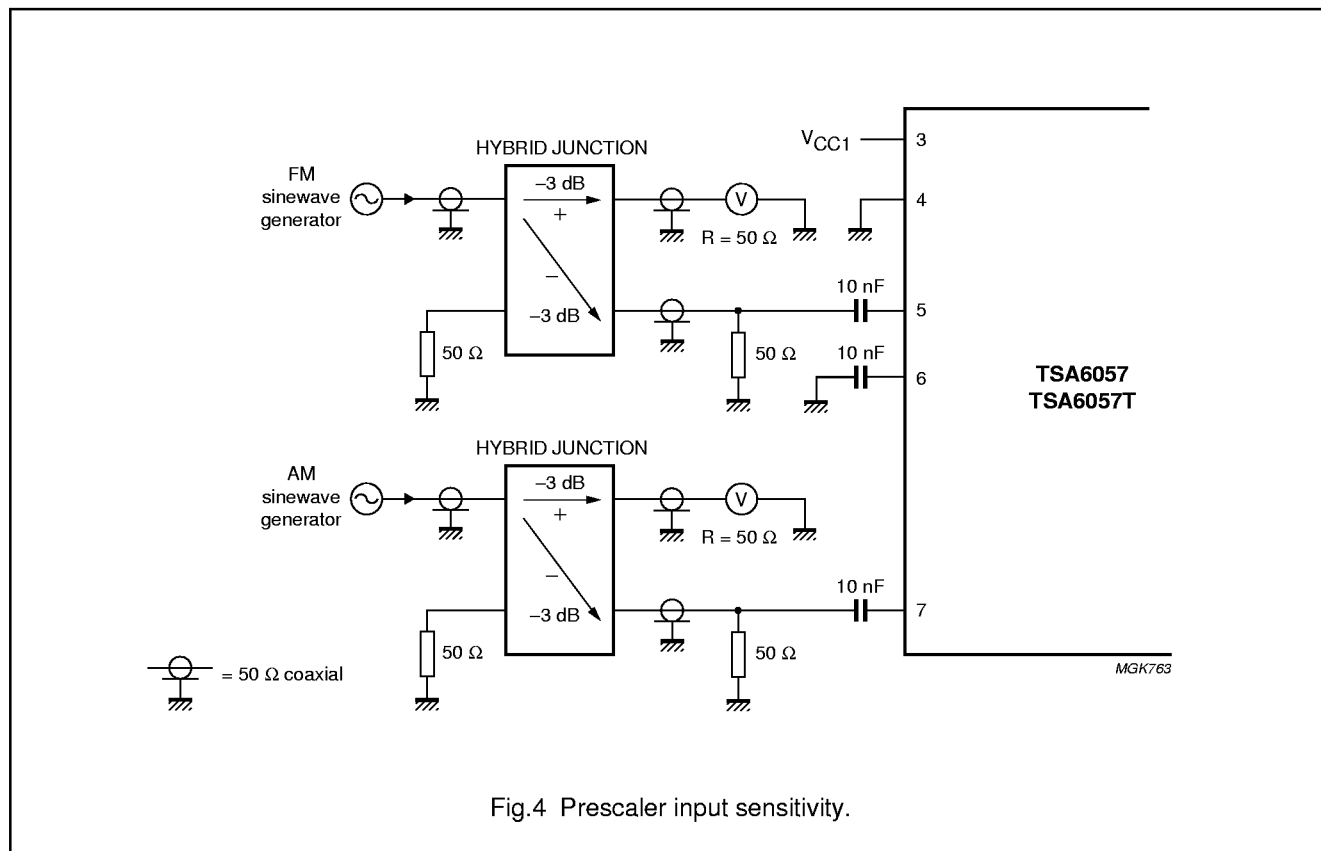
MGK762

Fig.3 Bit organization.

Radio tuning PLL frequency synthesizers

TSA6057; TSA6057T

Sensitivity measurement



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC1</sub>	supply voltage 1 (pin 3)		-0.3	+5.5	V
V <sub>CC2</sub>	supply voltage 2 (pin 16)		V <sub>CC1</sub>	12.5	V
P <sub>tot</sub>	total power dissipation		-	0.85	W
T <sub>amb</sub>	operating ambient temperature	version C1	-30	+85	°C
		version C8	-40	+85	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

## Radio tuning PLL frequency synthesizers

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**CHARACTERISTICS**

$V_{CC1} = 5\text{ V}$ ;  $V_{CC2} = 8.5\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{CC1}$	supply voltage 1 (pin 3)		4.5	5.0	5.5	V
$V_{CC2}$	supply voltage 2 (pin 16)	see Fig.6	$V_{CC1}$	8.5	12	V
$I_{CC1}$	supply current pin 3	no outputs loaded	12	20	28	mA
$I_{CC2}$	supply current pin 16	no outputs loaded version C1	0.7	1.0	1.5	mA
		version C8	0.2	0.5	1	mA
<b>I<sup>2</sup>C-bus inputs (SDA and SCL)</b>						
$V_{IH}$	input voltage HIGH		3.0	–	5.0	V
$V_{IL}$	input voltage LOW		–0.3	–	+1.5	V
$I_{IH}$	input current HIGH		–	–	10	$\mu\text{A}$
$I_{IL}$	input current LOW		–	–	10	$\mu\text{A}$
<b>SDA output open-collector</b>						
$V_{OL}$	output voltage LOW	$I_{OL} = 3.0\text{ mA}$	–	–	0.4	V
<b>AS input</b>						
$V_{IH}$	input voltage HIGH		3.0	–	5.0	V
$V_{IL}$	input voltage LOW		–0.3	–	+1.0	V
$I_{IH}$	input current HIGH		–	–	10	$\mu\text{A}$
$I_{IL}$	input current LOW		–	–	10	$\mu\text{A}$
<b>RF inputs (AM<sub>I</sub> and FM<sub>I</sub>)</b>						
$f_{iAM(max)}$	maximum input frequency on AM <sub>I</sub>		30	–	–	MHz
$f_{iAM(min)}$	minimum input frequency on AM <sub>I</sub>		–	–	0.512	MHz
$f_{iFM(max)}$	maximum input frequency on FM <sub>I</sub>		150	–	–	MHz
$f_{iFM(min)}$	minimum input frequency on FM <sub>I</sub>		–	–	30	MHz
<b>PIN AM<sub>I</sub></b>						
$V_{iAM(rms)}$	input voltage on AM <sub>I</sub> (RMS value)	$V_{iFM} = 0\text{ V}$ ; measured in Fig.4	30	–	500	mV
$R_{AM}$	resistance		–	5.9	–	k $\Omega$
$C_{AM}$	capacitance		–	2	–	pF
<b>PIN FM<sub>I</sub></b>						
$V_{iFM(rms)}$	input voltage on FM <sub>I</sub> (RMS value)	$V_{iAM} = 0\text{ V}$ ; measured in Fig.4	20	–	300	mV
$R_{FM}$	resistance		–	3.6	–	k $\Omega$
$C_{FM}$	capacitance		–	2	–	pF



## Radio tuning PLL frequency synthesizers

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Oscillator (XTAL1 and XTAL2)</b>						
R <sub>XTAL</sub>	resistance	4 MHz crystal; see Fig.5	–	–	150	Ω
<b>Programmable charge pump</b>						
I <sub>chp</sub>	output current to loop filter					
	bit CP = logic 0	version C1	3	5	7	μA
	bit CP = logic 0	version C8	3	5	9	μA
	bit CP = logic 1		400	500	600	μA
<b>Ripple rejection: f<sub>ripple</sub> = 100 Hz</b>						
RR1	20 log ΔV <sub>CC1</sub> /ΔV <sub>O</sub>		40	50	–	dB
RR2	20 log ΔV <sub>CC2</sub> /ΔV <sub>O</sub>		40	50	–	dB
<b>Band switch output (pin 8)</b>						
V <sub>OH</sub>	output voltage HIGH		–	–	12	V
V <sub>OL</sub>	output voltage LOW	I <sub>OL</sub> = 3 mA	–	–	0.8	V
I <sub>LO</sub>	output leakage current	V <sub>OH</sub> = 12 V	–	–	10	μA
<b>Reference frequency output (pin 9)</b>						
f <sub>ref</sub>	output frequency	4 MHz crystal	–	40	–	kHz
V <sub>OH</sub>	output voltage HIGH	I <sub>source</sub> = 5 μA	1.2	1.4	1.7	V
V <sub>OL</sub>	output voltage LOW		–	0.1	0.2	V
<b>Tuning voltage amplifier outputs</b>						
<b>AM OUTPUT (PIN 15)</b>						
V <sub>O(max)</sub>	maximum output voltage	I <sub>source</sub> = 0.5 mA; version C1	V <sub>CC2</sub> – 1.5	–	–	V
	maximum output voltage	I <sub>source</sub> = 0.5 mA; version C8	V <sub>CC2</sub> – 0.9	–	–	V
V <sub>O(min)</sub>	minimum output voltage	I <sub>sink</sub> = 1 mA	–	–	0.8	V
I <sub>source(max)</sub>	maximum output source current		0.5	–	–	mA
I <sub>sink(max)</sub>	maximum output sink current		1.0	–	–	mA
<b>FM OUTPUT (PIN 13)</b>						
V <sub>O(max)</sub>	maximum output voltage	I <sub>source</sub> = 0.5 mA; version C1	V <sub>CC2</sub> – 1.5	–	–	V
	maximum output voltage	I <sub>source</sub> = 0.5 mA; version C8	V <sub>CC2</sub> – 0.9	–	–	V
V <sub>O(min)</sub>	minimum output voltage	I <sub>sink</sub> = 1 mA	–	–	0.8	V
I <sub>source</sub>	maximum output source current		0.5	–	–	mA
I <sub>sink</sub>	maximum output sink current		1.0	–	–	mA
Z <sub>O(off)</sub>	impedance of switched off output		5	–	–	MΩ
I <sub>bias</sub>	input bias current (absolute value)		–	1	5	nA

Radio tuning PLL frequency synthesizers

TSA6057; TSA6057T

APPLICATION INFORMATION

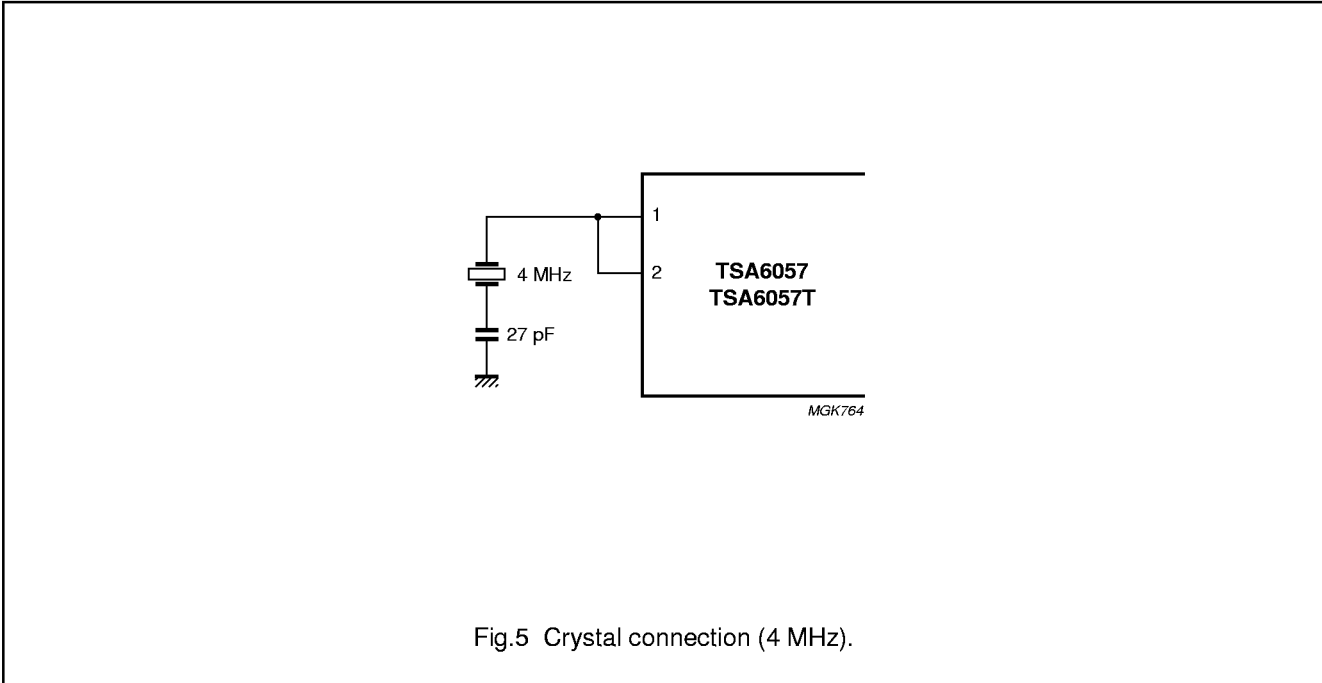


Fig.5 Crystal connection (4 MHz).

Radio tuning PLL frequency synthesizers

TSA6057; TSA6057T

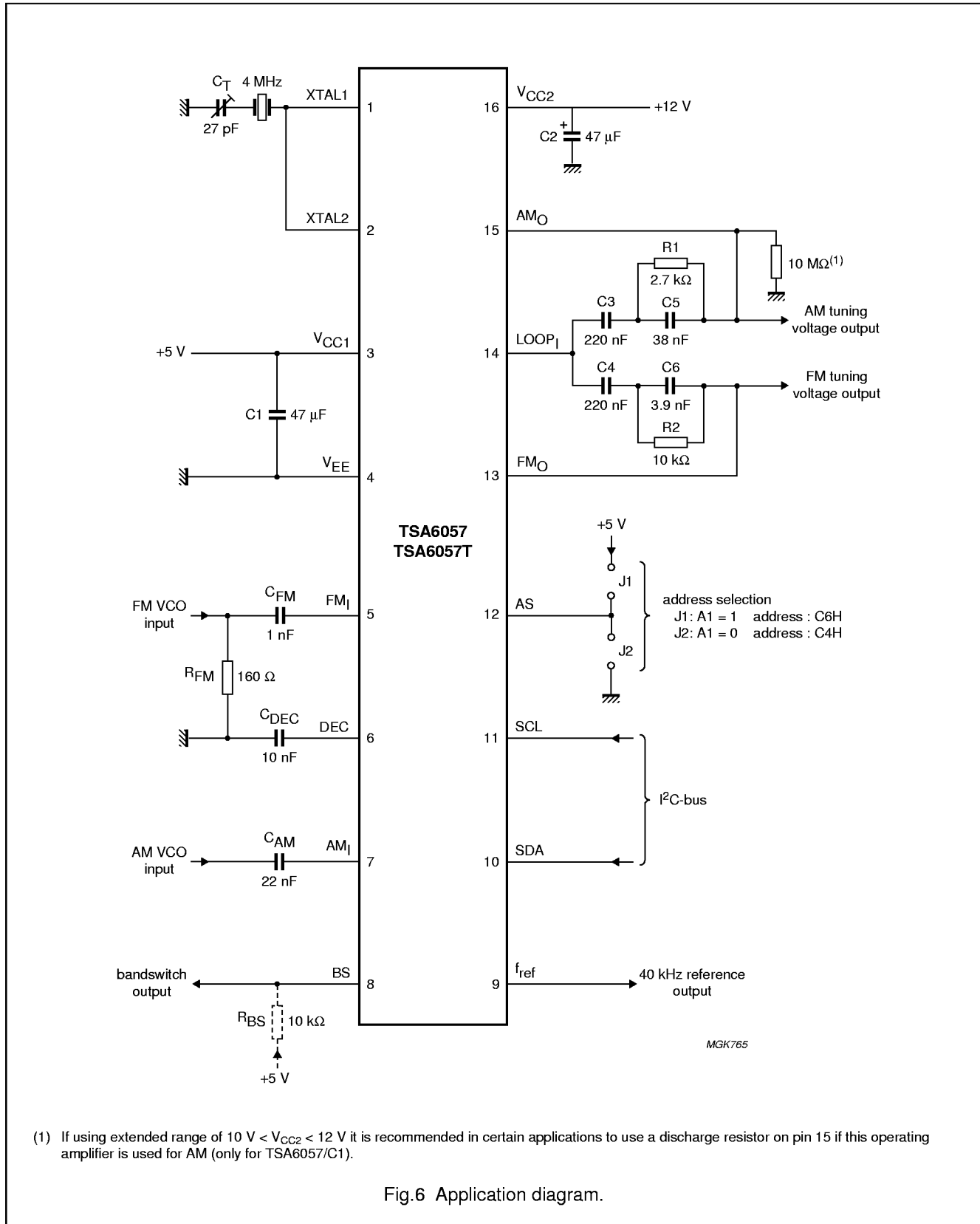


Fig.6 Application diagram.

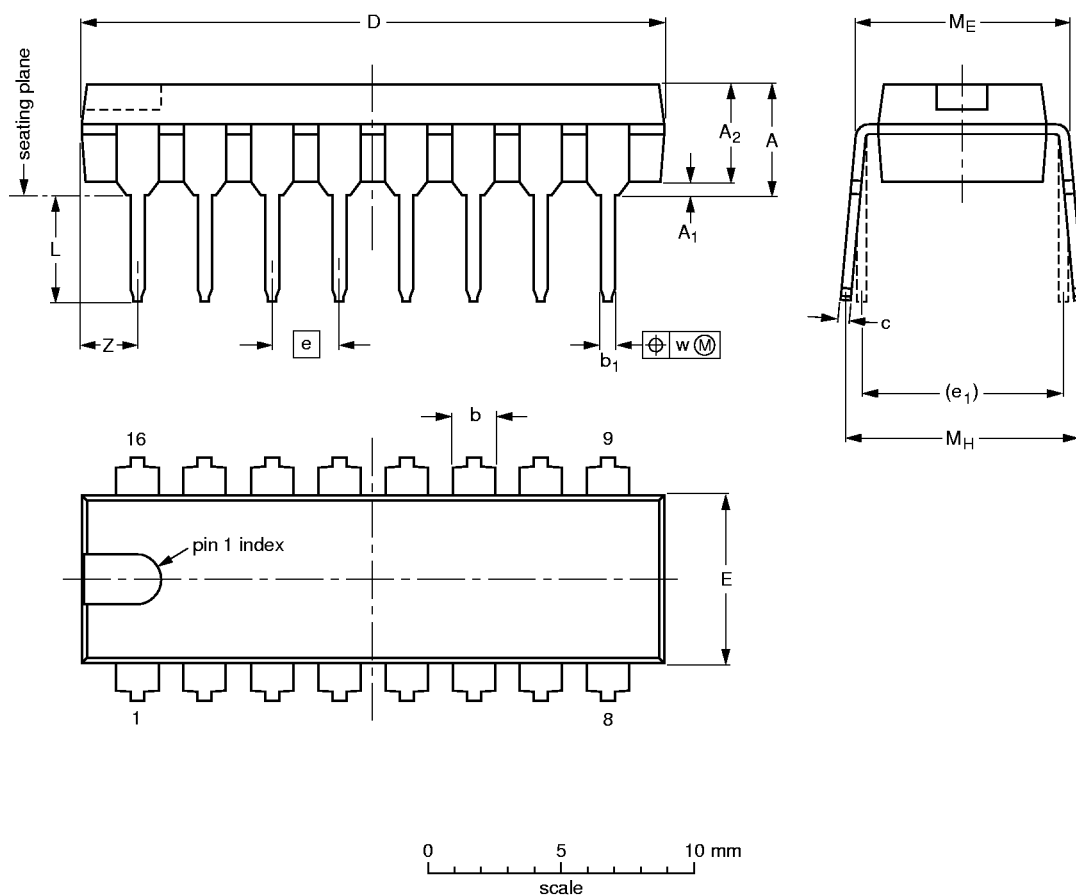
Radio tuning PLL frequency synthesizers

TSA6057; TSA6057T

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

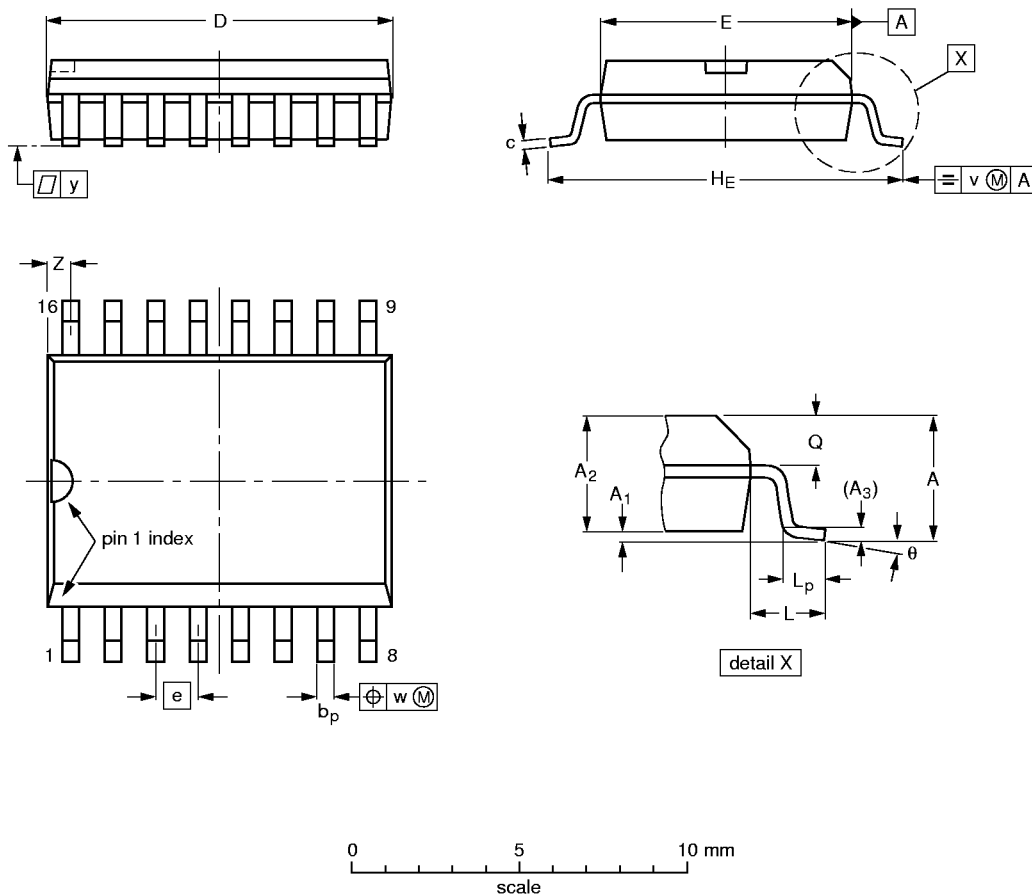
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT38-1	050G09	MO-001AE			92-10-02 95-01-19

Radio tuning PLL frequency synthesizers

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S016: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT162-1	075E03	MS-013AA			95-01-24 97-05-22

## Radio tuning PLL frequency synthesizers

## TSA6057; TSA6057T

### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### DIP

##### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### SO

##### REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

##### WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.