TMS 9927JL,NL VIDEO TIMER/CONTROLLER

990/9900 FAMILY MICROCOMPUTER COMPONENTS

- Second sourced by SMC as CRT5027
- TTL Compatibility
- Standard and Non-standard CRT Monitor Capability
- Scrolling Capability
- Interlaced and Non-interlaced Formatting
- Fully Programmable Display Format
  - Characters per data row
  - Data rows per frame
  - Raster scans per data row
  - Raster scans per frame
- Fully Programmable Monitor Format
  - Blanking
  - Horizontal sync
  - Vertical sync
  - Composite sync
- Two Programming Methods
  - Processor controlled
  - PROM on data bus
- Generation of Cursor Video
- N-channel Silicon-Gate Technology

DESCRIPTION

The TMS9927 is a single-chip video timer and controller produced using N-channel silicon-gate MOS technology. This 40-pin package contains the logic to generate all the timing signals for display of video data on standard or nonstandard CRT monitors in both interlaced or noninterlaced format. The only function not on the chip is the dot counter; which, due to high video frequencies, cannot easily be implemented with MOS technology. All the inputs and outputs are TTL compatible.

There are nine 8-bit control registers which are user programmable (see *Table 1*). Seven of the control registers are for horizontal and vertical formatting and two are for cursor address.

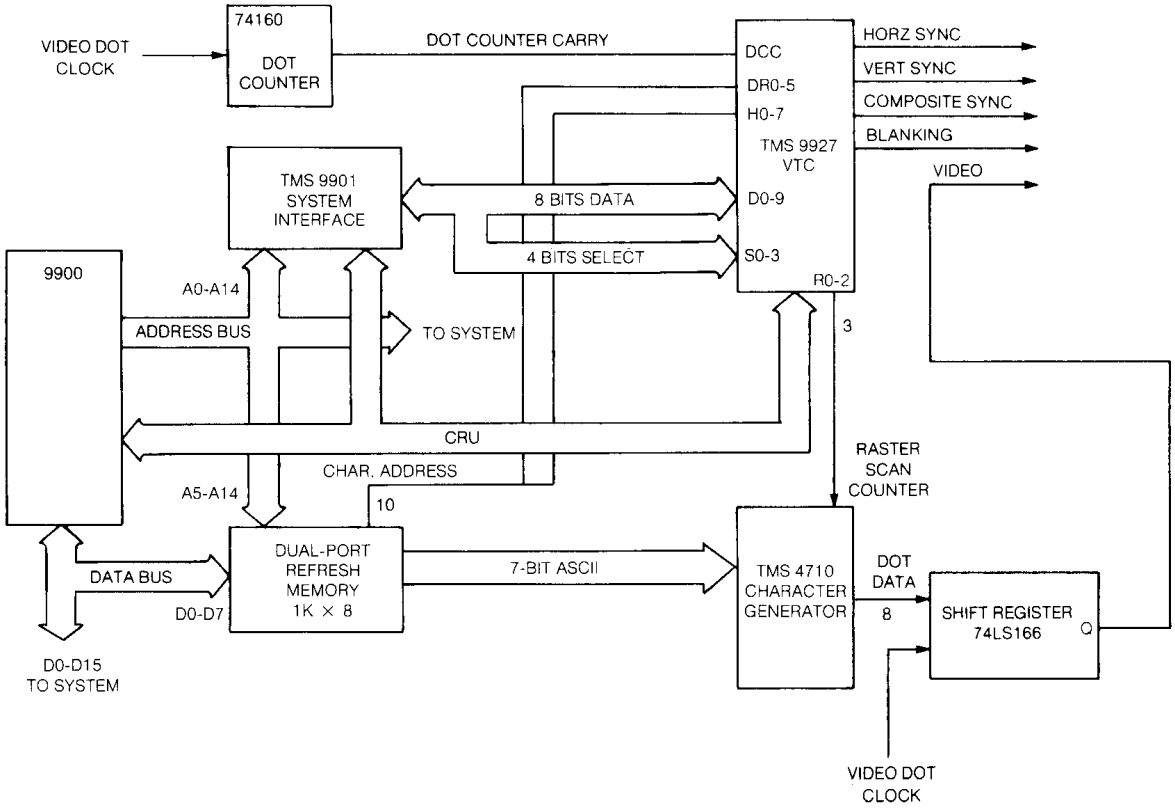


Figure 1. Typical System Interconnect

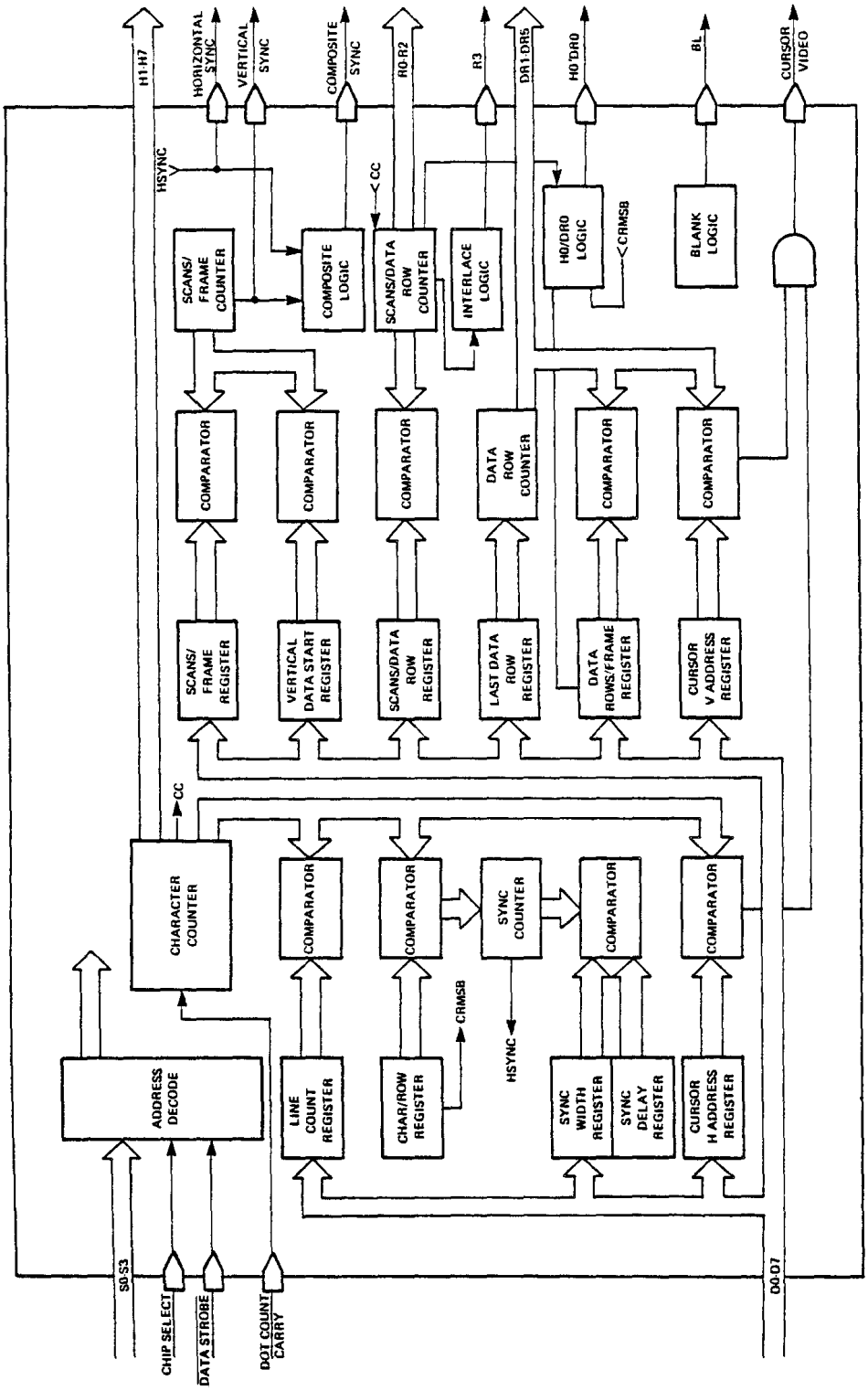
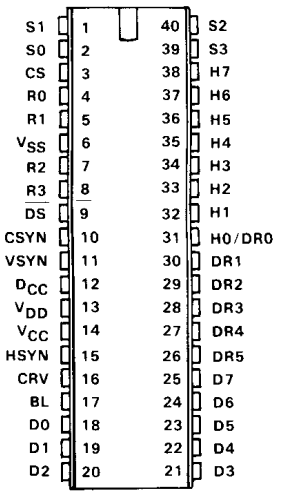


Figure 2. TMS 9927 Architecture.

TMS 9927 PIN FUNCTIONS

Signature	*I/O*	*Description*
D0-7	I/O	Data bus. Input bus for control words from microprocessor or PROM. Bidirectional bus for cursor address.
CS	I	Signals chip that it is being addressed
S0-3	I	Register address bits for selecting one of seven control registers or either of the cursor address registers
$\overline{DS}$	I	Strobes D0-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus
DCC	I	Carry from off chip dot counter establishing basic character clock rate.
H7-1	O	Character counter outputs.
R0-2	O	Three most significant bits of the Scan Counter: row select inputs to character generator.
H0/DR0	O	Pin definition is user programmable. Output is MSB of Character Counter if MSB of Characters/Data Row word is a "1", otherwise output is MSB of Data Row Counter
R3	O	Least significant bit of the scan counter. In interlaced mode this bit defines the odd or even field. In this way, odd scan lines of the character font are selected during the odd field and even scans during the even field
DR1-5	O	Data Row counter outputs
BL	O	Defines non active portion of horizontal and vertical scans.
HSYN	O	Initiates horizontal retrace
VSYN	O	Initiates vertical retrace
CSYN	O	Active in non-interlaced mode only. Provides a true RS-170 composite sync waveform.
V_{CC}	PS	+5 volt Power Supply
V_{DD}	PS	+12 volt Power Supply
V_{SS}	PS	Ground reference



FUNCTIONAL DESCRIPTION

Application Oriented Use

The TMS9927 interfaces to the central processor unit, if one is used, through the communications register unit (CRU) via a TMS9901, as shown in *Figure 2*, or it functions as a mapped memory device. The TMS9901 converts 8 bits of serial CRU data to parallel data to feed the TMS9927 data bus for loading the control registers. The CPU, using the CRU, decodes the high order bits of the address for the TMS9927 chip select and the four low order bits are connected directly to the TMS9927 Video Timer and Controller (VTC) for control register select. The character column (H1-H7) and row lines (DR1-DR5) combine to address the refresh RAM. The refresh RAM outputs the seven-bit ASCII code for the character to be displayed to the character generator, the TMS4710. The character generator uses the raster scan counter (R0-R2) to select which row of the dot matrix to output. A shift register then shifts the dot information out to the video terminal at the dot frequency.

The TMS9927 does have a self-load function as shown in *Figure 3*. It is accomplished by putting the self-load command on the VTC select lines and strobing DATA STROBE ($\overline{DS}$). This causes the TMS9927 to output address information on its row select lines to the control PROM (74S288). The outputs of the control PROM are loaded into the VTC control registers. There are two types of self-load: processor and nonprocessor. The nonprocessor self-load automatically starts the timing chain after load is completed. Processor self-load only causes a self-load and then waits for the start command from the processor. The select signals to the VTC which cause self-load should be applied for the entire duration of self-load.

Table 1. Select Decodes

S0	*S1*	*S2*	*S3*	*Command*	*Description*
0	0	0	0	Load Control Register 0	
0	0	0	1	Load Control Register 1	
0	0	1	0	Load Control Register 2	
0	0	1	1	Load Control Register 3	See *Table 2*
0	1	0	0	Load Control Register 4	
0	1	0	1	Load Control Register 5	
0	1	1	0	Load Control Register 6	
0	1	1	1	Processor Self Load	Command from processor instructing TMS 9927 to enter Self Load Mode
1	0	0	0	Read Cursor Row Address	
1	0	0	1	Read Cursor Character Address	
1	0	1	0	Reset	Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command.
1	0	1	1	Up Scroll	Increments address of first displayed data row on page. ie; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0.
1	1	0	0	Load Cursor Character Address	
1	1	0	1	Load Cursor Row Address	
1	1	1	0	Start Timing Chain	Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one TMS9927 the dot counter carry should be held low during the $\overline{DS}$ for this command.
1	1	1	1	Non-Processor Self Load	Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on S0-3 long enough to guarantee self load (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one TMS 9927, the Dot Counter Carry should be held low when this command is removed.

Note: During Self Load, the scan counter states corresponding to the nine load command addresses will load the appropriate register. Therefore if reseting of the cursor X and Y position registers is required via self load the PROM words for address 1100 and 1101 should be programmed as all zeros.

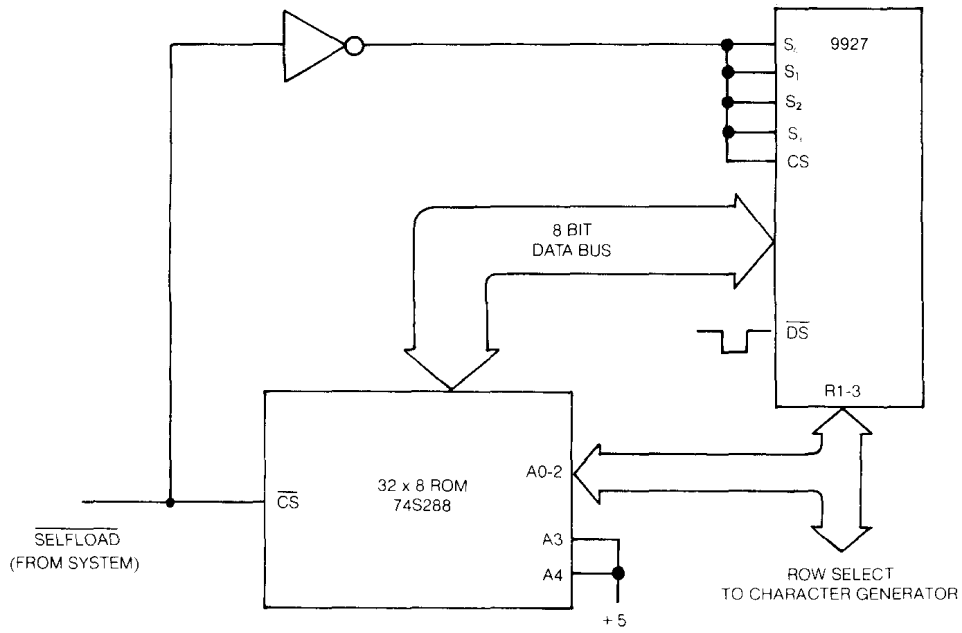


Figure 3. Self-load Command

ARCHITECTURE

General

The functional block illustrates the architecture of the TMS9927 video timer and controller. The architecture is designed to be as general as possible so that by programming the control registers properly almost any raster scan CRT can be controlled with this chip.

Select Lines

Lines S0-S3 are the select lines. They select the control register for loading via the data bus (DB0-DB7) and also select control functions for the device (see *Table 1*). The bit assignments for the nine control registers are given in *Table 2*. Notice that the cursor line address and the character address can both be read; therefore, the TMS9927 data bus must be bidirectional.

Table 2. TMS 9927 Control Registers.