ADVANCED INFORMATION

STEP-UP VOLTAGE CONVERTER

FEATURES

- **Guaranteed 0.9 V Operation**
- **Very Low Quiescent Current**
- **Internal Bandgap Reference**
- **High Efficiency MOS Switching**
- **Low Output Ripple**
- **Laser-Trimmed Output Voltage**
- **Laser-Trimmed Oscillator**
- **Undervoltage Lockout**
- **Regulation by Pulse Burst Modulation (PBM)**

APPLICATIONS

- **Battery Powered Systems**
- **Cellular Telephones**
- **Pagers**
- **Personal Communications Equipment**
- **Portable Instrumentation**
- **Portable Consumer Equipment**
- **Radio Control Systems**

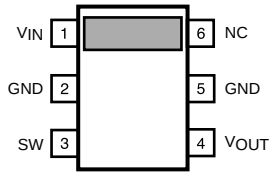
DESCRIPTION

The TK65020 low power step-up DC-DC converter is designed for portable battery-powered systems, capable of operating from a single battery cell down to 0.9 V. The TK65020 provides the power switch and the control circuit for a boost converter. The converter takes a DC input and boosts it up to a regulated 2.5 V output .

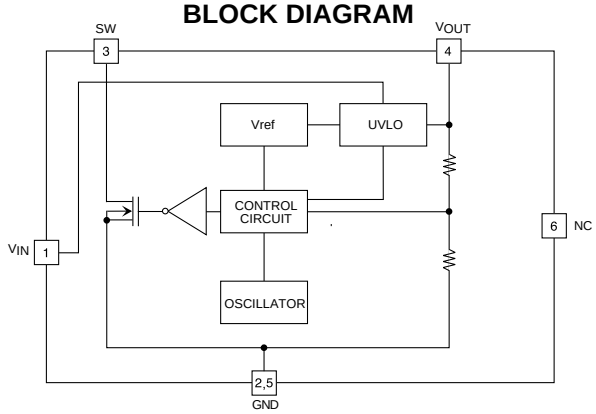
The output voltage is laser-trimmed. An internal Undervoltage Lockout (UVLO) circuit is utilized to prevent the inductor switch from remaining in the “on” mode when the battery voltage is too low to permit normal operation. Pulse Burst Modulation (PBM) is used to regulate the voltage at the V_{OUT} pin of the IC. PBM is the process in which an oscillator signal is gated or not gated to the switch drive each period. The decision is made just before the start of each cycle and is based on comparing the output voltage to an internally-generated bandgap reference. The decision is latched, so the duty ratio is not modulated within a cycle. The average duty ratio is effectively modulated by the “bursting” and skipping of pulses which can be seen at the SW pin of the IC. Special care has been taken to achieve reliability through the use of Oxide, double Nitride passivation. The TK65020 is available in a miniature 6-pin SOT-23L-6 surface mount package.

For other output levels, please refer to the TK651xx and TK652xx Toko series of step-up converters.

TK65020



BLOCK DIAGRAM



ORDERING INFORMATION

TK65020MTL

Tape/Reel Code

TAPE/REEL CODE
TL: Tape Left

ABSOLUTE MAXIMUM RATINGS

All Pins Except SW and GND ..... 6 V
SW Pin ..... 9 V
Power Dissipation (Note 1) ..... 400 mA
Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range .....-20 to +80 °C
Junction Temperature ..... 150 °C

TK65020 ELECTRICAL CHARACTERISTICS

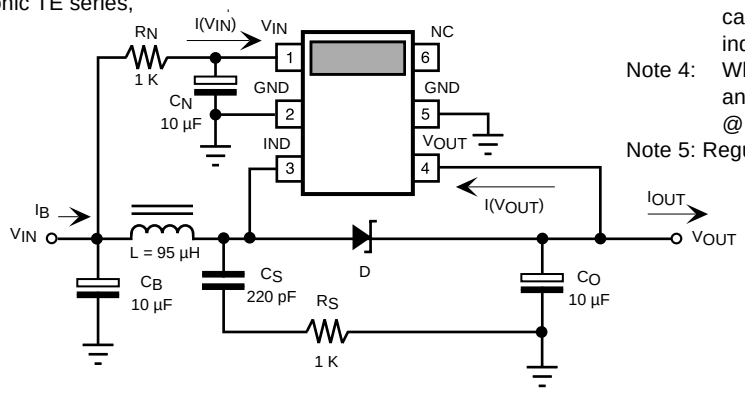
Over operating temperature range and supply voltage range, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Supply Voltage		0.90		1.60	V
$I_{B(Q)}$	No Load Battery Current (Note 3)	V_{IN} = 1.3 V, I_{OUT} = 0 mA, T_A = 25 ° C		41	62	µA
$I(V_{IN})$	Quiescent Current into V_{IN} Pin	V_{IN} = 1.3 V, I_{OUT} = 0 mA, T_A = 25 ° C		11	20	µA
$I(V_{OUT})$	Quiescent Current into V_{OUT} Pin	V_{IN} = 1.3 V, I_{OUT} = 0 mA		12	20	µA
f_{OSC}	Internal Oscillator Frequency	V_{IN} = 1.3 V, I_{OUT} = 0 mA	70	83	102	kHz
$\Delta f_{OSC}/\Delta T$	Temperature Stability of Oscillator	V_{IN} = 1.3 V, No Pulse Skipping		0.1		%/° C
D_{OSC}	On-time Duty Ratio of Oscillator	T_A = 25 ° C	45	50	55	%
$V_{OUT(REG)}$	Regulation Threshold of V_{OUT}	T_A = 25 ° C	2.38	2.50	2.58	V
$\Delta V_{OUT}/\Delta T$	Temperature Stability of $V_{OUT(REG)}$	V_{IN} = 1.3 V, I_{OUT} = 0 mA		100		mV
$\Delta V_{OUT(LOAD)}$	Load Regulation of $V_{OUT(REG)}$	V_{IN} = 1.3 V, I_{OUT} = 0 to 4 mA		0	50	mV
$\Delta V_{OUT(LINE)}$	Line Regulation of $V_{OUT(REG)}$	ΔV_{IN} = 0.25 V	-20		30	mV
$R_{SW(ON)}$	On-resistance of SW Pin	$T_A \geq$ 2.4		1.0		V
EFF	Converter Efficiency (Notes 3,4)	V_{IN} = 1.3 V, I_{OUT} = 6 mA, L = 95 µH, 3DF Coil		76		%
V_{ULV}	Undervoltage Lockout Voltage	T_A = 25 ° C, (Note 5)		0.45	0.79	V
$I_{OUT(MAX)}$	Maximum I_{OUT} for Converter (Notes 2,4)	V_{IN} = 1.1 V, T_A = 25 ° C, L = 95 µH, 3DF Coil	5	8.0		mA
		V_{IN} = 1.3 V, T_A = 25 ° C, L = 95 µH, 3DFCoil	9	15.0		mA
		V_{IN} = 1.1 V, T_A = 25 ° C, L = 39 µH, D73 Coil		19.8		mA
		V_{IN} = 1.3 V, T_A = 25 ° C, L = 39 µH, D73 Coil		38.0		mA

Note 1: Derate at 0.8 mW/ºC for operation above T_A = 25 ºC ambient temperature, when heat conducting copper foil path is maximized on the printed circuit board. When this is not possible, a derating factor of 1.6 mW/ °C must be used.

BENCH TEST CIRCUIT

Inductor L: Toko A682AE-014 or equivalent
Diode D: LL103A or equivalent
Capacitors C_N:C_O:C_B: Panasonic TE series, ECS-TOJY106R

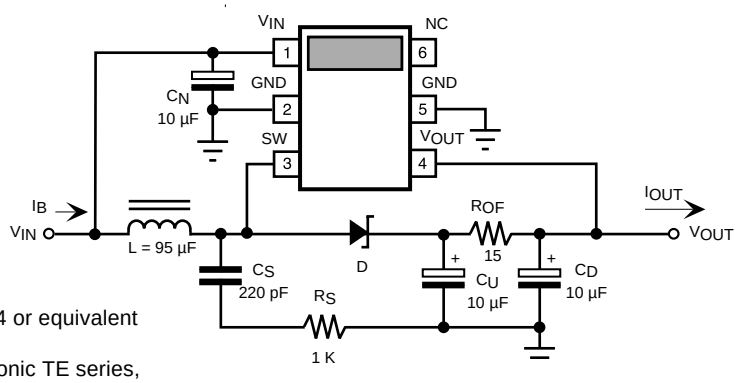


Note 2: Maximum load current depends on inductor value and input voltages.
Note 3: Output ripple depends on filter capacitor values, ESRs and the inductor value.
Note 4: When using specified Toko inductor and Schottky diode with V_F = 0.45 V @ 100 mA.
Note 5: Regulation not guaranteed

The Bench Test Circuit is used most of the time to measure the typical (typ.) values in the Electrical Characteristics section, and make the Typical Performance graphs.

Note: In measuring the oscillator frequency and the Max I_{OUT} on the bench, the converter was loaded until “no pulse skipping” mode was achieved.

FINAL TEST CIRCUIT



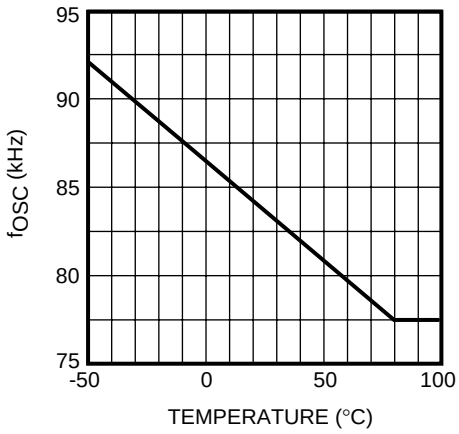
Inductor L: Toko A682AE-014 or equivalent
Diode D: LL101
Capacitors C_N:C_U:C_D: Panasonic TE series, ECS-TOJY106R

Above is the Final Test Circuit through which each of the production parts must pass. In this test circuit, the part is tested against the specification limits in the data sheet (the min. and max. values in the Electrical Characteristics) at room temperature, and is rejected if the tested values are outside the minimum (min.) and maximum (max.) values.

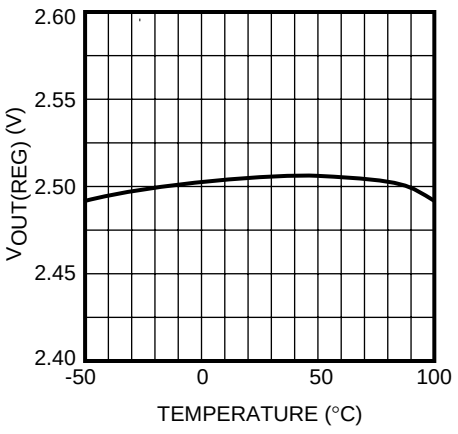
TYPICAL PERFORMANCE CHARACTERISTICS

TK65020

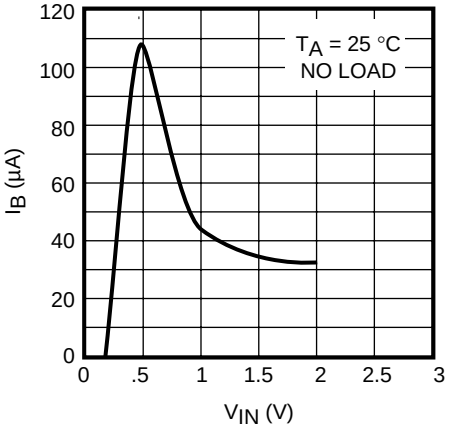
OSCILLATOR FREQUENCY vs. TEMPERATURE



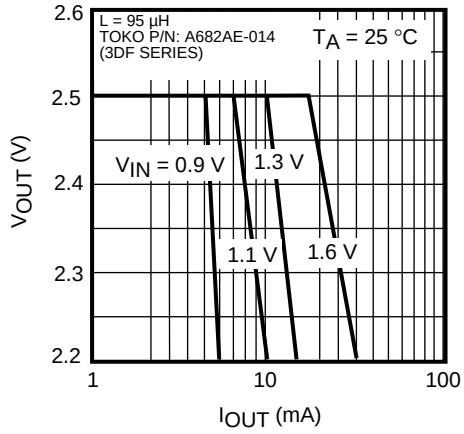
OUTPUT REGULATION VOLTAGE vs. TEMPERATURE



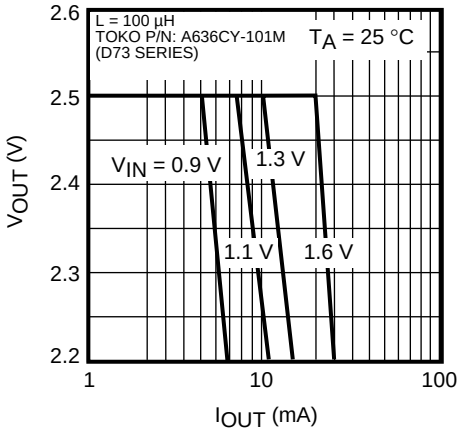
BATTERY CURRENT vs. INPUT VOLTAGE



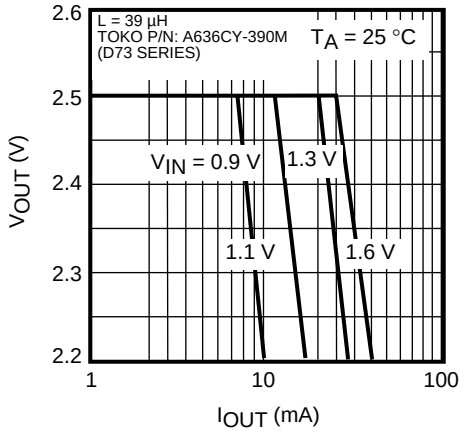
OUTPUT VOLTAGE vs. LOAD CURRENT



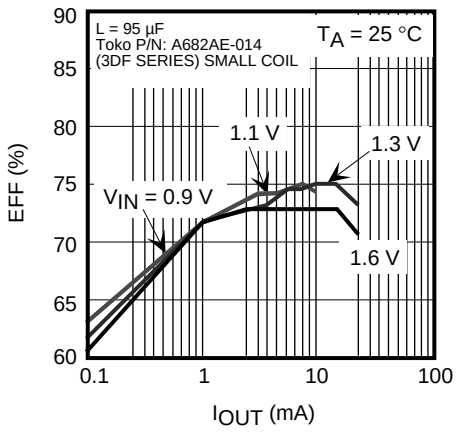
OUTPUT VOLTAGE vs. LOAD CURRENT



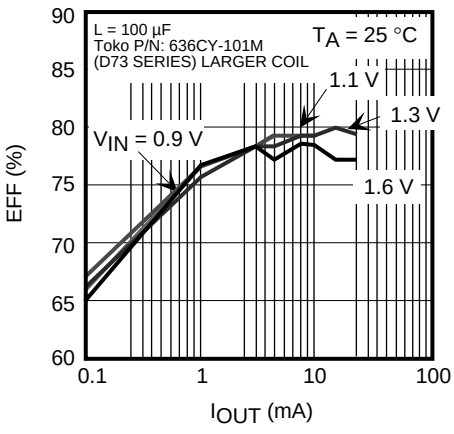
OUTPUT VOLTAGE vs. LOAD CURRENT



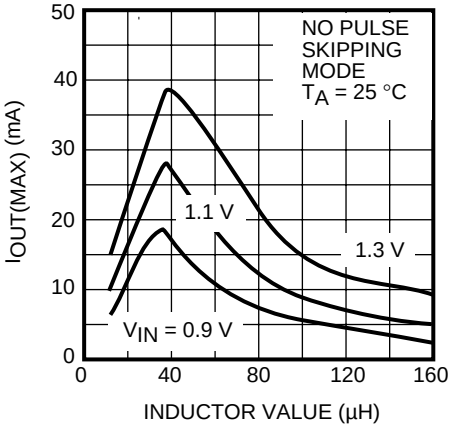
EFFICIENCY vs. LOAD CURRENT



EFFICIENCY vs. LOAD CURRENT



MAXIMUM OUTPUT CURRENT vs. INDUCTOR VALUE (µH)



SINGLE-CELL APPLICATION

The TK65020 is a boost converter control IC with the power MOSFET switch built into the device. It operates from a single battery cell and steps up the output voltage to a regulated 2.5 V. The device operates at a fixed nominal clock frequency of 83 kHz.

In its simplest form, a boost power converter using the TK65020 requires only three external components: an inductor, a diode, and a capacitor.

The analysis is easier to follow when referencing the simple boost circuit below.

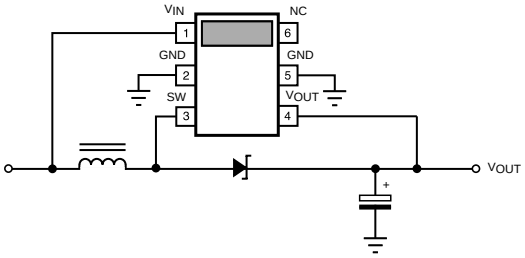


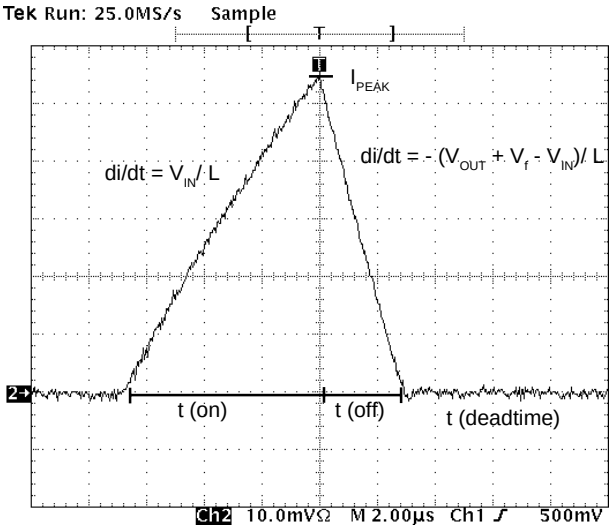
FIGURE 1: SIMPLE BOOST CONVERTER

THEORY OF OPERATION

The converter operates with one terminal of an inductor connected to the DC input and the other terminal connected to the switch pin of the IC. When the switch is turned on, the inductor current ramps up. When the switch is turned off (or "lets go" of the inductor), the voltage flies up as the inductor seeks out a path for its current. A diode, also connected to the switching node, provides a path of conduction for the inductor current to the boost converter's output capacitor. The TK65020 monitors the voltage of the output capacitor and has a 2.5 V threshold at which the converter switching becomes deactivated. So the output capacitor charges up to 2.5 V and regulates there, provided that no more current is drawn from the output than the inductor can provide**. The primary task, then, in designing a boost converter with the TK65020 is to determine the inductor value (and its peak current rating to prevent inductor core saturation problems) which will provide the amount of current needed to guarantee that the output voltage will be able to maintain regulation up to a specified maximum load current.** Secondary necessary tasks also include choosing the diode and the output capacitor. Then the snubber and filtering component values (consult the "Ripple and Noise Considerations" section) can be determined if needed or desired.

The TK65020 runs with a fixed oscillator frequency and it regulates by applying or skipping pulses to the internal power switch. This regulation method is called Pulse Burst Modulation (PBM).

ANALYSIS OF SWITCHING CYCLE



Above is the input or inductor current waveform over a switching cycle.

From an oscillator standpoint, the switching cycle consists of only an on-time and an off-time. But from an inductor current standpoint, the switching cycle breaks down into three important sections: on-time, off-time, and deadtime. The on-time of the switch and the inductor current are synonymous. During the on-time, the inductor current increases. During the off-time, the inductor current decreases as it flows into the output. When the inductor current reaches zero, that marks the end of the inductor current off-time. For the rest of the cycle, the inductor current remains at zero. Since no energy is being either stored or delivered, that remaining time is called "deadtime." This mode of the inductor current decaying to zero every cycle is called "discontinuous mode." In summary, energy is stored in the inductor during on-time, delivered to the output during off-time, and remains at zero during deadtime.

SINGLE-CELL APPLICATION (CONT.)

The output current of the boost converter comes from the second half of the input current triangle waveform (averaged over the period or multiplied by the frequency) given by the equation:

$$I_{OUT} = [I_{PK} \times t(off)] \times f / 2$$

and:

$$I_{PK} = (V_{IN} / L) \times t(on) = V_{IN} D / f L$$

and:

$$\begin{aligned} t(off) &= I_{PK} / [(V_{OUT} + V_F - V_{IN}) / L] \\ &= (V_{IN} D / f L) / [(V_{OUT} + V_F - V_{IN}) / L] \\ &= V_{IN} D / f (V_{OUT} + V_F - V_{IN}) \end{aligned}$$

therefore:

$$I_{OUT} = (V_{IN})^2 (D)^2 / 2 f L (V_{OUT} + V_F - V_{IN})$$

which derives Equation 1 of the next section.

INDUCTOR SELECTION

It is under the condition of lowest input voltage that the boost converter output current capability is the lowest for a given inductance value. Three other significant parameters with worst-case values for calculating the inductor value are: highest switching frequency, lowest duty ratio (of the switch on-time to the total switching period), and highest diode forward voltage. Other parameters which can affect the required inductor value, but for simplicity will not be considered in this first analysis are: the series resistance of the DC input source (i.e., the battery), the series resistance of the internal switch, the series resistance of the inductor itself, ESR of the output capacitor, input and output filter losses, and snubber power loss.

The converter reaches maximum output current capability when the switch runs at the oscillator frequency, without pulses being skipped. The output current of the boost converter is then given by the equation:

$$I_{OUT} = \frac{(V_{IN})^2 (D)^2}{2 f L (V_{OUT} + V_F - V_{IN})} \quad (1)$$

where "V_{IN}" is the input voltage, "D" is the on-time duty ratio of the switch, "*f*" is the switching (oscillator) frequency, "L" is the inductor value, "V_{OUT}" is the output voltage, and "V_F" is the diode forward voltage. It is important to note that Equation 1 makes the assumption stated in Equation 2:

$$V_{IN} \le (V_{OUT} + V_F)(1 - D) \quad (2)$$

The implication from Equation 2 is that **the inductor will operate in discontinuous mode**.

Using worst-case conditions, the inductor value can be determined by simply transforming the above equation in terms of "L":

$$L_{(MIN)} = \frac{V_{IN(MIN)}^2 D_{(MIN)}^2}{2 f_{(MAX)} I_{OUT(MAX)} [V_{OUT(MIN)} + V_{F(MAX)} - V_{IN(MIN)}]} \quad (3)$$

where "$V_{F(MAX)}$" is best approximated by the diode forward voltage at about two-thirds of the peak diode current value. The peak diode current is the same as the peak input current, the peak switch current, and the peak inductor current. The formula is:

$$I_{PK} = \frac{V_{IN} D}{f L} \quad (4)$$

Some reiteration is implied because "L" is a function of "V_F" which is a function of "I_{PK}" which, in turn, is a function of "L". The best way into this loop is to first approximate "V_F", determine "L", determine "I_{PK}", and then determine a new "V_F". Then, if necessary, reiterate.

When selecting the actual inductor, it is necessary to make sure that the peak current rating of the inductor (i.e., the current which causes the core to saturate) is greater than the maximum peak current the inductor will encounter. To determine the maximum peak current, use Equation 4 again, but this time use maximum values for "V_{IN}" and "D", and minimum values for "*f*" and "L".

It may also be necessary when selecting the inductor to check the rms current rating of the inductor. Whereas peak current rating is determined by core saturation, rms current

SINGLE-CELL APPLICATION (CONT.)

rating is determined by wire size and power dissipation in the wire resistance. The inductor rms current is given by:

$$I_{L(RMS)} = I_{PK} \sqrt{D + \frac{\frac{I_{PK}\, f\, L}{V_{OUT} + V_F - V_{IN}}}{3}} \quad (5)$$

where "I_{PK}" is the same maximized value that was just used to check against inductor peak current rating, and the term in the numerator within the radical that is added to the [on-time] duty ratio, "D", is the off-time duty ratio.

Toko America, Inc. can offer a miniature matched magnetic solution in a wide range of inductor values and sizes to accommodate varying power level requirements. The following series of Toko inductors work especially well with the TK65020 : 10RF, 12RF, 3DF, D73, and D75. The 5CA series can be used for isolated-output applications, although such design objectives are not considered here.

OTHER CONVERTER COMPONENTS

In choosing a diode, parameters worthy of consideration are: forward voltage, reverse leakage, and capacitance. The biggest efficiency loss in the converter is due to the diode forward voltage. A Schottky diode is typically chosen to minimize this loss. Possible choices for Schottky diodes are: LL103A from ITT MELF case; 1N5017 from Motorola (through hole case); MBR0530 from Motorola (surface mount) or 15QS02L from Nihon EC (surface mount).

Reverse leakage current is generally higher in Schottkys than in pin-junction diodes. If the converter spends a good deal of the battery lifetime operating at very light load (i.e., the system under power is frequently in a standby mode), then the reverse leakage current could become a substantial fraction of the entire average load current, thus degrading battery life. So don't dramatically oversize the Schottky diode if this is the case.

Diode capacitance isn't likely to make much of an undesirable contribution to switching loss at this relatively low switching frequency. It can, however, increase the snubber (look in the "Ripple and Noise Considerations" section) dissipation requirement.

The output capacitor, the capacitor connected from the diode cathode to ground, has the function of averaging the current pulses delivered from the inductor while holding a relatively smooth voltage for the converter load. Typically, the ripple voltage cannot be made smooth enough by this capacitor alone, so an output filter is used. In any case, to minimize the dissipation required by the output filter, the output capacitor should still be chosen with consideration to smoothing the voltage ripple. This implies that its Equivalent Series Resistance (ESR) should be low. This usually means choosing a larger size than the smallest available for a given capacitance. To determine the peak ripple voltage on the output capacitor for a single switching cycle, multiply the ESR by the peak current which was calculated in Equation 4. ESR can be a strong function of temperature, being worst-case when cold. The capacitance should be capable of integrating a current pulse with little ripple. Typically, if a capacitor is chosen with reasonably low ESR, and if the capacitor is the right type of capacitor for the application (typically aluminum electrolytic or tantalum), then the capacitance will be sufficient.

ESR and printed circuit board layout have strong influence on RF interference levels. Special care must be taken to optimize PCB layout and component placement.

THE BENEFITS OF INPUT FILTERING

In practice, it may be that the peak current (calculated in Equation 4) flowing out of the battery and into the converter will cause a substantial input ripple voltage dropped across the resistance inside the battery. This becomes a more likely case for cold temperature (when battery series resistance is higher), higher load rating converters (whose inductors must draw higher peak currents), and when the battery is undersized for the peak current application.

While the simple analysis used a parameter "V_{IN}" to represent the converter input voltage in the equations, one may not know what "V_{IN}" value to use if it is delivered by a battery that allows high ripple to occur. For example, assume that the converter draws a peak current of 100 mA for a 1 V input, and assume that the input is powered by a partially discharged AAA battery which might have a series resistance of 2 Ohms at 0 °C. (Environmentally clean, so called "green" batteries tend to have higher source resistance than their "unclean" predecessors). If such partially discharged battery voltage is 1 V without load, the converter battery voltage will sag to about 0.8 V during the on-time. This can cause two problems: 1) with the effective input voltage to the converter reduced in this way, the converter output capacity will decrease, 2) if the same battery is powering the TK65020 at the V_{IN} pin (i.e., the

SINGLE-CELL APPLICATION (CONT.)

normal case), then the IC may become inoperable due to insufficient V_{IN}. This is why the application test circuit features an RC filter into the V_{IN} pin. The current draw is very small, so the voltage drop across this filter resistor is negligible. The filter serves to average out the input ripple caused by the battery resistance. Note that this filter is optional, and the net effect of its use is the extension of battery life by allowing the battery to be discharged more deeply.

A more power-efficient method comes at the price of a large capacitor. This can be placed in parallel with the battery to help channel the converter current pulses away from the battery. The capacitor must have low ESR compared to the battery resistance in order to accomplish this effectively.

Still another solution is to filter the DC input with an LC filter. However, it is more likely that the filter will be either too large or too lossy. It is of questionable benefit to smooth the input if the DC loss through the filter is large.

Assuming that input ripple voltage at the battery terminal and converter input is large, and that we filter the V_{IN} pin of the IC as in the test circuit, then the parameter "V_{IN}" in the previous equations is not usable, and we will need to use parameters to represent both the source voltage *and* the source resistance.

SWITCH ON-RESISTANCE, INDUCTOR WINDING RESISTANCE, AND CAPACITANCE ESR

The on-resistance of the TK65020's internal switch is about 1 Ohm maximum. Using the previously stated example of 100 mA peak current, the voltage drop across the switch would reach 100 mV during the on-time. This subtracts from the voltage which is impressed across the inductor to store energy during the on-time. As a result, less energy is delivered to the output during the off-time.

If the winding resistance of the inductor increases to 1 Ohm or greater, the voltage drop across the winding resistance also subtracts from the voltage used to store energy in the core. This causes a degradation in efficiency.

As the inductor delivers energy into the output capacitor during the off-time, its current decays at a rate proportional to the voltage drop across it. The idealized equations assume that the voltage at the switching node is clamped at a diode drop above the output voltage. However, the ESR of the output capacitor can increase the voltage drop across the inductor by the additional voltage dropped across the ESR when the peak current flows in it. For example, the voltage across a capacitor with an ESR of 2 Ohms (not unusual at cold temperature) would jump by 200 mV when 100 mA peak current began to flow in it. This extra voltage drop would cause the inductor current to ramp down more quickly, thus depleting the available output current. Possible choices for low ESR capacitors are: Panasonic TE series (surface mount); AVX TPS series (surface mount); Matsuo 267 series (surface mount); Sanyo OS-CON series.

RIPPLE AND NOISE CONSIDERATIONS

The filtered test circuit of the TK65020 is shown below in Figure 2.

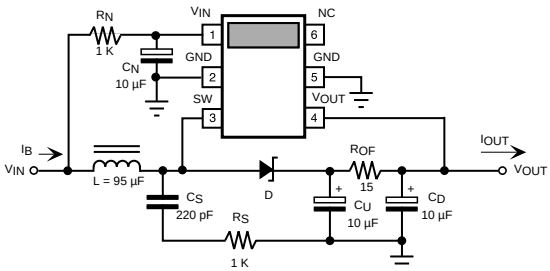


FIGURE 2: FILTERED TEST CIRCUIT

SINGLE-CELL APPLICATION (CONT.)

Compared to the simple boost circuit, this Filtered Test Circuit adds the following circuitry: the RC filter into the V_{IN} pin, the RC snubber, the RC filter at the converter output, and the pull-up resistor to the LOI pin.

The RC filter at the V_{IN} pin is used only to prevent the ripple voltage at the battery terminals from prematurely causing undervoltage lockout of the IC. This is only needed when the inductor value is relatively small and the battery resistance is relatively high and the V_{IN} range must extend as low as possible.

The snubber (optional) is composed of a series RC network from the switch pin to ground (or to the output or input if preferred). Its function is to dampen the resonant LC circuit which rings during the inductor current deadtime. When the current flowing in the inductor through the output diode decays to zero, the parasitic capacitance at the switch pin from the switch, the diode, and the inductor winding has energy which rings back into the inductor, flowing back into the battery. If there is no snubbing, it is feasible that the switch pin voltage could ring below ground. Although the IC is well protected against latch-up, this ringing may be undesirable due to radiated noise. To be effective, the snubber capacitor should be large (e.g., 5 ~ 20 times) in comparison to the parasitic capacitance. If it is unnecessarily large, it dissipates extra energy every time the converter switches. The resistor of the snubber should be chosen such that it drops a substantial voltage as the ringing parasitic capacitance attempts to pull the snubber capacitor along for the ride. If the resistor is too small (e.g., zero), the snubber capacitance just adds to the ringing energy. If the resistor is too large (e.g., infinite), it effectively disengages the snubber capacitor from fighting the ringing.

The RC filter at the converter output attenuates the conducted noise; the converter may not require this.

Finally, the pull-up resistors at the LOI pin are needed only if this output signal is used. Most of this circuitry which appears in the test circuit has been added to minimize ripple and noise effects. But when this is not critical, the circuit can be minimized.

When any DC-DC converter is used to convert power in RF circuits (e.g., pagers) the spectral noise generated by the converter, whether conducted or radiated, is of concern. The oscillator of the TK65020 has been trimmed and stabilized to 83 +/- 4 kHz with the intention of greatly minimizing interference at the common IF frequency of 455 kHz.

In comparison with conventional IC solutions, where the oscillator frequency is not controlled tightly, the TK65020 can achieve as much as 20-30 dB improvements in RF interference reduction by means of its accurately controlled oscillator frequency. This IF frequency is halfway between the fifth and sixth harmonics of the oscillator. The fifth harmonic of the maximum oscillator frequency and the sixth harmonic of the minimum oscillator frequency still leave a 39 kHz band centered around 455 kHz, within which a fundamental harmonic of the oscillator will not fall. Since the TK65020 operates by Pulse Burst Modulation (PBM), the switching pattern can be a subharmonic of the oscillator frequency. The simplest example, and the one to be avoided the most, is that of the converter causing every other oscillator pulse to be skipped. This means that the switching pattern would have a fundamental frequency of one-half the oscillator frequency, or 41.5 kHz. This is the eleventh harmonic, which lands at 456.5 kHz, right in the IF band. Fortunately, the energy is rather weak at the eleventh harmonic. Even more fortunate is the ease with which that regulation mode is avoided.

The internal regulator comparator has a finite hysteresis. When an additional filter is used (e.g., the RC filter of the test circuit, or an LC filter), the ripple at the regulation node is minimized. This limits the rate at which the oscillator can be gated. In practice, this means that rather than exhibiting a switching pattern of skipping every other oscillator pulse, it would be more likely to exhibit a switching pattern of three or four pulses followed by the same number of pulses skipped. Although this also tends to increase the output ripple, it is low frequency and has low magnitude (e.g., 10 kHz and 10 mV) which tends to be of little consequence.

SINGLE-CELL APPLICATION (CONT.)

HIGHER-ORDER DESIGN EQUATION

$$I_{OUT} = \frac{V_{BB}^2 \; D \left(\frac{D}{2f\,L}\right)\left[1 - \frac{D}{2f\,L}(R_S + R_L + R_{SW})\right]^2}{V_{OUT} + R_{OF}I_{OUT(TGT)} + \frac{D}{2f\,L}(V_{BB}R_U) + V_F - V_{BB}\left(1 - \frac{D}{2f\,L}(R_S + R_L)\right)} - \frac{fC_S[V_{BB}^2 + (V_{OUT} + V_F)^2 + (V_{OUT} + V_F - V_{BB})^2]}{2(V_{OUT} + V_F)}$$

The equation above was developed as a closed form approximation. In order to allow a closed form approximation, the design variable that required the least approximation was "I_{OUT}," as opposed to "L".

The approximations made in the equation development have the primary consequence that error is introduced as resistive losses become relatively large. As it is normally a practical design goal to ensure that resistive losses will be relatively small, this seems acceptable. The variables used are:

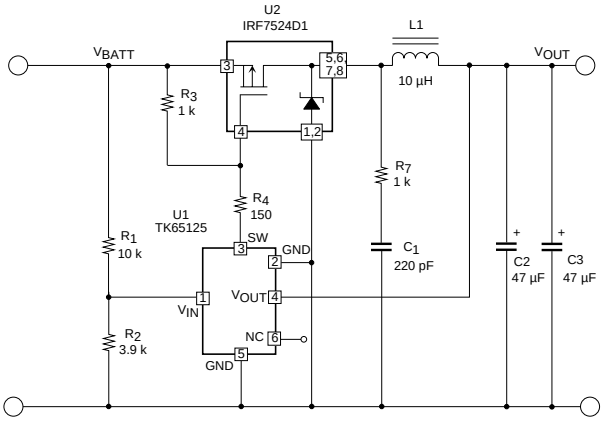
I_{OUT}	Output current *capability*	$I_{OUT(TGT)}$	Targeted output current capability
V_{OUT}	Output voltage	V_F	Diode forward voltage
V_{BB}	Battery voltage, unloaded	D	Oscillating duty ratio of main switch
f	Oscillator frequency	L	Inductance value
R_S	Source resistance (battery + filter)	R_L	Inductor winding resistance
R_{SW}	Switch on-state resistance	R_{OF}	Output filter resistance
R_U	ESR of upstream output capacitor	C_S	Snubber capacitance

Deriving a design solution with this equation is necessarily an iterative process. Use worst-case tolerances as described for inductor selection, using different values for "L" to approximately achieve an "I_{OUT}" equal to the targeted value. Then, fine tune the parasitic values as needed and, if necessary, readjust "L" again and reiterate the process.

STEP-DOWN CONVERTER APPLICATION

HOW TO MAKE A STEP-DOWN CONVERTER USING THE TK65020 AND AN IRF7524D1 "FETKY" PART

The TK65020 can be used as a controller in a step-down converter with the following two additional changes. See Fig 3.



Note: L = 10 µH
Toko P/N: 636CY-100M
D73C Coil

FIGURE 3: STEP-DOWN CONVERTER USING THE TK65020 SCHEMATIC

1) **Change the main switch orientation for use in a step-down converter.** An external P-channel power MOSFET is used as the main switch in a step-down converter configuration. The gate of FET is turned on through a resistor divider being pulled down to GND by the internal output transistor of the TK65020. This application requires both a logic level P-channel MOSFET and a Schottky diode. An IRF7524D1 "FETKY" part contains both in a small micro 8 package.

2) **Change the voltage seen at the V_{IN} pin of the TK65020 to below the regulation voltage at the V_{OUT} pin.** A resistor divider between the converter V_{IN} and the chip V_{IN} pin drops the voltage seen at the V_{IN} pin. If the V_{IN} pin is a higher voltage than the V_{OUT} pin, the TK65020 will not regulate the output, but will continue to pulse its output transistor.

WHERE TO USE THIS STEP-DOWN CONVERTER

The TK65020 is a Pulse Burst Modulation (PBM) controller with a fixed duty cycle of approximately 50%. Therefore, only if V_{BATT} is more than twice the voltage of V_{OUT} can the converter run in Continuous Current Mode (CCM). The converter can and does regulate in Discontinuous Current Mode (DCM) for lighter output current loads with V_{IN} less than twice the voltage of V_{OUT}. But DCM produces more peak current and more ripple current than CCM. Below is a table giving some examples of where this type of step-down converter might be used.

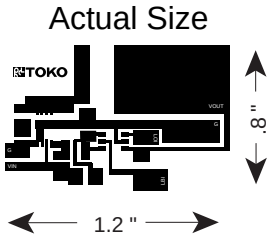
Type Battery	# of Cells	V_{BATT} Range	V_{OUT}	Typ. Max I_{OUT}	Oper Mode	Inductor
Li-ion	2 (Note 1)	5.4 to 8.4 V	2.5 V	500 mA	DCM	10 µH
NiMH	4 (Note 2)	4.4 to 5.2 V	2.5 V	500 mA	DCM	10 µH
NiMH	6 (Note 2)	6.6 to 7.8 V	2.5 V	500 mA	CCM	120 µH

Note 1: Li-ion cell voltage range 2.7 V to 4.2 V
Note 2: NiMH cell voltage range 1.1 V to 1.3 V

STEP-DOWN CONVERTER APPLICATION (CONT.)

THE AMOUNT OF BOARD SPACE NEEDED TO IMPLEMENT THIS STEP-DOWN CONVERTER

An evaluation board for this converter has been made using a TOKO 3DF, D73 or D75 series inductor, using only 0.96 sq. inches of board space. The artwork for the surface-mount circuit board is shown below in Figure 4.



Note: Short pin 2 to 5 for use with TK65020

FIGURE 4: TK65020 STEP-DOWN CONVERTER EVALUATION BOARD ARTWORK

PULSED LOAD APPLICATION

Often in the world of power conversion, the current draw of the load circuit is not constant, but rather pulsed. It is common in power supply design to size the power path large enough, and make the feedback loop fast enough to support these pulsed maximum currents. For applications where the pulse width is long or unpredictable, this approach may be warranted. However, in applications where the pulse width and maximum frequency of occurrence is predictable, such as digital cell phones or two-way pagers, it may be easier and wiser to increase the energy storage in the output filter of the power supply and keep the power path small. This leads to the need for a very large value output capacitor. Panasonic makes a series AL gold cap "super cap" which is a low voltage, large value capacitor in the one farad range.

Before designing a low power DC-DC converter with a "super cap" in its output filter, it is necessary to know the loading profile (the waveform of the current going into the load from the output of the converter) of the application in which it is to be used. The converter can then be designed so that the "super cap" can be recharged in the time before the next big discharge current pulse comes along.

Figure 5 is an example "super cap" charge/discharge diagram showing that the charge into the cap needs to equal the charge leaving the cap during discharge. This diagram comes from the loading and unloading profile information. In reality, some extra charge needs to go into the cap to make up for the losses caused by ESR of the cap.

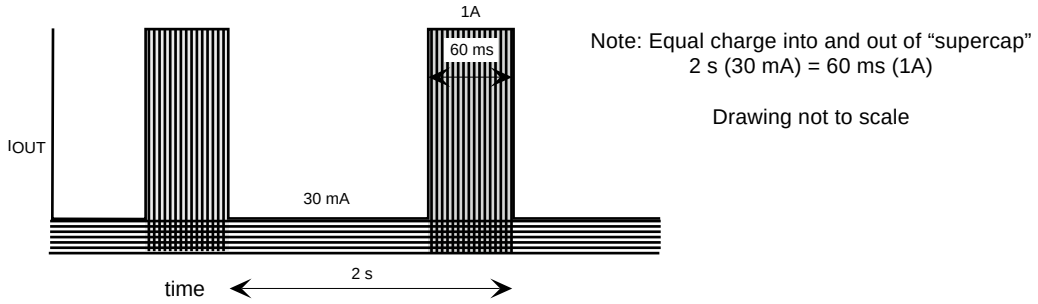


FIGURE 5: "SUPER CAP" CHARGE/DISCHARGE DIAGRAM

Figure 6 is a schematic for this "super cap" example application.

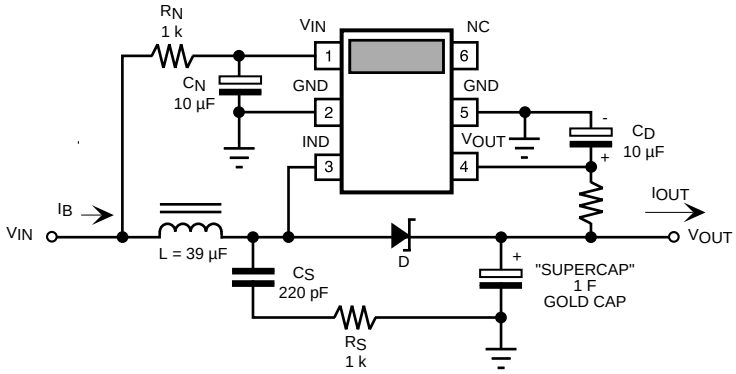
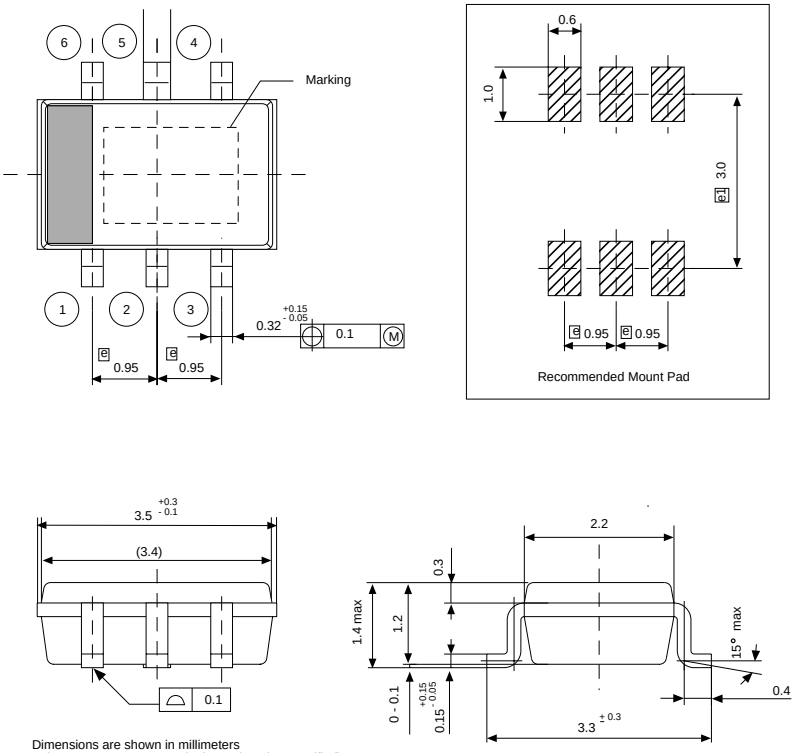


FIGURE 6: PULSED LOAD "SUPER CAP" APPLICATION SCHEMATIC

PACKAGE OUTLINE

SOT-23L-6



Dimensions are shown in millimeters
Tolerance: x.x = ± 0.2 mm (unless otherwise specified)

Marking Information

	Marking
TK65020	20M

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