

## COMPLEMENTARY SILICON HIGH-POWER TRANSISTORS

... designed for use in general purpose power amplifier and switching applications.

### FEATURES:

\* Collector-Emitter Sustaining Voltage -

$V_{CE(sus)}$  = 40V(Min)- TIP33,TIP34  
 60V(Min)- TIP33A,TIP34A  
 80V(Min)- TIP33B,TIP34B  
 100V(Min)- TIP33C,TIP34C

\* DC Current Gain  $hFE=40(\text{Min})@I_C = 1.0A$

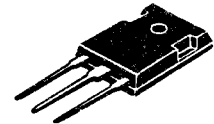
\* Current Gain-Bandwidth Product  $f_T=3.0 \text{ MHz}(\text{Min})@I_C=0.5A$

<b>NPN</b>	<b>PNP</b>
<b>TIP33</b>	<b>TIP34</b>
<b>TIP33A</b>	<b>TIP34A</b>
<b>TIP33B</b>	<b>TIP34B</b>
<b>TIP33C</b>	<b>TIP34C</b>

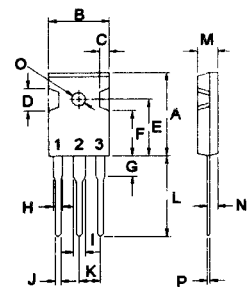
10 AMPERE  
COMPLEMENTARY SILICON  
POWER TRANSISTORS  
40 -100 VOLTS  
80 WATTS

### MAXIMUM RATINGS

Characteristic	Symbol	TIP33 TIP34	TIP33A TIP34A	TIP33B TIP34B	TIP33C TIP34C	Unit
Collector-Emitter Voltage	$V_{CEO}$	40	60	80	100	V
Collector-Base Voltage	$V_{CBO}$	40	60	80	100	V
Emitter-Base Voltage	$V_{EBO}$	5.0				V
Collector Current - Continuous - Peak	$I_C$	10 15				A
Base Current	$I_B$	3.0				A
Total Power Dissipation@ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	80 0.64				W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{STG}$	-65 to +150				$^\circ\text{C}$



TO-247(3P)



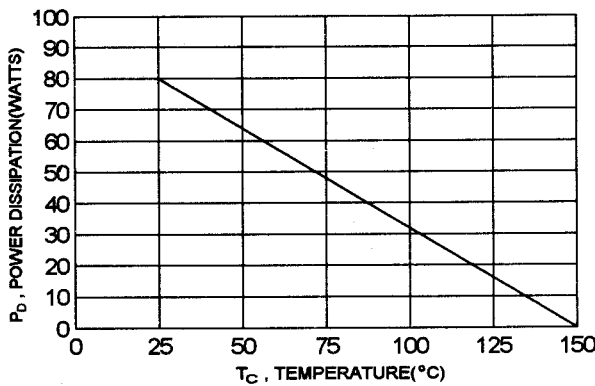
PIN 1.BASE  
2.COLLECTOR  
3.EMITTER

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	$R_{\theta jc}$	1.56	$^\circ\text{C/W}$

DIM	MILLIMETERS	
	MIN	MAX
A	20.63	22.38
B	15.38	16.20
C	1.90	2.70
D	5.10	6.10
E	14.81	15.22
F	11.72	12.84
G	4.20	4.50
H	1.82	2.46
I	2.92	3.23
J	0.89	1.53
K	5.26	5.66
L	18.50	21.50
M	4.68	5.36
N	2.40	2.80
O	3.25	3.65
P	0.55	0.70

FIGURE -1 POWER DERATING



**TIP33, TIP33A, TIP33B, TIP33C NPN / TIP34, TIP34A, TIP34B, TIP34C PNP**

**ELECTRICAL CHARACTERISTICS (  $T_C = 25^\circ\text{C}$  unless otherwise noted )**

Characteristic	Symbol	Min	Max	Unit
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**OFF CHARACTERISTICS**

Collector-Emitter Sustaining Voltage(1) ( $I_C = 30\text{ mA}$ , $I_B = 0$ )	TIP33, TIP34 TIP33A, TIP34A TIP33B, TIP34B TIP33C, TIP34C	$V_{CEO(sus)}$	40 60 80 100	V
Collector Cutoff Current ( $V_{CE} = 30\text{ V}$ , $I_B = 0$ ) ( $V_{CE} = 60\text{ V}$ , $I_B = 0$ )	TIP33, TIP34, TIP33A, TIP34A TIP33B, TIP34B, TIP33C, TIP34C	$I_{CEO}$	0.7 0.7	mA
Collector Cutoff Current ( $V_{CE} = 40\text{ V}$ , $V_{EB} = 0$ ) ( $V_{CE} = 60\text{ V}$ , $V_{EB} = 0$ ) ( $V_{CE} = 80\text{ V}$ , $V_{EB} = 0$ ) ( $V_{CE} = 100\text{ V}$ , $V_{EB} = 0$ )	TIP33, TIP34 TIP33A, TIP34A TIP33B, TIP34B TIP33C, TIP34C	$I_{CES}$	0.4 0.4 0.4 0.4	mA
Emitter Cutoff Current ( $V_{EB} = 5.0\text{ V}$ , $I_C = 0$ )		$I_{EBO}$	1.0	mA

**ON CHARACTERISTICS (1)**

DC Current Gain ( $V_{CE} = 4.0\text{ V}$ , $I_C = 1.0\text{ A}$ ) ( $V_{CE} = 4.0\text{ V}$ , $I_C = 3.0\text{ A}$ )		$h_{FE}$	40 20	100
Collector-Emitter Saturation Voltage ( $I_C = 3.0\text{ A}$ , $I_B = 0.3\text{ A}$ ) ( $I_C = 10\text{ A}$ , $I_B = 2.5\text{ A}$ )		$V_{CE(sat)}$		1.0 4.0
Base-Emitter On Voltage ( $I_C = 3.0\text{ A}$ , $V_{CE} = 4.0\text{ V}$ ) ( $I_C = 10\text{ A}$ , $V_{CE} = 4.0\text{ V}$ )		$V_{BE(on)}$		1.6 3.0

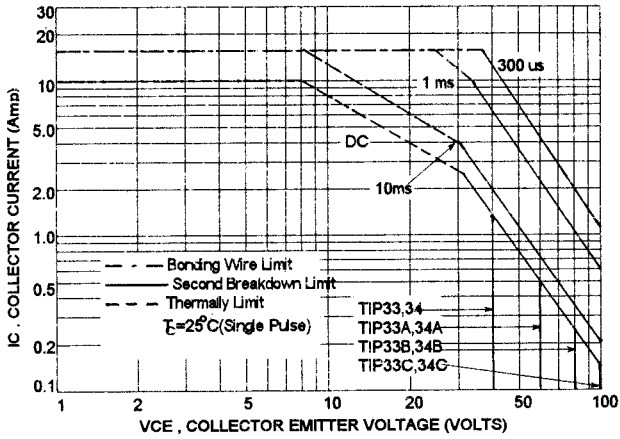
**DYNAMIC CHARACTERISTICS**

Current Gain - Bandwidth Product (2) ( $I_C = 0.5\text{ A}$ , $V_{CE} = 10\text{ V}$ , $f_{TEST} = 1\text{ MHz}$ )		$f_T$	3.0	MHz
Small Signal Current Gain ( $I_C = 0.5\text{ A}$ , $V_{CE} = 10\text{ V}$ , $f = 1\text{ kHz}$ )		$h_{fe}$	20	

(1) Pulse Test: Pulse width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

(2)  $f_T = |h_{fe}| \cdot f_{TEST}$

FIG-2 ACTIVE- REGION SAFE OPERATING AREA

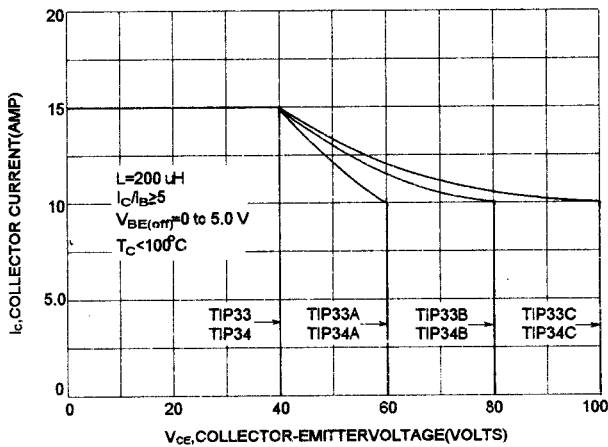


FORWARD BIAS

There are two limitation on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of FIG-2 is base on  $T_c = 25^\circ\text{C}$ ;  $T_{J(PK)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_c \geq 25^\circ\text{C}$ , second breakdown limitations do not derate the same as thermal limitations.

FIG-3 REVERSE BIAS SAFE OPERATING AREA



REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases with the base-to-emitter junction reverse biased under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several mean such as active clamping, RC snubbing, load line shaping, etc. the safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. FIG-3 gives the RBSOA characteristics.

FIG-4 DC CURRENT GAIN

