# **Power MOSFET**

# 30 V, 12 A, Single N-Channel, SO-8

### **Features**

- High Density Power MOSFET with Ultra Low R<sub>DS(on)</sub> for Higher Efficiency
- Miniature SO-8 Surface Mount Package Saving Board Space
- I<sub>DSS</sub> Specified at Elevated Temperature
- Diode Exhibits High Speed, Soft Recovery

# **Applications**

- Power Management for Battery Power Products
- Portable Products
- Computers, Printers, PCMCIA Cards
- Cell Phones, Cordless Telephones

# MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit	
Drain-to-Source Voltage			V <sub>DSS</sub>	30	V	
Gate-to-Source Voltage	Gate-to-Source Voltage			±20	V	
Continuous Drain	Steady	T <sub>A</sub> = 25°C	I <sub>D</sub>	9.6	Α	
Current (Note 1)	State	T <sub>A</sub> = 70°C		7.6		
	tp ≤10 s	$T_A = 25^{\circ}C$		12		
Power Dissipation	Stead	y State	$P_{D}$	1.56	W	
(Note 1)	tp ≤	≤10 s		2.5		
Continuous Drain	Steady	T <sub>A</sub> = 25°C	I <sub>D</sub>	7.0	Α	
Current (Note 2)	State	T <sub>A</sub> = 70°C		5.6		
Power Dissipation (Note 2)		T <sub>A</sub> = 25°C	P <sub>D</sub>	0.83	W	
Pulsed Drain Current	tp = 10 μs, DC = 2 %		I <sub>DM</sub>	50	Α	
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C	
Source Current (Body Diode)			I <sub>S</sub>	6.0	Α	
Single Pulse Drain–to–Source Avalanche Energy ( $V_{DD}$ = 20 V, $V_{GS}$ = 5 V, $I_{PK}$ = 7.25 A, L = 19 mH, $R_G$ = 25 $\Omega$ )			E <sub>AS</sub>	500	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C		

# THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	80	°C/W
Junction-to-Ambient - t = 1 0 s (Note 1)	$R_{\theta JA}$	50	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	150	

- 1. Surface-mounted on FR4 board using 1 in sq. pad size
- (Cu area = 1.127 in sq. [1 oz] including traces)
  2. Surface–mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412 in sq.)

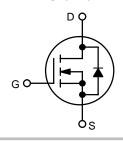


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### http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX
30 V	9.7 m $\Omega$ @ 10 V	12 A
00 1	15.5 mΩ @ 4.5 V	.1

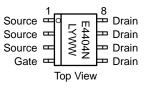
# **N-Channel**



# **MARKING DIAGRAM/ PIN ASSIGNMENT**



SO-8 **CASE 751** STYLE 12



E4404N = Device Code = Assembly Location = Year WW = Work Week

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>		
NTMS4404NR2	SO-8	2500/Tape & Reel		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Units
OFF CHARACTERISTICS	•			•		•	
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /				25		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	., .,,,	T <sub>J</sub> = 25°C			1.0	μΑ
	$V_{GS} = 0 \text{ V}, V_{DS} = 30 \text{ V}$ $T_{J} = 100^{\circ}\text{C}$	T <sub>J</sub> = 100°C			5.0		
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} =$	±20 V			±100	nA
ON CHARACTERISTICS (Note 3)	•					-	
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D = 3$	250 μΑ	1.0	2.2	3.0	V
Gate Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>				-5.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> =	= 12 A		9.7	11.5	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> =	= 6.0 A		15.5	17.5	
Forward Transconductance	9FS	V <sub>DS</sub> = 15 V, I <sub>D</sub> =	: 12 A		17.5		S
CHARGES AND CAPACITANCES							
Input Capacitance	C <sub>ISS</sub>				1975	2500	pF
Output Capacitance	C <sub>OSS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz,	V <sub>DS</sub> = 24 V		575	750	
Reverse Transfer Capacitance	C <sub>RSS</sub>				180	300	
Total Gate Charge	Q <sub>G(TOT)</sub>				50	70	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>	1,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,			2.4		1
Gate-to-Source Charge	Q <sub>GS</sub>	$V_{GS} = 10 \text{ V}, V_{DS} = 24$	$V_{GS} = 10 \text{ V}, V_{DS} = 24 \text{ V}, I_D = 12 \text{ A}$		7.5		
Gate-to-Drain Charge	$Q_{GD}$	1			16		
SWITCHING CHARACTERISTICS, V <sub>GS</sub> = '	10 V (Note 4)						
Turn-On Delay Time	t <sub>d(ON)</sub>				15	25	ns
Rise Time	tr	$V_{GS} = 10 \text{ V}, V_{DS} = 24 \text{ V}, I_{D} = 12 \text{ A},$ $R_{G} = 2.5 \Omega$			25	50	
Turn-Off Delay Time	t <sub>d(OFF)</sub>				35	55	
Fall Time	t <sub>f</sub>				15	30	
SWITCHING CHARACTERISTICS, V <sub>GS</sub> = 4	I.5 V (Note 4)						
Turn-On Delay Time	t <sub>d(ON)</sub>				20		ns
Rise Time	tr	$V_{GS} = 4.5 \text{ V}, V_{DS} = 24$	V, I <sub>D</sub> = 6.0 A,		80		]
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$R_{G} = 2.5 \Omega$			25		
Fall Time	t <sub>f</sub>				15		
DRAIN-SOURCE DIODE CHARACTERIST	TICS (Note 4)						
Forward Diode Voltage	$V_{SD}$	$V_{CC} = 0 \ V_{CC} = 6.0 \ A$	T <sub>J</sub> = 25°C		0.80	1.1	V
			T <sub>J</sub> = 125°C		0.65		
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 \text{ V, } d_{ISD}/d_t = 100 \text{ A/}\mu\text{s,}$ $I_S = 6.0 \text{ A}$			40	55	ns
Charge Time	t <sub>a</sub>				23		
Discharge Time	tb				17		1
Reverse Recovery Charge	Q <sub>RR</sub>				0.05		μС

- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
   Switching characteristics are independent of operating junction temperatures.

# **TYPICAL PERFORMANCE CURVES**

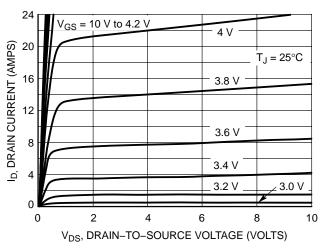


Figure 1. On-Region Characteristics

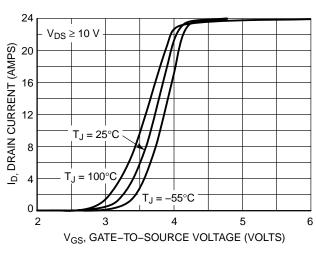


Figure 2. Transfer Characteristics

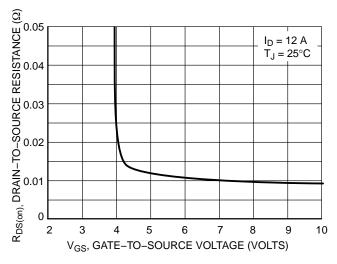


Figure 3. On-Resistance vs. Gate-to-Source Voltage

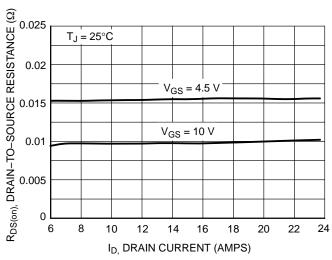


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

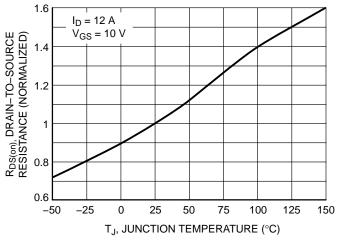


Figure 5. On–Resistance Variation with Temperature

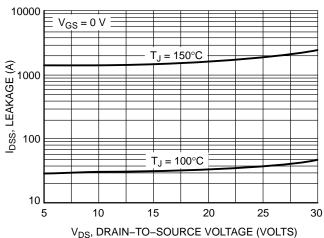
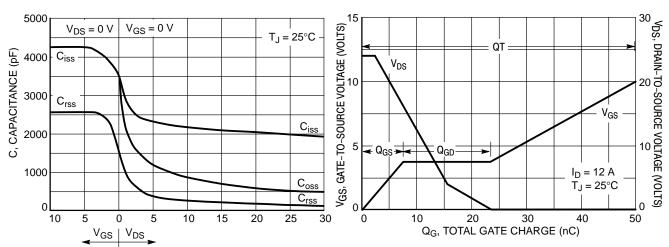


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# **TYPICAL PERFORMANCE CURVES**



GATE-TO-SOURCE OR DRAIN-TO-SOURCE VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

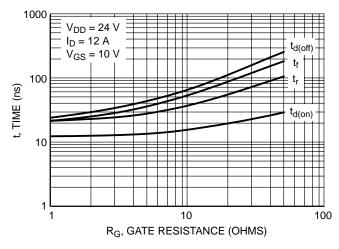


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

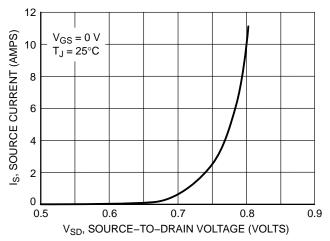


Figure 10. Diode Forward Voltage vs. Current

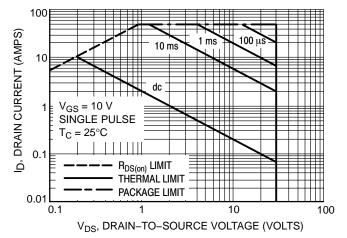


Figure 11. Maximum Rated Forward Biased Safe Operating Area

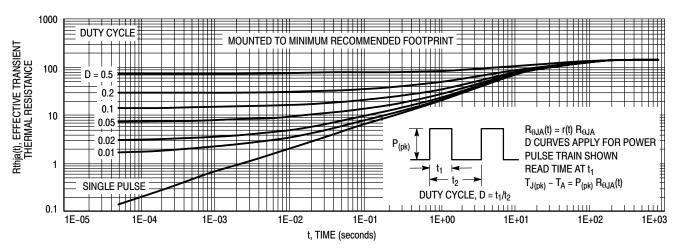
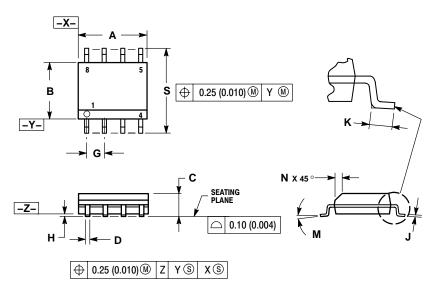


Figure 12. Thermal Response - Various Duty Cycles

# PACKAGE DIMENSIONS

# SOIC-8 NB CASE 751-07 **ISSUE AA**



### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14 5M 1982
- CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. 751–01 THRU 751–06 ARE OBSOLETE, NEW
- STANDARD IS 751-07.

	MILLIMETERS		INCHES			
DIM	MIN	MAX	MIN	MAX		
Α	4.80	5.00	0.189	0.197		
В	3.80	4.00	0.150	0.157		
C	1.35	1.75	0.053	0.069		
ם	0.33	0.51	0.013	0.020		
G	1.27 BSC		0.05	50 BSC		
Н	0.10	0.25	0.004	0.010		
7	0.19	0.25	0.007	0.010		
K	0.40	1.27	0.016	0.050		
M	0 °	8 °	0 °	8 °		
N	0.25	0.50	0.010	0.020		
S	5.80	6.20	0.228	0 244		

## STYLE 12:

PIN 1. SOURCE

- SOURCE
- 3. SOURCE GATE
- DRAIN
- DRAIN
- DRAIN
- DRAIN

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