PRELIMINARY

4-BIT SINGLE CHIP OTP MICRO CONTROLLER

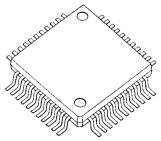
■ GENERAL DESCRIPTION

The **NJU3555** is the C-MOS 4-bit Single Chip OTP type Micro Controller with programmable Flash Memory.

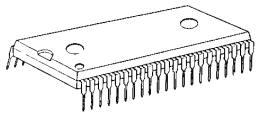
It is completely compatible with the **NJU3505** in function and the pin configuration. Therefore, the **NJU3555** is suitable for the final evaluation before **NJU3505** mask generation, the small quantity production and short lead-time.

* *In this data sheet, only OTP programming and the difference between **NJU3555** and **NJU3505** are mentioned mainly.*
*Therefore the detail function and specification should be referred on the **NJU3505** data sheet.*

■ PACKAGE OUTLINE



NJU3555FA1



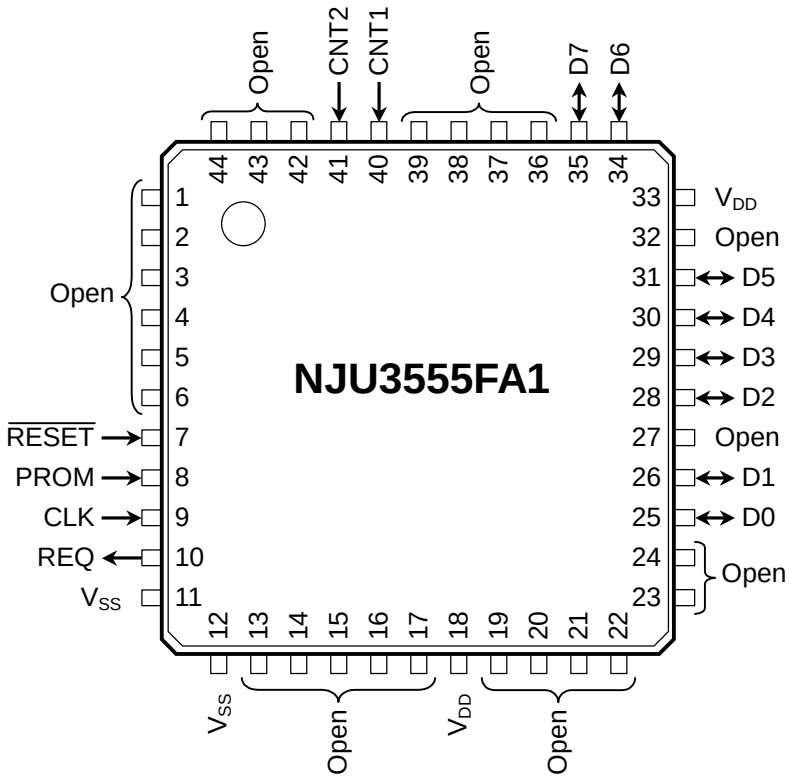
NJU3555L

■ FEATURES

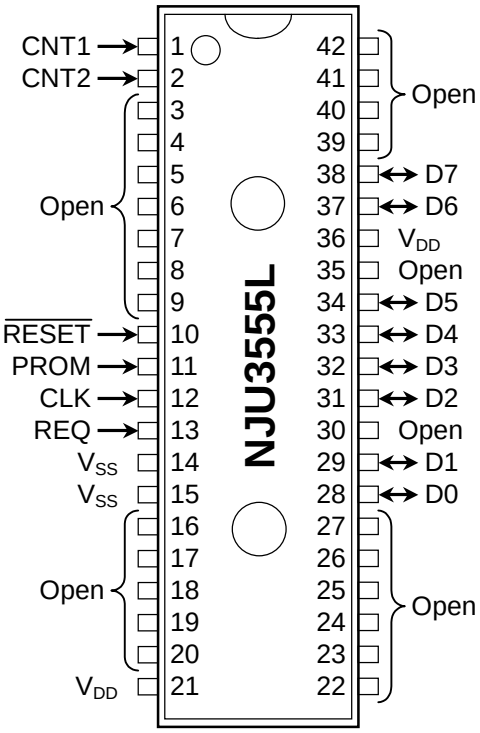
- Internal One Time Programmable ROM 8,192 X 8bits
  (8,128 X 8bits (Program area)
  64 X 8bits (Option area))
- Internal Data RAM 256 X 4bits
- Wide operating voltage range 2.7V ~ 5.5V
- Package outline QFP44-A1 / SDIP42 (Compatible with **NJU3505**)
- ROM programmer “SUPERPRO/L” by XELTEK co,.

■ PIN CONFIGURATION IN OTP PROGRAMMING MODE

[QFP44-A1]

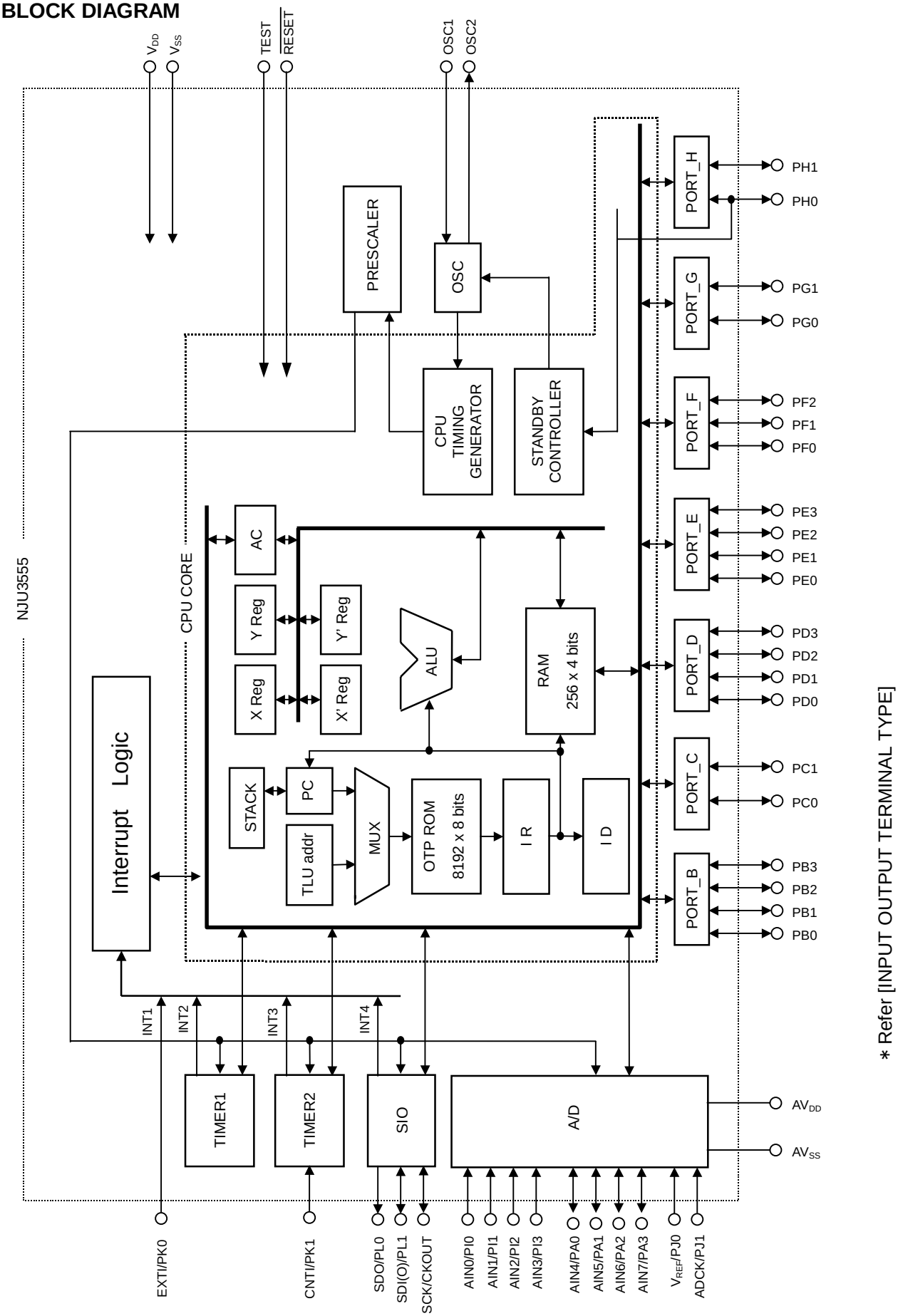


[SDIP42]



Note) The pin configuration in Normal operating mode is the same as **NJU3505**.

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION IN OTP PROGRAMMING MODE

No.		SYMBOL	INPUT / OUTPUT	F U N C T I O N
NJU 3555F	NJU 3555L			
7	10	$\overline{\text{RESET}}$	INPUT	RESET terminal. When the low-level input-signal, the system is initialized.
25, 26, 28-31, 34, 35	28, 29, 31-34, 37, 38	D0 - D7	INPUT/OUTPUT	Data bus
1 2	40, 41	CNT1 CNT2	INPUT INPUT	OTP control input terminal
10	13	REQ	OUTPUT	Request output terminal
9	12	CLK	INPUT	Clock input terminal
8	11	PROM	INPUT	OTP programming enable terminal
18, 33	21, 36	V_{DD}	-	Power Source (5V)
11, 12	14, 15	V_{SS}	-	Power Source (0V)

Note 1) Use at V_{DD}=5V in OTP programming mode.
2) Non connect anything to the other terminals.

■ Difference between NJU3555 (OTP version) and NJU3505 (MASK version)

● Operating mode

NJU3555 has two operating modes. One is "Normal operating mode" and the other is "OTP programming mode".

- Normal operating mode
  The "TEST" terminal is set to low level. (The terminal is recommended to connect to GND.)
  Operating voltage range; 2.7V ~ 5.5V.

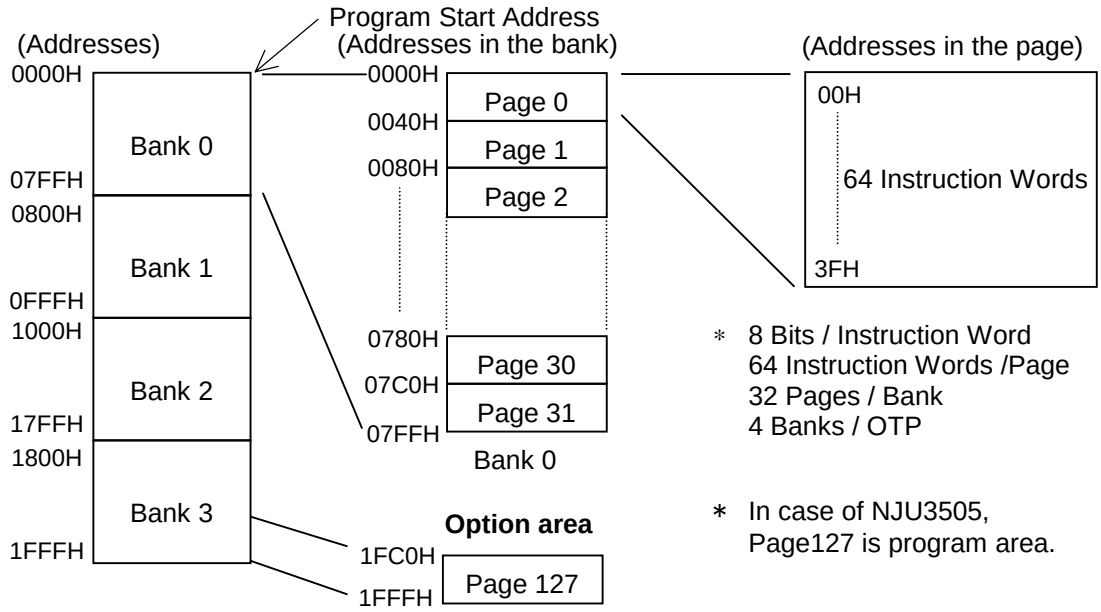
- OTP Programming mode
  User program is read out from or written into the OTP by the universal programmer "SUPERPRO/L" and converting adapter made by XELTEK co,.(USA).

● Programming memory (OTP)

The address location of programming memory (OTP) of **NJU3555** is compatible with the masked ROM of **NJU3505**, excepting the option area.
The option area is located in page 127(64bytes) in the following.

Program Area **:** Addresses **0000H ~ 1FBFH** : 8,128bytes
Option Area **:** Addresses **1FC0H ~ 1FFFH** : 64bytes

[PROGRAM MEMORY AREA]



* 8 Bits / Instruction Word
64 Instruction Words /Page
32 Pages / Bank
4 Banks / OTP

* In case of NJU3505,
Page127 is program area.

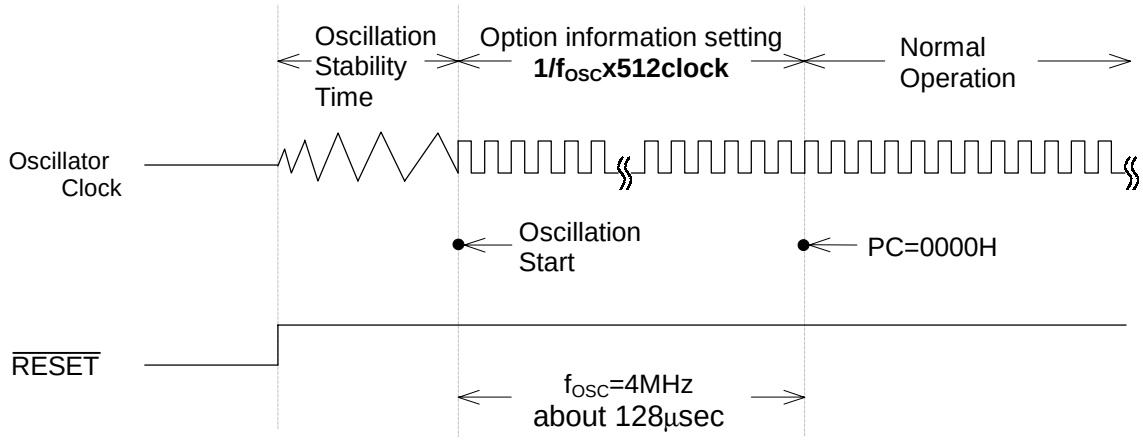
- Reset Terminal Type

	NJU3555	NJU3505
Internal Pull-up Resistance	With Pull-up	Without Pull-up

- Option information set in the initialization

When the initialization is performed($\overline{\text{RESET}}$ terminal is "L"), the operation information stored in option area is set as shown in the following timing chart . The option information is set in the term of **1 / f_{osc} x 512clock** after RESET releasing and oscillation stability time. After information set, the program counter is set to 0000H and the **NJU3555** operates in normal.

[TIMING CHART]



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ +7.0	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD} + 0.3	V
Output Voltage	V_{OUT}	-0.3 ~ V_{DD} + 0.3	V
Analog Supply Voltage	AV_{DD}	-0.3 ~ V_{DD} + 0.3	V
Analog Reference Voltage	V_{REF}	-0.3 ~ AV_{DD} + 0.3	V
Analog Input Voltage	AIN0 ~ AIN7	-0.3 ~ AV_{DD} + 0.3	V
Operating Temperature	T_{opr}	-20 ~ +75	°C
Storage Temperature	T_{stg}	-55 ~ +125	°C

Note)

The difference of electrical characteristics between **NJU3555** (OTP version) and **NJU3505** (MASK version)

		NJU3505		**NJU3555**
•Supply Voltage (V_{DD}) MIN.		2.4V	→	2.7V
•Supply Current				
5V	(I_{DD1}) Max.	1.2mA	→	30mA
	(I_{DD2}) Max.	1.2mA	→	30mA
	(I_{DD3}) Max.	1.6mA	→	30mA
	(I_{DD4}) Max.	4.0mA		30mA
	(I_{DD5}) Max.	4.0μA	→	20μA
3V	(I_{DD1}) Max.	0.5mA	→	20mA
	(I_{DD2}) Max.	0.5mA	→	20mA
	(I_{DD3}) Max.	0.6mA		20mA
	(I_{DD4}) Max.	1.0mA	→	20mA
	(I_{DD5}) Max.	2.0μA	→	20μA

■ ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS 1-1

(V_{DD}=3.6~5.5V, V_{SS}=0V, Ta=-20~75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	V_{DD}	3.6		5.5	V	
Supply Current	I_{DD1}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz X'tal Oscillation in Reset			30	mA	*3
	I_{DD2}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz Ceramic Oscillation in Reset			30	mA	*3
	I_{DD3}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz CR Oscillation in Reset			30	mA	*3
	I_{DD4}	V_{DD} V_{DD}=5V, f_{OSC}=4MHz Operating (Except ADC)			30	mA	*3
	I_{DD5}	V_{DD} V_{DD}=5V, STANDBY Mode			20	μA	*3
	I_{ADD}	AV_{DD} AV_{DD}=V_{DD}=5V, ADCK=225kHz		3.0	5.0	mA	*3
High-Level Input Voltage	V_{IH1}	AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0~PE3, AIN0/PI0~AIN3/PI3, SDI(O)/PL1, SCK/CKOUT	0.7V_{DD}		V_{DD}	V	*1
	V_{IH2}	PF0~PF2, PG0, PG1, PH0, PH1, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, $\overline{RESET}$	0.8V_{DD}		V_{DD}	V	*1
	V_{IH3}	OSC1	V_{DD}-1.0		V_{DD}	V	
Low-level Input Voltage	V_{IL1}	AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0~PE3, AIN0/PI0~AIN3/PI3, SDI(O)/PL1, SCK/CKOUT	0		0.3V_{DD}	V	*1
	V_{IL2}	PF0~PF2, PG0, PG1, PH0, PH1, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, $\overline{RESET}$	0		0.2V_{DD}	V	*1
	V_{IL3}	OSC1	0		1.0	V	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

■ ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS 1-2

(V_{DD}=3.6~5.5V, V_{SS}=0V, Ta=-20~75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
High-Level Input Current	I_{IH}	V_{DD}=5.5V, V_{IN}=5.5V AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0~PE3, PF0~PF2, PG0, PG1, PH0, PH1, AIN0/PI0~AIN3/PI3, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, SDI(O)/PL1, $\overline{\text{RESET}}$, SCK/CKOUT			10	μA	*1
Low-Level Input Current	I_{IL1}	V_{DD}=5.5V, V_{IN}=0V Without pull-up resistance AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0~PE3, PF0~PF2, PG0, PG1, PH0, PH1, AIN0/PI0~AIN3/PI3, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, SDI(O)/PL1, SCK/CKOUT			-10	μA	*1
	I_{IL2}	V_{DD}=5.5V, V_{IN}=0V With pull-up resistance AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0~PE3, PF0~PF2, PG0, PG1, PH0, PH1, AIN0/PI0~AIN3/PI3, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, SDI(O)/PL1, $\overline{\text{RESET}}$, SCK/CKOUT			-100	μA	*1
High-Level Output Voltage	V_{OH}	I_{OH}=-100μA PD0~PD3, PE0~PE3, PF0~PF2, PG0, PG1, PH0, PH1, SDO/PL0, SDI(O)/PL1, SCK/CKOUT	V_{DD}-0.5			V	*2
Low-Level Output Voltage	V_{OL1}	I_{OL1}=400μA PD0~PD3, PE0~PE3, PF0~PF2, PG0, PG1, PH0, PH1, SDO/PL0, SDI(O)/PL1, SCK/CKOUT			0.5	V	*2
	V_{OL2}	I_{OL2}=15mA AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1			2.0	V	*2
Output Leakage Current	I_{OD}	V_{DD}=5.5V, V_{OH}=5.5V AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1			10	μA	*2
Input Capacitance	C_{IN}	Except V_{DD}, V_{SS} terminals f_{OSC}=1MHz Other terminals : 0V		10	20	pF	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

■ ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS 2-1

(V_{DD}=2.7~3.6V, V_{SS}=0V, Ta=-20~75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	V_{DD}	2.7		3.6	V	
Supply Current	I_{DD1}	V_{DD} V_{DD}=3V, f_{OSC}=1MHz X'tal Oscillation in Reset			20	mA	*3
	I_{DD2}	V_{DD} V_{DD}=3V, f_{OSC}=1MHz Ceramic Oscillation in Reset			20	mA	*3
	I_{DD3}	V_{DD} V_{DD}=3V, f_{OSC}=1MHz CR Oscillation in Reset			20	mA	*3
	I_{DD4}	V_{DD} V_{DD}=3V, f_{OSC}=2MHz Operating (Except ADC)			20	mA	*3
	I_{DD5}	V_{DD} V_{DD}=3V, STANDBY Mode			20	μA	*3
	I_{ADD}	AV_{DD} AV_{DD}=V_{DD}=3V, ADCK=225kHz		2.5	3.5	mA	*3
High-Level Input Current	V_{IH1}	AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0~PE3, AIN0/PI0~AIN3/PI3, SDI(O)/PL1, SCK/CKOUT	0.8V_{DD}		V_{DD}	V	*1
	V_{IH2}	PF0~PF2, PG0, PG1, PH0, PH1, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, $\overline{RESET}$	0.85V_{DD}		V_{DD}	V	*1
	V_{IH3}	OSC1	V_{DD}-0.3		V_{DD}	V	
Low-Level Input Voltage	V_{IL1}	AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0~PE3, AIN0/PI0~AIN3/PI3, SDI(O)/PL1, SCK/CKOUT	0		0.2V_{DD}	V	*1
	V_{IL2}	PF0~PF2, PG0, PG1, PH0, PH1, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, $\overline{RESET}$	0		0.15V_{DD}	V	*1
	V_{IL3}	OSC1	0		0.3	V	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

■ ELECTRICAL CHARACTERISTICS DC CHARACTERISTICS 2-2

(V_{DD}=2.7~3.6V, V_{SS}=0V, Ta=-20~75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
High-Level Input Current	I_{IH}	V_{DD}=3.6V, V_{IN}=3.6V AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0~PE3, PF0~PF2, PG0, PG1, PH0, PH1, AIN0/PI0~AIN3/PI3, V_{REF}/PJ0, ADCK/PJ1, $\overline{\text{EXTI}}$/PK0, CNTI/PK1, SDI(O)/PL1, $\overline{\text{RESET}}$, SCK/CKOUT			10	μA	*1
Low-Level Input Current	I_{IL1}	V_{DD}=3.6V, V_{IN}=0V Without pull-up resistance AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0~PE3, PF0~PF2, PG0, PG1, PH0, PH1, AIN0/PI0~AIN3/PI3, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1, SDI(O)/PL1, SCK/CKOUT			-10	μA	*1
	I_{IL2}	V_{DD}=3.6V, V_{IN}=0V With pull-up resistance AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1, PD0~PD3, PE0~PE3, PF0~PF2, PG0, PG1, PH0, PH1, AIN0/PI0~AIN3/PI3, V_{REF}/PJ0, ADCK/PJ1, $\overline{\text{EXTI}}$/PK0, CNTI/PK1, SDI(O)/PL1, $\overline{\text{RESET}}$, SCK/CKOUT			-100	μA	*1
High-Level Output Voltage	V_{OH}	I_{OH}=-80μA PD0~PD3, PE0~PE3, PF0~PF2, PG0, PG1, PH0, PH1, SDO/PL0, SDI(O)/PL1, SCK/CKOUT	V_{DD}-0.5			V	*2
Low-Level Output Voltage	V_{OL1}	I_{OL1}=350μA PD0~PD3, PE0~PE3, PF0~PF2, PG0, PG1, PH0, PH1, SDO/PL0, SDI(O)/PL1, SCK/CKOUT			0.5	V	*2
	V_{OL2}	I_{OL2}=5mA AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1			1.0	V	*2
Output Leakage Current	I_{OD}	V_{DD}=3.6V, V_{OH}=3.6V AIN4/PA0~AIN7/PA3, PB0~PB3, PC0, PC1			10	μA	*2
Input Capacitance	C_{IN}	Except V_{DD}, V_{SS} terminals f_{OSC}=1MHz Other terminals : 0V		10	20	pF	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

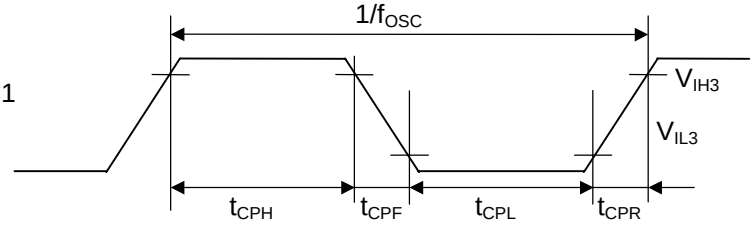
■ ELECTRICAL CHARACTERISTICS AC CHARACTERISTICS 1

(V_{SS}=0V, Ta= -20~75°C)

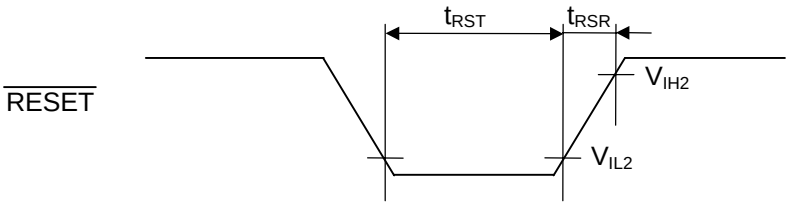
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Operating Frequency	f_{OSC}	V_{DD}=2.7~3.6V	X'tal Resonator	0.03		2.0	MHz
			Ceramic Resonator	0.03		2.0	
			External Resistor Oscillation	0.03		1.0	
			External Clock	0.03		2.0	
		V_{DD}=3.6~5.5V	X'tal Resonator	0.03		4.0	
			Ceramic Resonator	0.03		4.0	
			External Resistor Oscillation	0.03		2.0	
			External Clock	0.03		4.0	
Instruction Cycle Time	t_C				$6/f_{OSC}$		s
External Clock Pulse Width	t_{CPH}	V_{DD}=2.7~3.6V		250		16600	ns
	t_{CPL}	V_{DD}=3.6~5.5V		125		16600	
External Clock Rise Time / Fall Time	t_{CPR} / t_{CPF}	V_{DD}=2.7~5.5V				20	ns
$\overline{RESET}$ Low-Level Width	t_{RST}	V_{DD}=2.7~5.5V		$4/f_{OSC}$			s
$\overline{RESET}$ Rise Time	t_{RSR}	V_{DD}=2.7~5.5V				20	ms
Port Input Level Width	t_{PIN}	V_{DD}=2.7~5.5V		$6/f_{OSC}$			s
Edge Detection (PH1) Rise Time / Fall Time	t_{EDR} / t_{EDF}	V_{DD}=2.7~5.5V				200	ns
Restart Signal (PH0) Rise Time	t_{STR}	V_{DD}=2.7~5.5V				200	ns
External interrupt input (EXTI) Rise Time / Fall Time	t_{EXR} / t_{EXF}	V_{DD}=2.7~5.5V				200	ns
CNTI Clock Frequency	f_{CT}	V_{DD}=2.7~5.5V				$f_{OSC}/64$	Hz
CNTI High-Level Width	t_{CT}	V_{DD}=2.7~5.5V		$6/f_{OSC}$			s
CNTI Rise Time / Fall Time	t_{CTR} / t_{CTF}	V_{DD}=2.7~5.5V				200	ns

■ AC CHARACTERISTICS 1 TIMING CHART

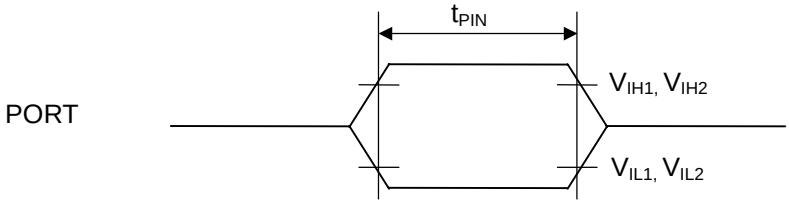
EXTERNAL CLOCK



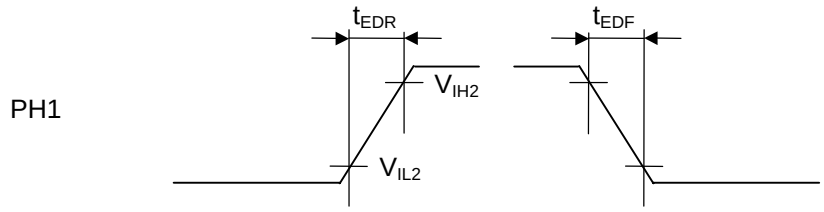
RESET INPUT



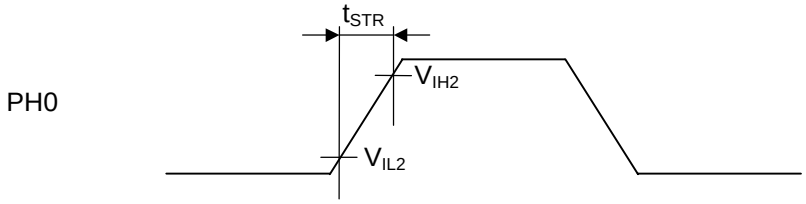
PORT INPUT



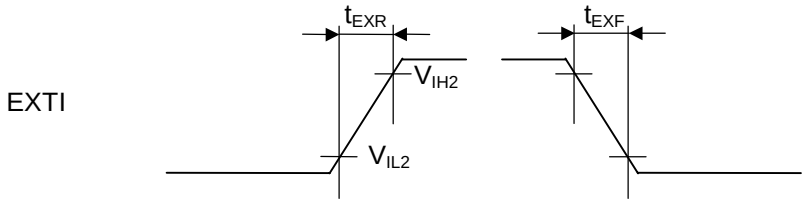
EDGE DETECTOR INPUT



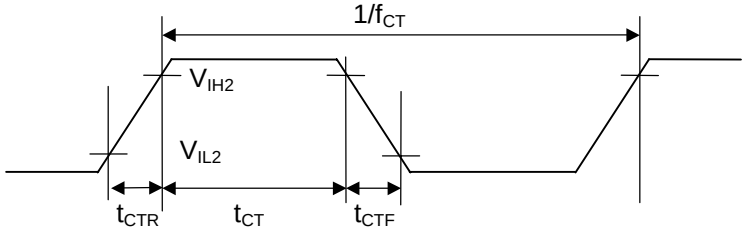
RESTART SIGNAL INPUT



EXTERNAL INTERRUPT



TIMER2 EXTERNAL CLOCK TIMING CHART



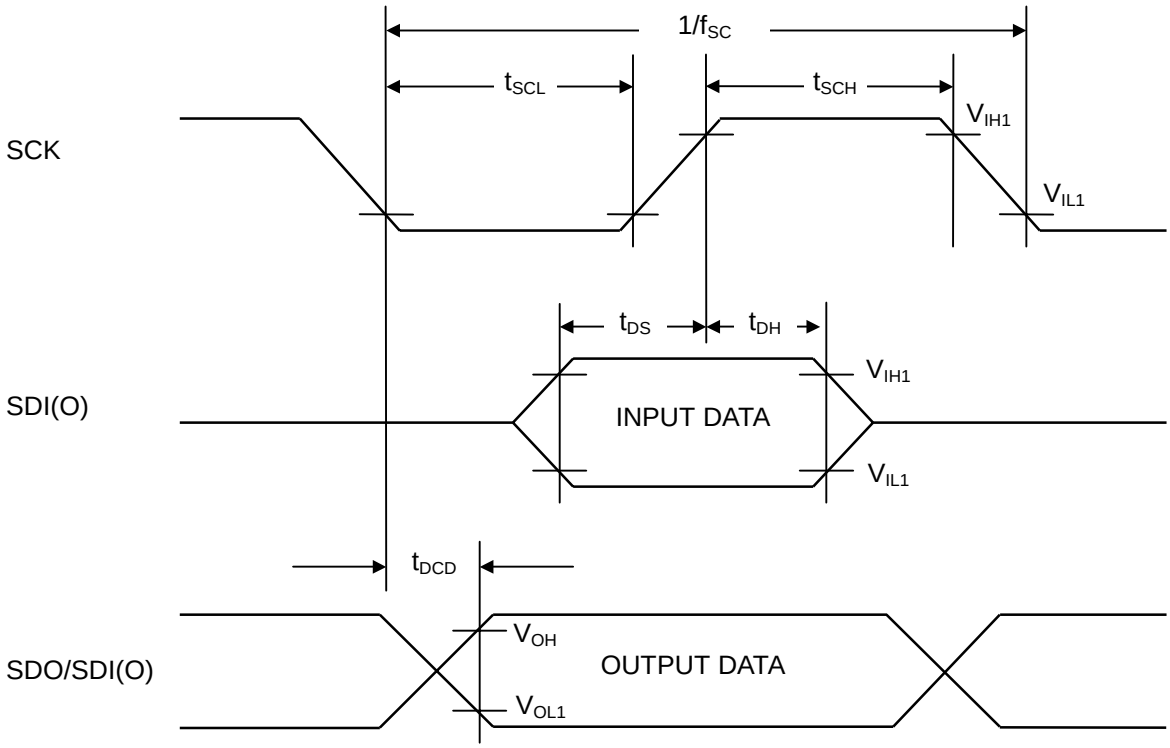
■ ELECTRICAL CHARACTERISTICS AC CHARACTERISTICS 2 SERIAL INTERFACE

(V_{SS}=0V, V_{DD}=2.7~5.5V, Ta= -20~75°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Serial Operating Frequency	f_{SC}	Internal Clock				(1/12) × f_{OSC}*	Hz
		External Clock				500k	
Clock Pulse Width Low-Level	t_{SCL}	Internal Clock	V_{DD}=2.7~3.6V f_{OSC}=2MHz	3.0			µs
			V_{DD}=3.6~5.5V f_{OSC}=4MHz	1.5			
		External Clock		1.0			
Clock Pulse Width High-Level	t_{SCH}	Internal Clock	V_{DD}=2.7~3.6V f_{OSC}=2MHz	3.0			µs
			V_{DD}=3.6~5.5V f_{OSC}=4MHz	1.5			
		External Clock		1.0			
SDI setup Time To SCK	t_{DS}			0.5			µs
SDI Hold time To SCK	t_{DH}			0.5			µs
SDO Data Fix Time To SCK	t_{DCD}					0.5	µs

* The dividing ratio of the internal clock is 1/2.

■ AC CHARACTERISTICS 2 SERIAL INTERFACE TIMING CHART



■ ELECTRICAL CHARACTERISTICS A/D CONVERTER CHARACTERISTICS

(V_{DD}=AV_{DD}=2.7~5.5V, V_{SS}=AV_{SS}=0V, Ta=25°C, f_{OSC}=4MHz)

PARAMETER	SYMBOL	C O N D I T I O N S	MIN	TYP	MAX	UNIT
Resolution	-		-	8	-	bits
Absolute Accuracy	-	V_{DD}=5V, AV_{DD}=5V, V_{REF}=5V			±2	LSB
Conversion Time	t_{CONV}	V_{DD}=5V, AV_{DD}=5V, V_{REF}=5V	40			µs
Reference Voltage	V_{REF}		2.7		AV_{DD}	V
Analog Input Voltage	V_{IA}		AV_{SS}		V_{REF}	V
ADCK Frequency	f_{ADCK}				225	kHz

■ OPTION as same as mask version (NJU3505)

1) INPUT OUTPUT Terminal Selection

All of input-output terminals select a terminal type for each port from the following table1 and table2 by the mask option.

[CIRCUIT TYPE TABLE 1]

SYMBOL	TERMINAL TYPES					REMARKS	
	Input / Output Terminal*1			EXTRA FUNCTION			
	Port of Input	Port of Output	Programmable Input / Output				
AIN4 / PA0			IOP IO	AD	Analog input to ADC (AIN4)		
AIN5 / PA1			IOP IO	AD	Analog input to ADC (AIN5)		
AIN6 / PA2			IOP IO	AD	Analog input to ADC (AIN6)		
AIN7 / PA3			IOP IO	AD	Analog input to ADC (AIN7)		
PB0			IOP IO				
PB1			IOP IO				
PB2			IOP IO				
PB3			IOP IO				
PC0	ICP IC	ONP ON					
PC1	ICP IC	ONP ON					
PD0	ICP IC	OC					
PD1	ICP IC	OC					
PD2	ICP IC	OC					
PD3	ICP IC	OC					
PE0	ICP IC	OC					
PE1	ICP IC	OC					
PE2	ICP IC	OC					
PE3	ICP IC	OC					

Note) The symbol in the above table is the same as in mask option generator software.

*1) The symbol and the detail circuits of INPUT OUTPUT TERMINAL are written in INPUT OUTPUT TERMINAL TYPE.

[CIRCUIT TYPE TABLE 2]

SYMBOL	TERMINAL TYPES					REMARKS	
	Input / Output Terminal*1			EXTRA FUNCTION			
	Port of Input	Port of Output	Programmable Input / Output				
PF0	ISP IS	OC					
PF1	ISP IS	OC					
PF2	ISP IS	OC					
PG0	ISP IS	OC					
PG1	ISP IS	OC					
PH0	ISP IS	OC			Restart signal input	E D	With restart input Without restart input
PH1	ISP IS	OC			Edge detection	R F D	Rise edge detection Fall edge detection Without edge detection
AIN0 / PI0	ICP IC			AD	Analog input to ADC (AIN0)		
AIN1 / PI1	ICP IC			AD	Analog input to ADC (AIN1)		
AIN2 / PI2	ICP IC			AD	Analog input to ADC (AIN2)		
AIN3 / PI3	ICP IC			AD	Analog input to ADC (AIN3)		
V_{REF} / PJ0	ISP IS			AD	Reference input (V_{REF})		
ADCK / PJ1 *2	ISP IS			ACP AC	External clock input (ADCK)		
EXTI / PK0 *2	ISP IS			IIP II	External interrupt input (EXTI)	R F	Rise interrupt input Fall interrupt input
CNTI / PK1 *2	ISP IS			IIP II	External clock of Timer 2 input (CNTI)		
SDO / PL0		OC		SO	Serial data output	MSB LSB	MSB first LSB first
SDI(O) / PL1 *2	ICP IC	OC		SDP SD	Serial data input/output		
SCK / CKOUT *2 *3				SCP SC	Serial clock input/output		
				-	Output clock divide by pre-scaler		

Note) The symbol in the above table is the same as in mask option generator software.

*1) The symbol and the detail circuits of INPUT OUTPUT TERMINAL are written in INPUT OUTPUT TERMINAL TYPE.

*2) The pull-up resistance is added to the terminal selected as the extra function.

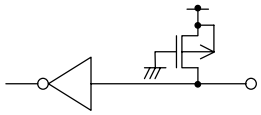
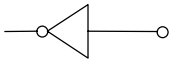
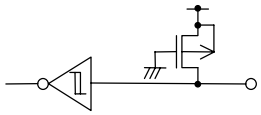
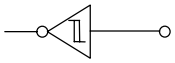
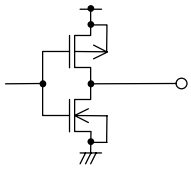
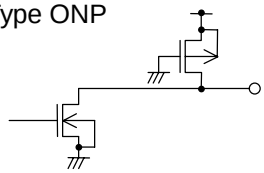
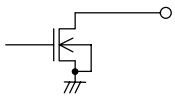
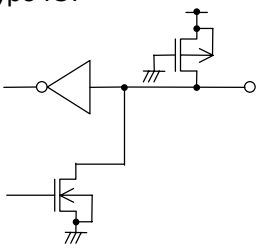
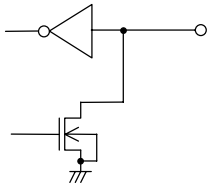
*3) When Serial INPUT-OUTPUT is selected, “SCK” is selected automatically. When it is not selected, “CKOUT” is selected automatically.

[MASK OPTION LIST]

SYMBOL	FUNCTION
ICP	C-MOS input with pull-up resistance
ISP	C-MOS Schmitt trigger input with pull-up resistance
IC	C-MOS input
IS	C-MOS Schmitt trigger input
ONP	Nch-FET Open-Drain output with pull-up resistance
OC	C-MOS output
ON	Nch-FET Open-Drain output
IIP	External interrupt input with pull-up resistance
II	External interrupt input
SDP	Serial data input/output with pull-up resistance
SD	Serial data input/output
SO	Serial data output
SCP	Serial clock input/output with pull-up resistance
SC	Serial clock input/output
AD	A/D converter
ACP	External clock input with pull-up resistance for ADC
AC	External clock input for ADC
IOP	Programmable input/output with pull-up resistance
IO	Programmable input/output

SYMBOL	FUNCTION
R	Rise edge detection
F	Fall edge detection
D	Prohibition of edge detection
MSB	Serial data order MSB first
LSB	Serial data order LSB first
1	1/2
2	1/4
3	1/8
4	1/16
5	1/32
6	1/64
7	1/128
8	1/256
9	1/512
a	1/1024
b	1/2048
c	1/4096
E	permission
D	prohibit

[INPUT OUTPUT TERMINAL TYPE]

	Types	With Pull-up	Without Pull-up	Terminals
INPUT TERMINAL	C-MOS	Type ICP 	Type IC 	PC0, PC1, PD0~PD3, PE0~PE3, AIN0/PI0~ AIN3/PI3, SDI(O)/PL1
	SCHMITT TRIGGER	Type ISP 	Type IS 	PF0~PF2, PG0, PG1, PH0, PH1, V_{REF}/PJ0, ADCK/PJ1, EXTI/PK0, CNTI/PK1
OUTPUT TERMINAL	C-MOS		Type ON 	PD0~PD3, PE0~PE3, PF0~PF2, PG0, PG1, PH0, PH1, SDO/PL0, SDI(O)/PL1
	N-channel(Nch) OPEN DRAIN	Type ONP 	Type ON 	PC0, PC1
PROGRAMMABLE INPUT OUTPUT TERMINAL	C-MOS INPUT / Nch OPEN DRAIN OUTPUT	Type IOP 	Type IO 	AIN4/PA0~ AIN7/PA3, PB0~PB3

2) Re-start signal Input Selection

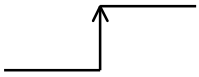
PH0 terminal performs as the re-start terminal to return from “STANDBY” mode. It is selected by mask option.

The STANDBY mode is released by the rising edge of the input signal to PH0 terminal, and the CPU re-starts the execution from the last address before the STANDBY mode in.

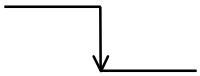
3) Edge Detector Selection

PH1 terminal is added the “Edge detect function” by the mask option.

Rising edge



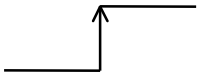
Falling edge



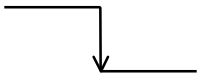
4) External Interrupt of the edge Selection

When the interrupt function is set by mask option. PK0 terminal performs as the interrupt input terminal. The polarity of the edge, rising as “low to high” or falling as “high to low”, is selected by the mask option.

Rising edge



Falling edge



5) The data order (MSB, LSB) of the Serial Interface

The data order of the Serial Interface is selected select either MSB or LSB first by the mask option.

6) A/D Control Clock

A/D Control Clock is selected either the external clock from ADCK terminal or the internal clock from the prescaler by the mask option.

7) Dividing ration of the internal clock

Each dividing ration of the count clocks of Timer1 and Timer2, the Internal shift clock of the Serial Interface, the clock of the A/D control clock and the output clock through the SCK/CKOUT terminal is selected among the following by the mask option.

The frequency of each clock is determined by the dividing ration and the 1-instruction term ($1/f_{OSC}$x6).

1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512, 1/1024, 1/2048, 1/4096

Note) As Timer2 clock, the external clock or the internal is selected by the program.
As the shift clock of the serial interface, the external clock or the internal is selected by the program.