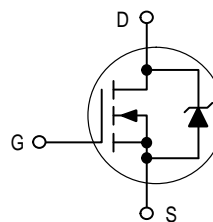


Designer's™ Data Sheet
TMOS E-FET™
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

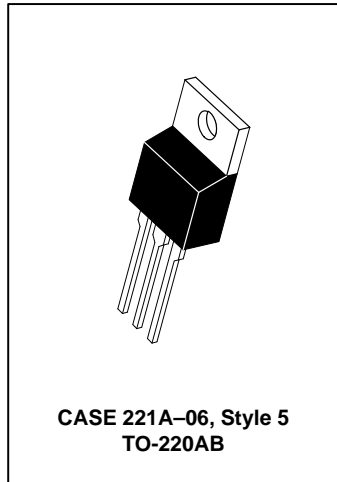
This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced TMOS E-FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters, PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature



MTP8N50E

TMOS POWER FET
8.0 AMPERES
500 VOLTS
 $R_{DS(on)} = 0.8 \text{ OHM}$



MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	500	Vdc
Drain-to-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	500	Vdc
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	Vdc
– Non-repetitive ($t_p \leq 10 \text{ ms}$)	V_{GSM}	± 40	Vpk
Drain Current — Continuous @ $T_C = 25^\circ\text{C}$	I_D	8.0	Adc
– Continuous @ $T_C = 100^\circ\text{C}$	I_D	5.0	
– Single Pulse ($t_p \leq 10 \text{ }\mu\text{s}$)	I_{DM}	32	Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	125	Watts
Derate above 25°C		1.0	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – STARTING $T_J = 25^\circ\text{C}$ ($V_{DD} = 25 \text{ Vdc}$, $V_{GS} = 10 \text{ Vdc}$, PEAK $I_L = 8.0 \text{ Apk}$, $L = 16 \text{ mH}$, $R_G = 25 \text{ }\Omega$)	EAS	510	mJ
Thermal Resistance			
– Junction-to-Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
– Junction-to-Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 sec.	T_L	260	$^\circ\text{C}$

This document contains information on a new product. Specifications and information herein are subject to change without notice.

E-FET and Designer's are trademarks of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.

MTP8N50E

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	500 —	— 500	— —	Vdc mV/°C	
Zero Gate Voltage Drain Current (V _{DS} = 500 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 400 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	— —	— —	250 1000	μAdc	
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	100	nAdc	
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	2.0 —	2.8 6.3	4.0 —	Vdc mV/°C	
Static Drain-to-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 4.0 Adc)	R _{DS(on)}	—	0.6	0.8	Ohms	
Drain-to-Source On-Voltage (V _{GS} = 10 Vdc) (I _D = 8.0 Adc) (I _D = 4.0 Adc, T _J = 125°C)	V _{DS(on)}	— —	5.0 —	7.2 6.4	Vdc	
Forward Transconductance (V _{DS} = 15 Vdc, I _D = 4.0 Adc)	g _{FS}	4.0	—	—	mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	—	1450	1680	pF
Output Capacitance		C _{oss}	—	190	246	
Transfer Capacitance		C _{rss}	—	45.4	144	
SWITCHING CHARACTERISTICS (2)						
Turn-On Delay Time	(R _{go} + C17n = 9.1 Ω)	t _{d(on)}	—	15	50	ns
Rise Time		t _r	—	33	72	
Turn-Off Delay Time		t _{d(off)}	—	40	150	
Fall Time		t _f	—	32	60	
Gate Charge (see Figure 8)	(V _{DS} = 400 Vdc, I _D = 8.0 Adc, V _{GS} = 10 Vdc)	Q _T	—	40	64	nC
		Q ₁	—	8.0	—	
		Q ₂	—	17	—	
		Q ₃	—	17.3	—	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage (I _S = 8.0 Adc, V _{GS} = 0 Vdc) (I _S = 8.0 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	— —	1.2 1.1	2.0 —	Vdc	
Reverse Recovery Time	(I _S = 8.0 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs)	t _{rr}	—	320	—	ns
		t _a	—	179	—	
		t _b	—	141	—	
Reverse Recovery Stored Charge		Q _{RR}	—	3.0	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)	L _D	—	4.5	—	nH	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L _S	—	7.5	—		

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

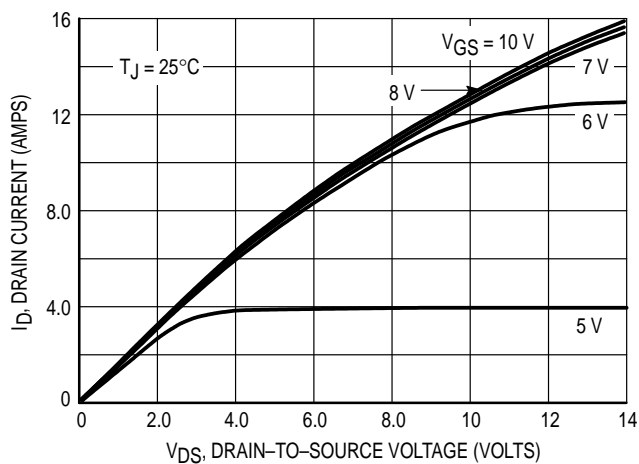


Figure 1. On-Region Characteristics

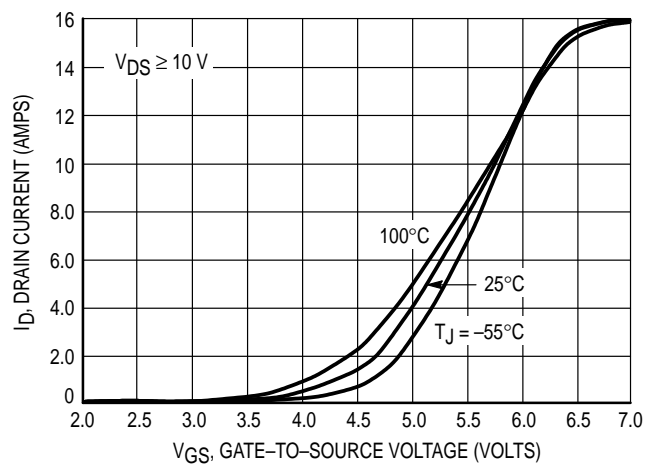


Figure 2. Transfer Characteristics

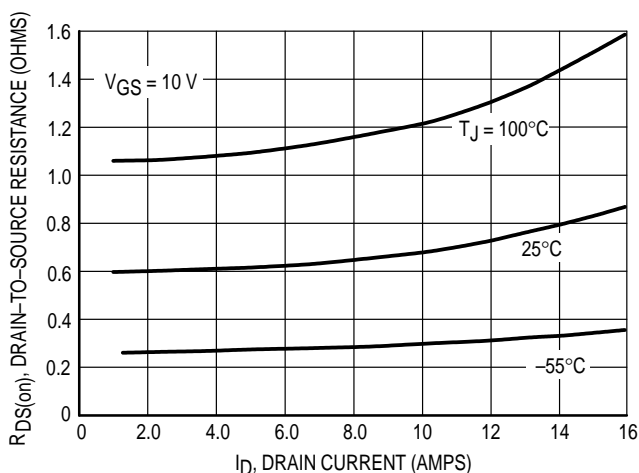


Figure 3. On-Resistance versus Drain Current and Temperature

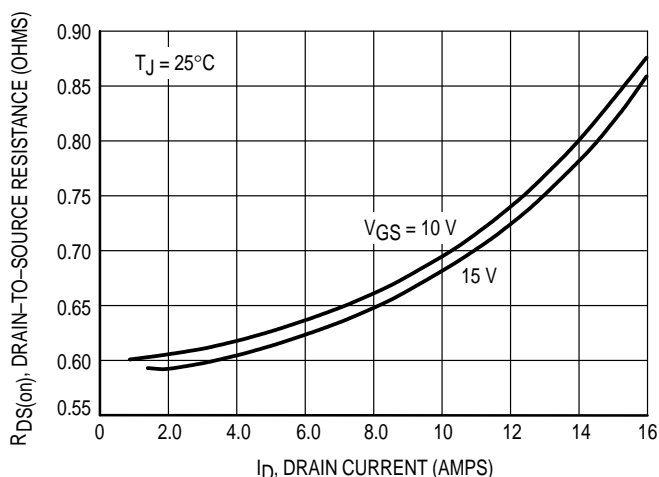


Figure 4. On-Resistance versus Drain Current and Gate Voltage

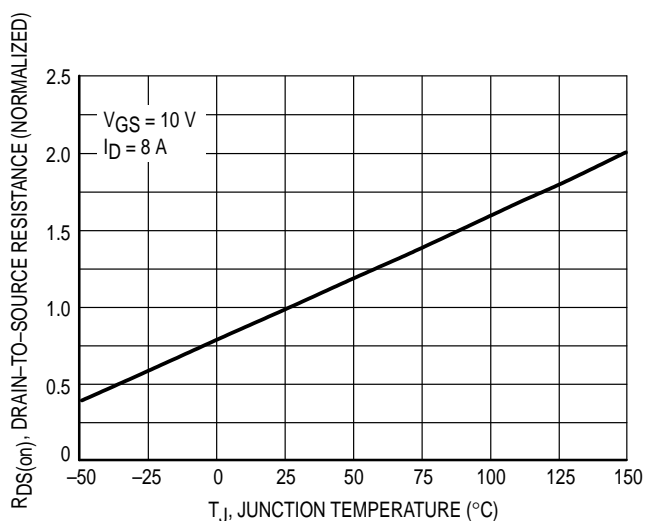


Figure 5. On-Resistance Variation with Temperature

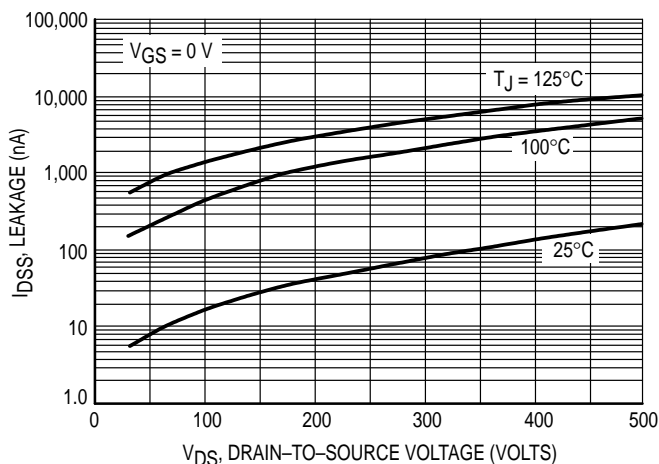


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

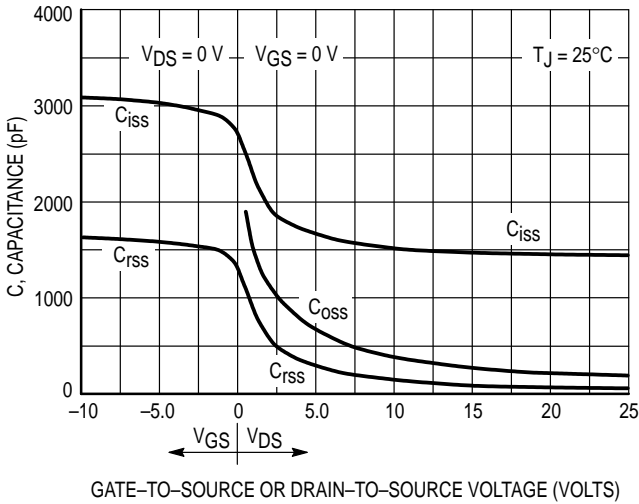


Figure 7. Capacitance Variation

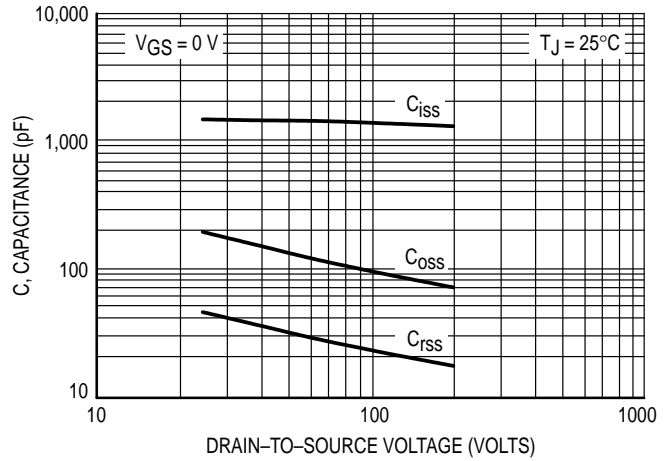


Figure 8. High Voltage Capacitance Variation

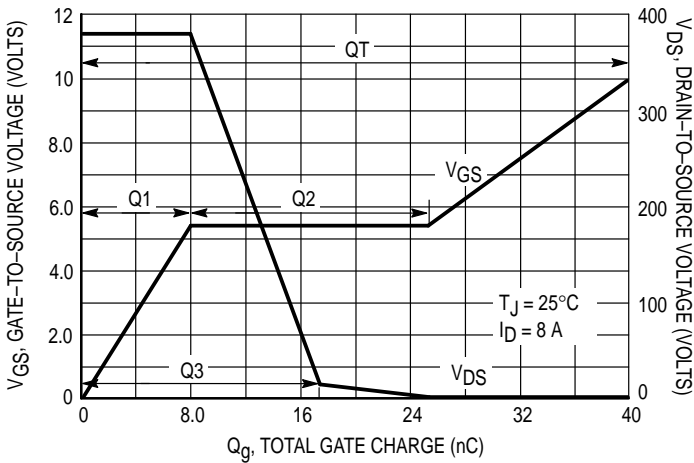


Figure 9. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

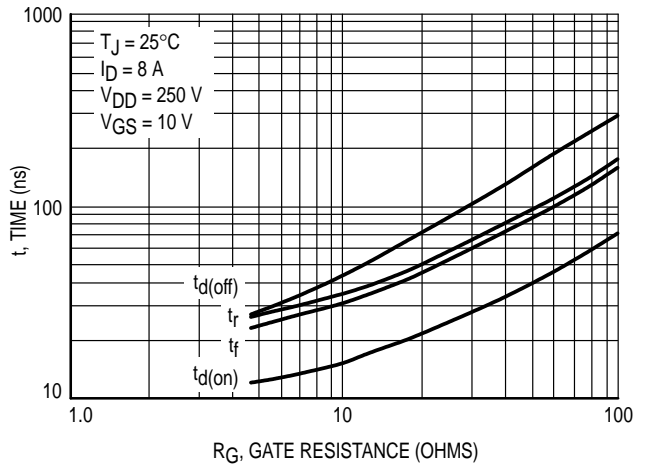


Figure 10. Resistive Switching Time Variation versus Gate Resistance

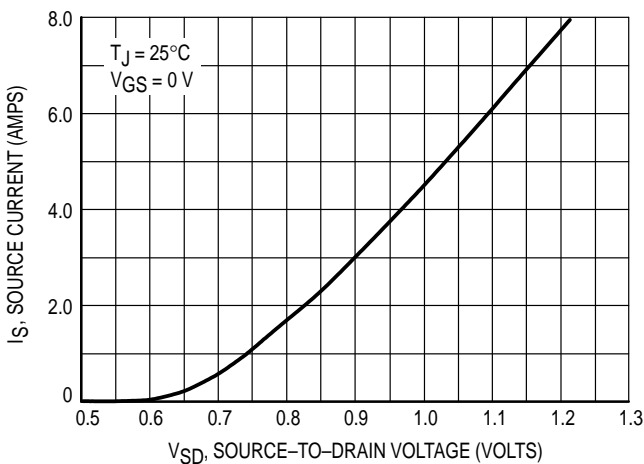


Figure 11. Diode Forward Voltage versus Current

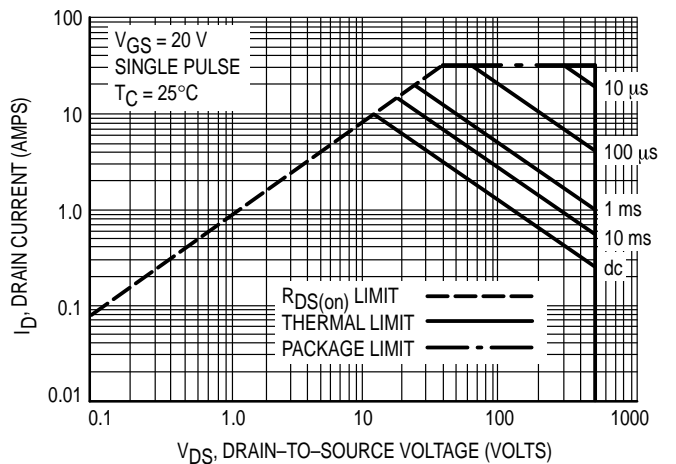


Figure 12. Maximum Rated Forward Biased Safe Operating Area

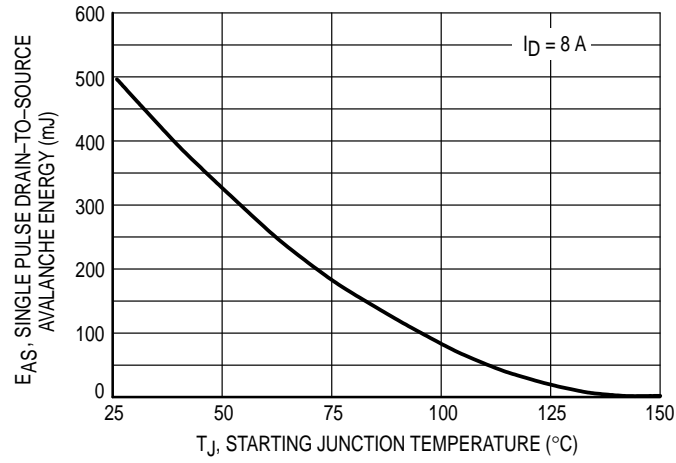


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

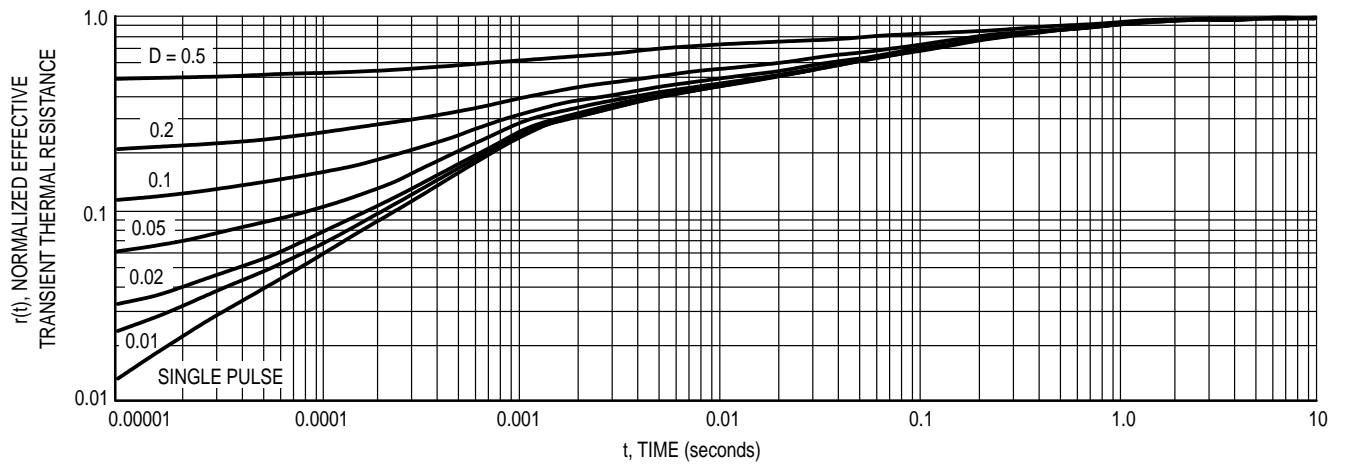
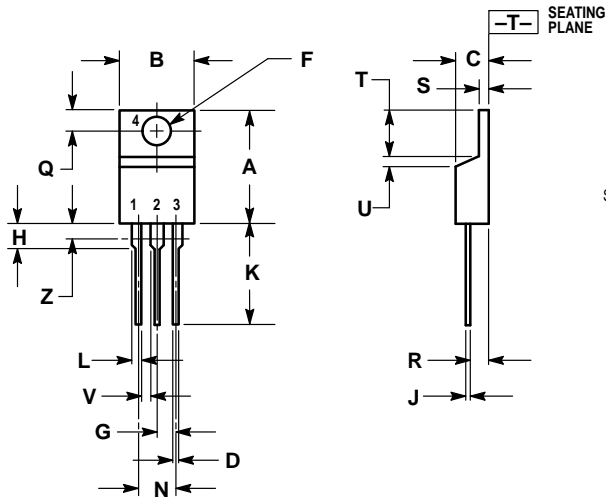


Figure 14. Thermal Response

PACKAGE DIMENSIONS



STYLE 5:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-06
 ISSUE Y

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