

# BIPOLAR DIGITAL INTEGRATED CIRCUIT

# $\mu$ PB1511TB

### 800 MHz INPUT DIVIDE BY 2, 4 PRESCALER IC FOR PORTABLE SYSTEMS

The  $\mu$ PB1511TB is a silicon monolithic integrated circuit designed as a divide by 2, 4 prescaler IC for portable radio systems. This IC is manufactured using NEC's 30 GHz  $f_{max}$  UHS0 (Ultra High Speed Process) silicon bipolar process.

Consequently, this IC is lower circuit current and smaller package than conventional  $\mu$ PB1509GV.

#### FEATURES

- Operating frequency :  $f_{in} = 50$  to 700 MHz @  $\div 2$ ,  
50 to 800 MHz @  $\div 4$
- Low current consumption : 3.5 mA @  $V_{CC} = 3.0$  V
- High-density surface mounting : 6-pin super minimold
- Supply voltage :  $V_{CC} = 2.4$  to 3.3 V
- Selectable division :  $\div 2, \div 4$

#### APPLICATIONS

- Portable radio systems
- Cellular/cordless telephone 2nd local prescaler

#### ORDERING INFORMATION

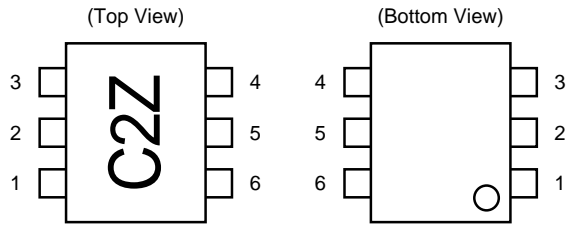
Part Number	Package	Marking	Supplying Form
$\mu$ PB1511TB-E3	6-pin super minimold	C2Z	Embossed tape 8 mm wide. Pin 1, 2, 3 face the tape perforation side. Qty 3 kpcs/reel.

**Remark** To order evaluation samples, please contact your local NEC sales office. (Part number for sample order:  $\mu$ PB1511TB)

**Caution Electro-static sensitive devices**

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

**PIN CONNECTIONS**



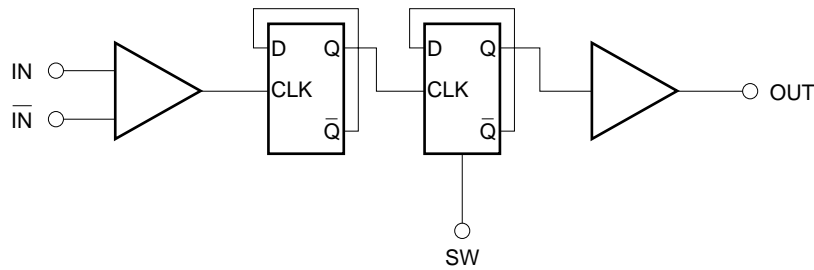
Pin No.	Pin Name
1	OUT
2	GND
3	SW
4	IN
5	$\overline{\text{IN}}$
6	V <sub>CC</sub>

**PRODUCT LINE-UP**

Part Number	I <sub>CC</sub> (mA)	V <sub>CC</sub> (V)	÷ 2 f <sub>in</sub> (MHz)	÷ 4 f <sub>in</sub> (MHz)	÷ 8 f <sub>in</sub> (MHz)	Package
μPB1509 GV	5.0	2.2 to 5.5	50 to 700	50 to 800	50 to 1 000	8-pin SSOP
μPB1511TB	3.5	2.4 to 3.3	50 to 700	50 to 800	–	6-pin super minimold

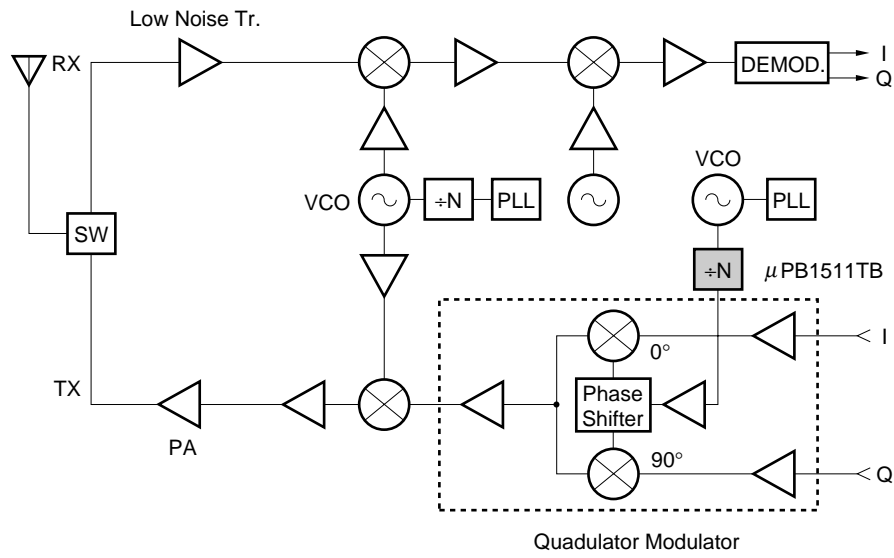
**Remark** This table shows the TYP. values of main parameters. Please refer to ELECTRICAL CHARACTERISTICS.

**INTERNAL BLOCK DIAGRAM**



SYSTEM APPLICATION EXAMPLE

One of the example for usage



This block diagram schematically shows the  $\mu$ PB1511TB's location in one of the example application system. The other applications are also acceptable for divider use.

**PIN EXPLANATIONS**

Pin No.	Symbol	Applied Voltage (V)	Functions and Explanation									
1	OUT	—	Divided frequency output pin. This pin is designed as emitter follower output. This pin can output 0.2 V <sub>P-P</sub> MIN. with 200 Ω load. This pin should be coupled to load device with capacitor (example: 1 000 pF) for DC cut.									
2	GND	0	Ground pin. Ground pattern on the board should be formed as widely as possible to minimize ground impedance.									
3	SW	H/L	Divide ratio control pin. Divide ratio can be determined by following applied level to these pins. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th colspan="2">SW</th> </tr> <tr> <th></th> <th>H</th> <th>L</th> </tr> </thead> <tbody> <tr> <th>Divide ratio</th> <td>1/2</td> <td>1/4</td> </tr> </tbody> </table> <p>These pins must be each equipped with bypass capacitor to minimize their impedance.</p>		SW			H	L	Divide ratio	1/2	1/4
	SW											
	H	L										
Divide ratio	1/2	1/4										
4	IN	—	Signal input pin. This pin should be coupled to signal source with capacitor (example: 1 000 pF) for DC cut.									
5	$\overline{\text{IN}}$	—	Signal input bypass pin. This pin must be equipped with bypass capacitor (example: 1 000 pF) to minimize ground impedance.									
6	V <sub>CC</sub>	2.4 to 3.3	Power supply pin. This pin must be equipped with bypass capacitor (example: 1 000 pF) to minimize ground impedance.									

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V <sub>CC</sub>	T <sub>A</sub> = +25°C	3.6	V
Input Voltage	V <sub>in</sub>	T <sub>A</sub> = +25°C, SW pin	3.6	V
Total Power Dissipation	P <sub>D</sub>	Mounted on double sided copper clad 50 × 50 × 1.6 mm epoxy glass PWB (T <sub>A</sub> = +85°C)	200	mW
Operating Ambient Temperature	T <sub>A</sub>		-40 to +85	°C
Storage Temperature	T <sub>stg</sub>		-55 to +150	°C

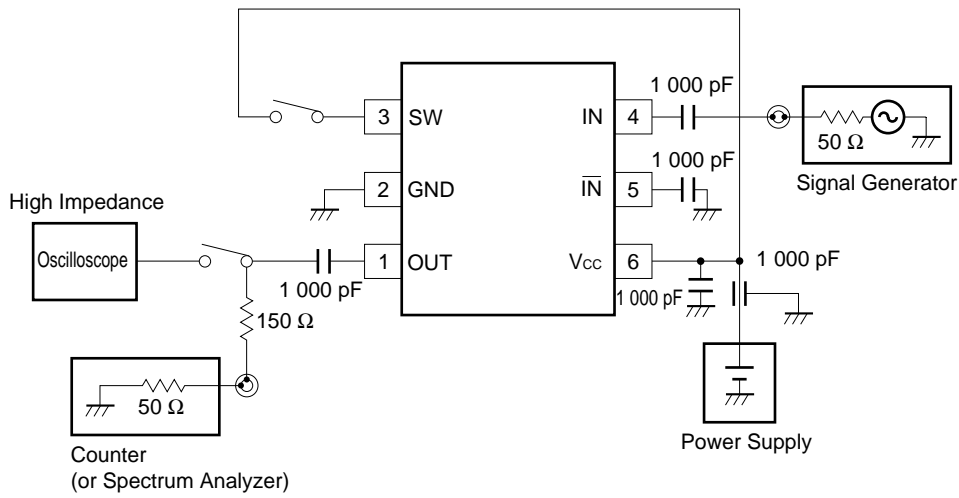
**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V <sub>CC</sub>	2.4	3.0	3.3	V
Operating Ambient Temperature	T <sub>A</sub>	-40	+25	+85	°C

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = +25°C, V<sub>CC</sub> = 3.0 V)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I <sub>CC</sub>	No signals	3.1	3.5	4.1	mA
Upper Limit Operating Frequency 1	f <sub>in(U)1</sub>	P <sub>in</sub> = -20 to 0 dBm	500	—	—	MHz
Upper Limit Operating Frequency 2	f <sub>in(U)2</sub>	P <sub>in</sub> = -20 to -5 dBm @ ÷ 2 @ ÷ 4	700 800	—	—	MHz
Lower Limit Operating Frequency 1	f <sub>in(L)1</sub>	P <sub>in</sub> = -20 to 0 dBm	—	—	50	MHz
Lower Limit Operating Frequency 2	f <sub>in(L)2</sub>	P <sub>in</sub> = -20 to -5 dBm	—	—	500	MHz
Input Power 1	P <sub>in1</sub>	f <sub>in</sub> = 50 to 800 MHz	-20	—	-5	dBm
Input Power 2	P <sub>in2</sub>	f <sub>in</sub> = 50 to 500 MHz	-20	—	0	dBm
Output Voltage	V <sub>out</sub>	R <sub>L</sub> = 200 Ω	0.2	0.3	—	V <sub>P-P</sub>
Divide Ratio Control Input High	V <sub>IH</sub>		0.7 × V <sub>CC</sub>	—	V <sub>CC</sub> + 0.5	V
Divide Ratio Control Input Low	V <sub>IL</sub>		-0.5	—	V <sub>CC</sub> × 0.3	V

TEST CIRCUIT

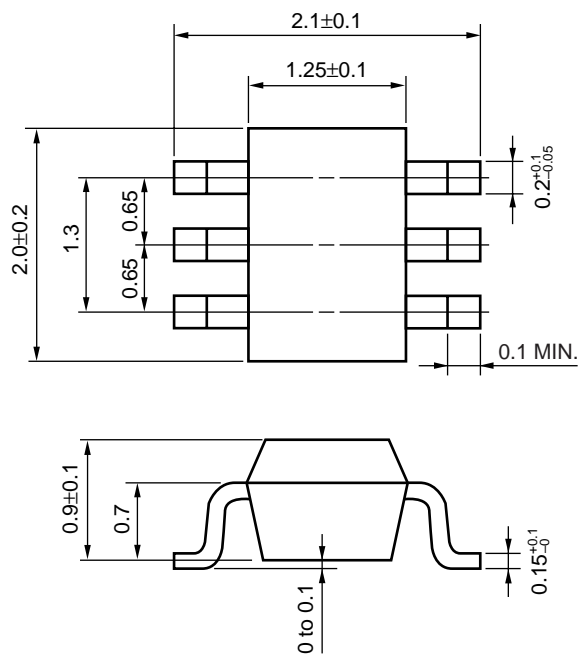


Divide Ratio Setting

SW	H	1/2
	L	1/4

PACKAGE DIMENSIONS

6-pin super minimold (Unit: mm)



**NOTE ON CORRECT USE**

- (1) Observe precautions for handling because of electrostatic sensitive devices.
- (2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation).  
Keep the track length of the ground pins as short as possible.
- (3) Connect a bypass capacitor (example: 1 000 pF) to the Vcc pin.

**RECOMMENDED SOLDERING CONDITIONS**

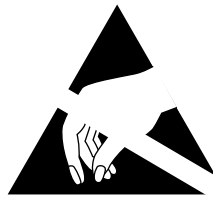
This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None <sup>Note</sup>	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None <sup>Note</sup>	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None <sup>Note</sup>	WS60-00-1
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit: None <sup>Note</sup>	—

**Note** After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

**Caution** Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).



## ATTENTION

OBSERVE PRECAUTIONS  
FOR HANDLING  
ELECTROSTATIC  
SENSITIVE  
DEVICES

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