DATA SHEET

UBA1710M
Modulator for GaAs power amplifiers

Product specification
Supersedes data of 1997 Feb 18
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Modulator for GaAs power amplifiers UBA1710M

FEATURES

- Power MOS modulators for control of GaAs power amplifier drain voltage
- Power control loop amplifier and MOS driver
- Voltage tripler for supply of MOS driver
- Positive-to-negative DC converter for GaAs power amplifier gate biasing.

APPLICATIONS

- Control of GaAs power amplifiers for GSM and DCS hand-held transceivers.

GENERAL DESCRIPTION

The UBA1710M integrates the functions required to operate the GaAs Power Amplifiers (PAs) from the CGY20xx family which are intended for GSM and DCS applications.

It includes a negative supply for PA gate biasing and most of the functions required to implement power control so that only a very few external component are required. The power control section integrates two power MOS devices for control of the PA drain voltages, an MOS driver and a feedback loop amplifier. The MOS driver is supplied from an on-chip voltage tripler.

QUICK REFERENCE DATA

SYMBOL	PARAMETER(1)	MIN.	TYP.	MAX.	UNIT
V_{CC}	analog supply voltage	4.2	4.8	7.5	V
V_{DD}	digital supply voltage	4.2	4.8	7.5	V
$I_{CC} + I_{DD}$	peak supply current in power-up mode	–	12	–	mA
T_{amb}	operating ambient temperature	–20	–	+85	°C

Note

1. For conditions, see Chapter “Characteristics”.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UBA1710M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

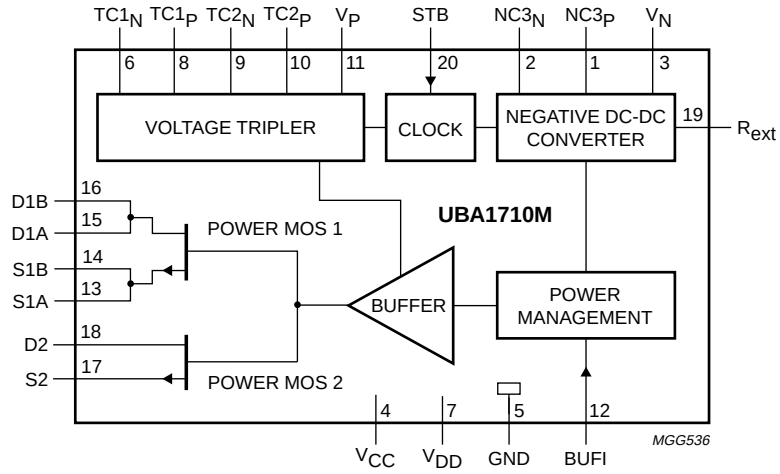


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$NC3_P$	1	charge pump tank capacitor
$NC3_N$	2	charge pump tank capacitor
V_N	3	negative bias voltage
V_{CC}	4	analog supply voltage
GND	5	ground
$TC1_N$	6	charge pump tank capacitor
V_{DD}	7	digital supply voltage
$TC1_P$	8	charge pump tank capacitor
$TC2_N$	9	charge pump tank capacitor
$TC2_P$	10	charge pump tank capacitor
V_P	11	positive tripler voltage
BUFI	12	buffer input
S1A	13	power MOS 1 source A
S1B	14	power MOS 1 source B
D1A	15	power MOS 1 drain A
D1B	16	power MOS 1 drain B
S2	17	power MOS 2 source
D2	18	power MOS 2 drain
R_{ext}	19	external resistance for V_N
STB	20	standby input (active HIGH)

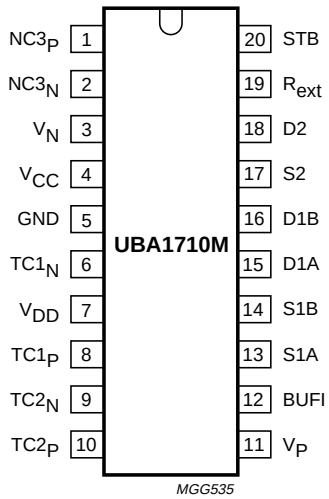


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Power control section

Power control for GaAs PAs from the CGY20xx family is achieved by varying the drain voltage. This is achieved with the UBA1710M by means of the two power MOS devices integrated on-chip. They enable separate control of the PA output stage from the pre-amplifier stages. They have a very low 'on' resistance for low drop voltage at high RF output power.

The MOS devices are driven by a buffer. The buffer amplifier, in association with power MOS, is included in a feedback loop to exhibit a high cut-off frequency (3 MHz) over the whole control dynamic range. This buffer allows fast switching of the MOS in accordance with GSM power ramping requirements.

DC-DC converters

One DC-DC converter is required to provide negative gate biasing to the GaAs PA.

The standard value is typically −2 V, without any external resistor connected. The other one is a voltage tripler and is required to supply the MOS driver. The driver is required to raise the MOS gate voltage well above the battery voltage in order to open the MOS switches ('high side' driver).

These DC-DC converters are operated at a typical frequency of 600 kHz supplied by an internal oscillator. Five external capacitors with a typical value of 0.1 μF (0603 SMD) are required to operate these converters.

Power management

The power management disables the PA drain voltage and prevents the PA from burnout if drain voltage is supplied before the negative gate voltage is available.

Standby mode

An additional feature includes a standby mode, reducing the current consumption to a maximum value of 1 μA.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	analog supply voltage	−0.5	+9.0	V
V_{DD}	digital supply voltage	−0.5	+9.0	V
V_I	DC input voltage			
	all pins (except BUFI)	−0.5	+9.0	V
	pin BUFI	−0.5	+5.0	V
I_I	DC current into any signal pin	−10	+10	mA
P_{tot}	total power dissipation	−	0.65	W
T_{stg}	storage temperature	−65	+150	°C
T_{amb}	operating ambient temperature	−20	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	100	K/W

CHARACTERISTICS

$V_{CC} = V_{DD} = 4.8$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$I_{CC} + I_{DD}$	peak supply current	power-up mode; PA on	–	12	–	mA
		power-down mode; PA off	–	5	–	mA
I_{stb}	standby current	standby mode	–	0.1	1	µA
Power MOS 1						
R_{DSon1}	on resistance	$I_{DS} = 1.3$ A	–	0.18	–	Ω
Power MOS 2						
R_{DSon2}	on resistance	$I_{DS} = 0.4$ A	–	0.5	–	Ω
Clock circuit						
f_{clk}	clock frequency		–	600	–	kHz
Voltage tripler						
V_{Po}	output voltage	with $I_{Po} = 2$ mA	11.3	11.8	12.3	V
$V_{R(p-p)}$	amplitude ripple (peak-to-peak value)	with $I_{Po} = 2$ mA; C1 = C2 = 100 nF; $C_P = 100$ nF	–	20	–	mV
t_{on}	turn-on time		–	100	–	µs
Negative DC/DC converter						
V_{No}	output voltage	with $I_{No} = 250$ µA; $R_{ext} = 470$ kΩ	–1.5	–1.8	–2.0	V
$V_{R(p-p)}$	amplitude ripple (peak-to-peak value)	with $I_{No} = 250$ µA; C3 = 100 nF; $C_N = 100$ nF	–	2	–	mV
t_{on}	turn-on time		–	280	–	µs
MOS buffer amplifier						
V_{IL}	LOW level input voltage		–	1.2	–	V
V_{IH}	HIGH level input voltage		–	3.4	–	V
t_{sw}	switching time from 0 to 4.5 V	2 Ω load at MOS outputs	–	1	–	µs

APPLICATION INFORMATION

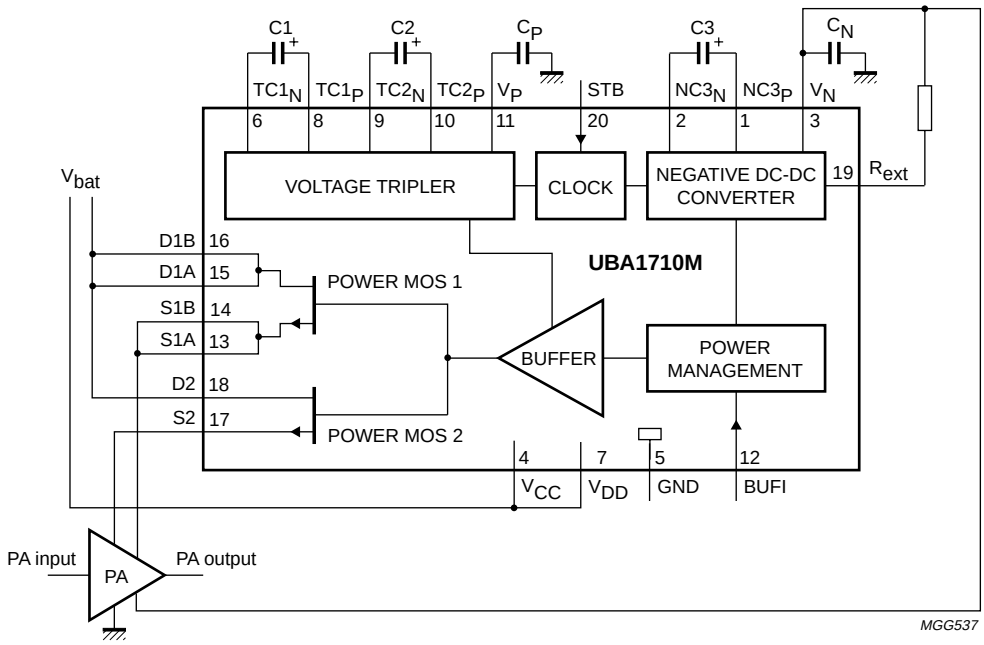
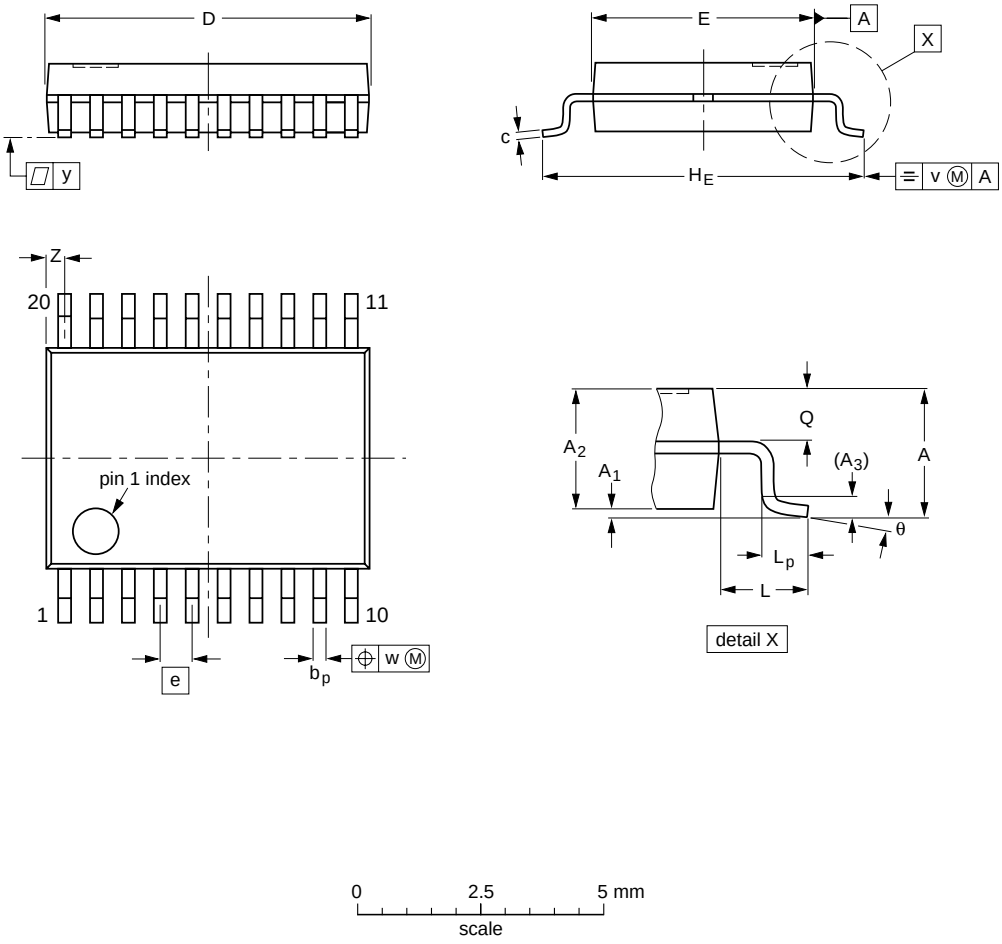


Fig.3 Application diagram.

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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