# DATA SHEET

# UBA1706
## Cordless telephone line interface

Objective specification
Supersedes data of 1999 Mar 08
File under Integrated Circuits, IC17

1999 Jun 04

Philips
Semiconductors

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# Cordless telephone line interface UBA1706

## FEATURES

### Line interface

- Low DC line voltage; operates down to 1.2 V (excluding polarity guard)
- Voltage regulator with adjustable DC voltage
- DC mask for voltage or current regulation (CTR21)
- Line current limitation for protection
- Electronic hook switch control input
- Transmit amplifier with:
  - Symmetrical inputs
  - Fixed gain
  - Large signal handling capability.
- Receive amplifier with fixed gain
- Transmit and receive amplifiers Automatic Gain Control (AGC) for line loss compensation.

### General purpose switches

Two switches with open-collector.

### 3-wire serial bus interface

Allows control of:

- DC mask (voltage or current regulation)
- Receive amplifier mute function
- AGC:
  - On/off
  - Slope
  - $I_{start}$ line current.
- The state of the general purpose switches
- Global power-down mode.

### Supply

Operates with external supply voltage from 3.0 to 5.5 V.

## APPLICATIONS

- Cordless base stations
- Mains or battery-powered telephone sets.

## GENERAL DESCRIPTION

The UBA1706 is a BiCMOS integrated circuit intended for use in mains-powered telecom terminals. It performs all speech and line interface functions, DC mask for voltage or current regulation and electronic hook switch control. The device also includes general purpose switches.

Most of the characteristics are programmable via a 3-wire serial bus interface.

## ORDERING INFORMATION

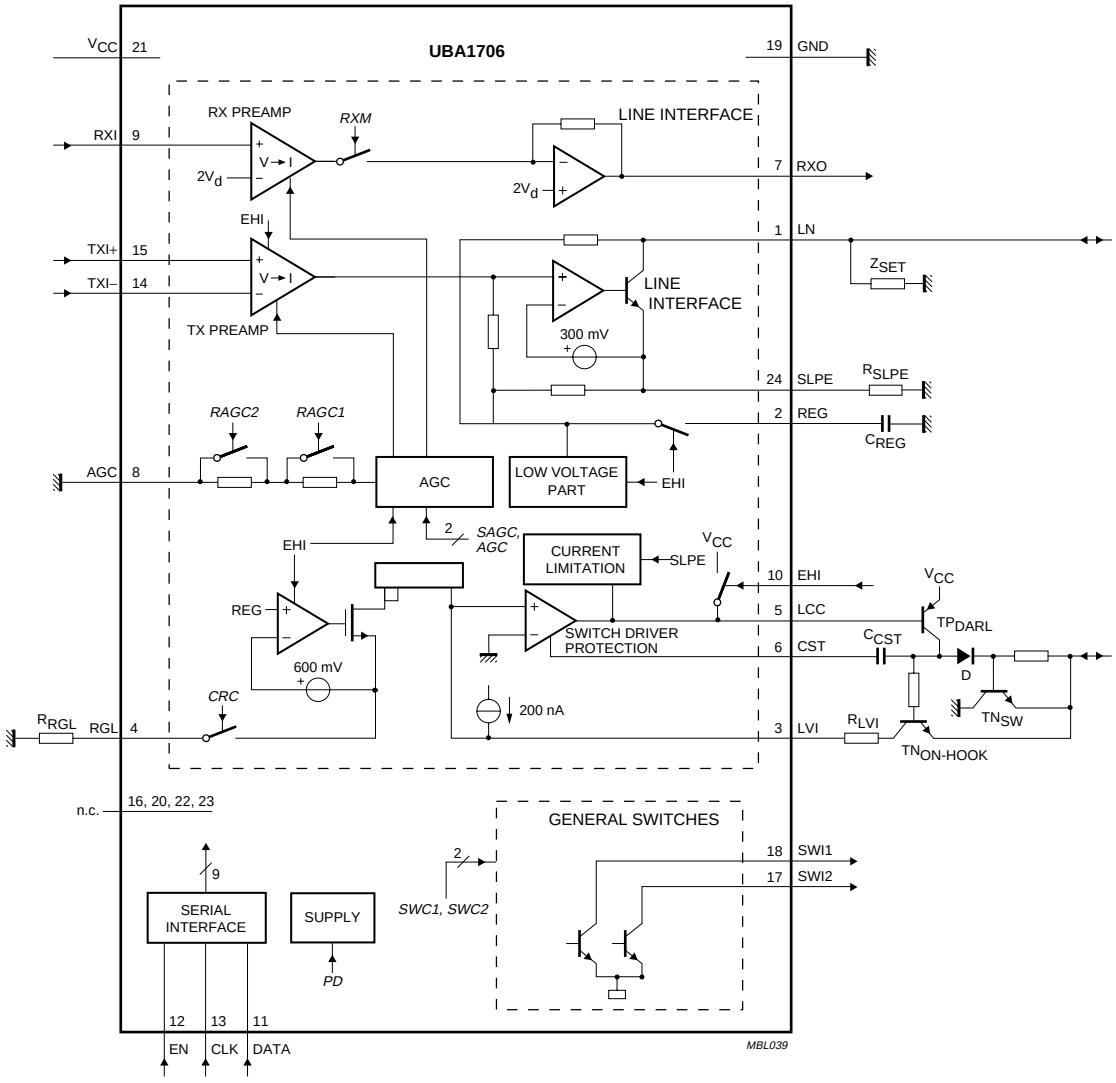
| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| UBA1706TS | SSOP24 | plastic shrink small outline package; 24 leads; body width 5.3 mm | SOT340-1 |

## QUICK REFERENCE DATA

$I_{line}$ = 15 mA; $V_{CC}$ = 3.3 V; $R_{SLPE}$ = 10 Ω; AGC pin connected to GND; $Z_{line}$ = 600 Ω; $Z_{SET}$ = 619 Ω; EHI = HIGH; f = 1 kHz; $T_{amb}$ = 25 °C; bit AGC at logic 1, all other configuration bits at logic 0; measured in the test circuit of Fig.14; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 3.0 | – | 5.5 | V |
| $I_{CC}$ | current consumption from pin $V_{CC}$ | normal operation; bit PD = 0 | – | 2.2 | 3.2 | mA |
| | | power-down mode; bit PD = 1 | – | 110 | 150 | μA |
| $I_{line}$ | line current operating range | normal operation | 11 | – | 140 | mA |
| | | with reduced performance | 3 | – | 11 | mA |
| $V_{LN}$ | DC line voltage | | 2.7 | 3.0 | 3.3 | V |
| $R_{REGC}$ | DC mask slope in current regulation mode | $I_{line}$ > 35 mA (typical); $R_{LVI}$ = 1 MΩ; $R_{RGL}$ = 7.15 kΩ; bit CRC = 1 | – | 1.4 | – | kΩ |
| $G_{v(trx)}$ | voltage gain | | | | | |
| | transmit amplifier from TXI to LN | $V_{TXI}$ = 50 mV (RMS) | 10.6 | 11.6 | 12.6 | dB |
| | receive amplifier from RXI to RXO | $V_{RXI}$ = 2 mV (RMS) | 36.9 | 37.9 | 38.9 | dB |
| $\Delta G_{v(trx)}$ | gain control range for transmit and receive amplifiers with respect to $I_{line}$ = 15 mA | $I_{line}$ = 90 mA | – | 6.5 | – | dB |

## BLOCK DIAGRAM




Bit names are given in italics.

Fig.1 Block diagram.

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| LN | 1 | positive line terminal |
| REG | 2 | line voltage regulator decoupling |
| LVI | 3 | negative line voltage sense input |
| RGL | 4 | reference for current regulation mode |
| LCC | 5 | line current control output |
| CST | 6 | input for stability capacitor |
| RXO | 7 | receive amplifier output |
| AGC | 8 | automatic gain control/line loss compensation adjustment |
| RXI | 9 | receiver amplifier input |
| EHI | 10 | electronic hook switch control input |
| DATA | 11 | serial bus data input |
| EN | 12 | programming serial bus enable input |
| CLK | 13 | serial bus clock input |
| TXI– | 14 | inverted transmit amplifier input |
| TXI+ | 15 | non-inverted transmit amplifier input |
| n.c. | 16 | not connected |
| SWI2 | 17 | NPN open-collector output 2 |
| SWI1 | 18 | NPN open-collector output 1 |
| GND | 19 | ground reference |
| n.c. | 20 | not connected |
| $V_{CC}$ | 21 | supply voltage |
| n.c. | 22 | not connected |
| n.c. | 23 | not connected |
| SLPE | 24 | connection for slope resistor |

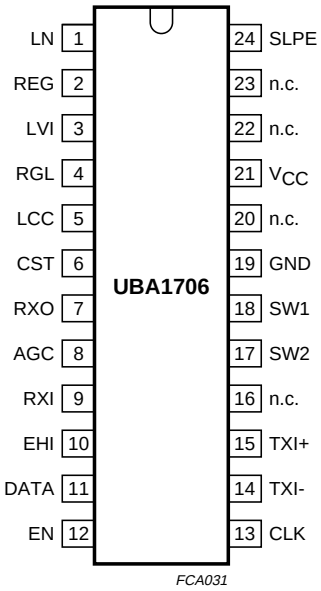



Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

All data given in this chapter consists of typical values, except when otherwise specified.

### Supply (pins $V_{CC}$ and GND; bit PD)

The UBA1706 must be supplied with an external stabilized voltage source across pins $V_{CC}$ and GND.

Without any signal and without any general purpose switch selected, the internal current consumption is 2.2 mA at $V_{CC}$ = 3.3 V. Each selected switch (pins SWI1 or SWI2) increases the current consumption by 600 μA.

To drastically reduce current consumption, the UBA1706 is provided with a power-down mode controlled by bit PD. When bit PD is at logic 1, the current consumption from $V_{CC}$ becomes 110 μA. In the power-down mode, the serial interface is the only function which remains active.

### Line interface

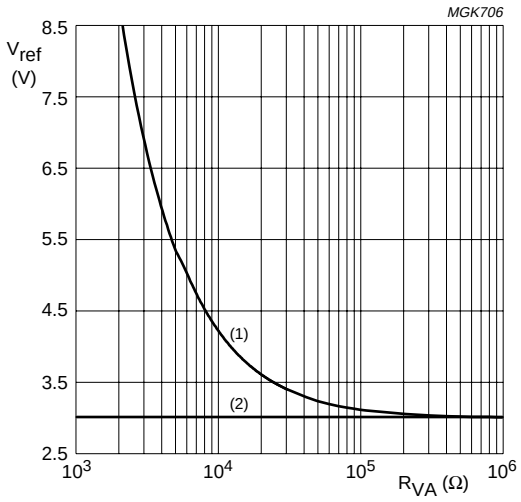
DC CHARACTERISTICS (PINS LN, SLPE, REG, CST, LVI, LCC, RGL AND GND; BIT CRC)

The IC generates a stabilized reference voltage ($V_{ref}$) across pins LN and SLPE. This reference voltage is equal to 2.9 V, is temperature compensated and can be adjusted by means of an external resistor ($R_{VA}$). The reference voltage can be increased by connecting the $R_{VA}$ resistor between pins REG and SLPE (see Fig.3).

The voltage at pin REG is used by the internal regulator to generate the stabilized reference voltage and is decoupled by a capacitor ($C_{REG}$) which is connected to GND. This capacitor, converted to an equivalent inductance (see Section “Set impedance”) realizes the set impedance conversion from its DC value ($R_{SLPE}$) to its AC value ($Z_{SET}$ in the audio frequency range). Figure 4 illustrates the reference voltage supply configuration. As can be seen from Fig.4, part of the line current flows into the $Z_{SET}$ impedance network and is not sensed by the UBA1706. Therefore, using the $R_{VA}$ resistor to change the value of the reference voltage will also modify all parameters related to the line current such as:

- The AGC
- The DC mask management
- The low voltage area characteristics.

In the same way, changing the value of $Z_{SET}$ also affects the characteristics. The IC has been optimized for $V_{ref}$ = 2.9 V and $Z_{SET}$ = 619 Ω.




(1) Influence of $R_{VA}$ on $V_{ref}$.
(2) $V_{ref}$ without influence of $R_{VA}$.

Fig.3 Reference voltage adjustment with $R_{VA}$.

The IC regulates the line voltage at pin LN, which can be calculated as follows:

$$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$$

$$I_{SLPE} = I_{line} - I_{ZSET} - I^* \cong I_{line} - I_{ZSET}$$

Where:

$I_{line}$ = line current

$I_{ZSET}$ = current flowing through $Z_{SET}$

I* = current consumed between LN and GND (approximately 100 μA).

The preferred value for $R_{SLPE}$ is 10 Ω. Changing $R_{SLPE}$ will affect more than the DC characteristics; it also influences the transmit gain, the gain control characteristics, the sidetone level and the maximum output swing on the line.

Nevertheless, for compliance with CTR21, 8.66 Ω is the optimum value for $R_{SLPE}$.

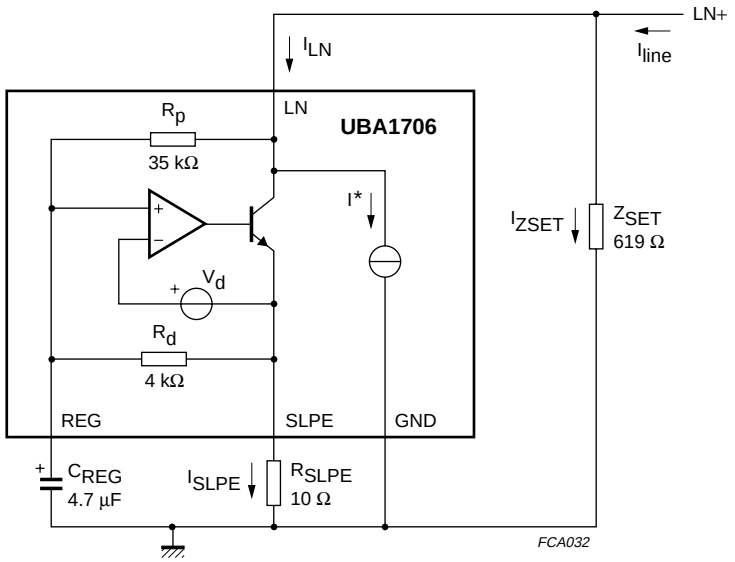



Fig.4 Reference voltage supply configuration.

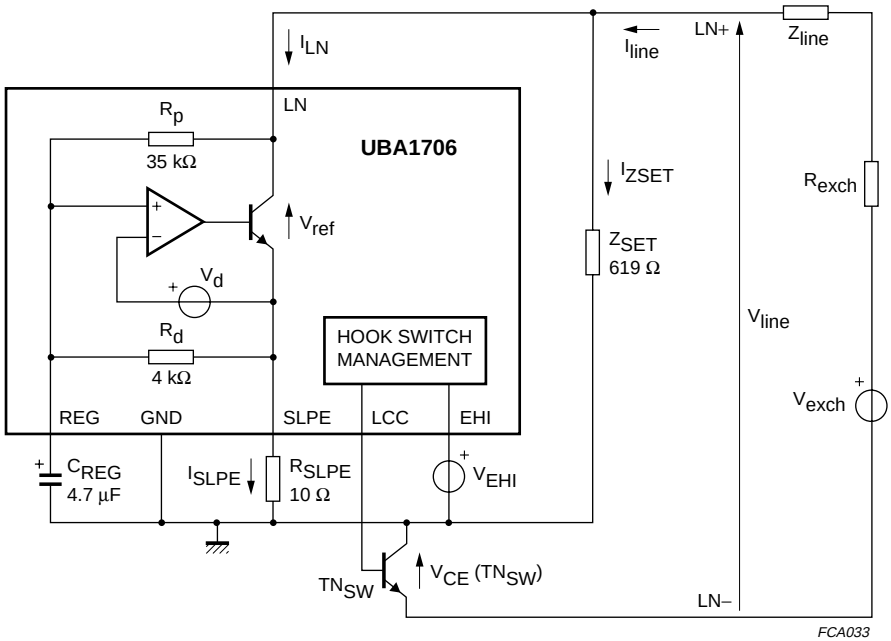



Fig.5 Line current settling simplified configuration.

The DC line current flowing into the set is determined by the exchange supply voltage ($V_{exch}$), the feeding bridge resistance ($R_{exch}$), the DC resistors of the telephone line ($R_{line}$) and the set ($R_{SET}$), the reference voltage ($V_{ref}$) and the voltage introduced by the transistor ($TN_{SW}$) used as line interrupter (see Fig.5).

With a line current below $I_{low}$ (8 mA with $Z_{SET}$ = 619 Ω), the internal reference voltage ($V_{ref}$) is automatically adjusted to a lower value. This means that several sets can operate in parallel with DC line voltages (excluding the polarity guard) down to 1.2 V. With a line current below $I_{low}$, the circuit has limited transmit and receive levels. This is called the low voltage area.

Figure 6 shows in more detail how the UBA1706, in association with some external components, manages the line interrupter ($TN_{SW}$ external transistor).

In on-hook conditions (voltage at pin EHI is LOW), the voltage at pin LCC is pulled up to the supply voltage level ($V_{CC}$) to turn off transistor $TP_{DARL}$. As a result, because of resistor $R_{PD}$, transistors $TN_{SW}$ and $TN_{ON\text{-}HOOK}$ are switched off. Transistor $TN_{ON\text{-}HOOK}$ disconnects resistor $R_{LVI}$ from the LN– line terminal to guarantee a high on-hook impedance.

In off-hook conditions (voltage at pin EHI is HIGH), an operational amplifier drives (at pin LCC) the base of transistor $TP_{DARL}$, which forms a current amplifier structure in association with $TN_{SW}$. The line current flows through transistor $TN_{SW}$. Transistor $TN_{ON\text{-}HOOK}$ is forced into deep saturation. A virtual ground is created at pin LVI because of the operational amplifier. A DC current ($I_{LVI}$) is sourced from pin LVI into the $R_{LVI}$ resistor to generate a voltage source. Thus, the voltage across pins GND and LN– becomes:

$$V_{CE}(TN_{SW}) = R_{LVI} \times I_{LVI} + V_{CE}(TN_{ON\text{-}HOOK}) \cong R_{LVI} \times I_{LVI}$$

The voltage $V_{line}$ across line terminals LN+ and LN– can be calculated as follows:

$$V_{line} \cong V_{ref} + R_{SLPE} \times (I_{line} - I_{ZSET}) + V_{CE}(TN_{SW})$$

Where:

$I_{line}$ = line current

$I_{ZSET}$ = current flowing through $Z_{SET}$.

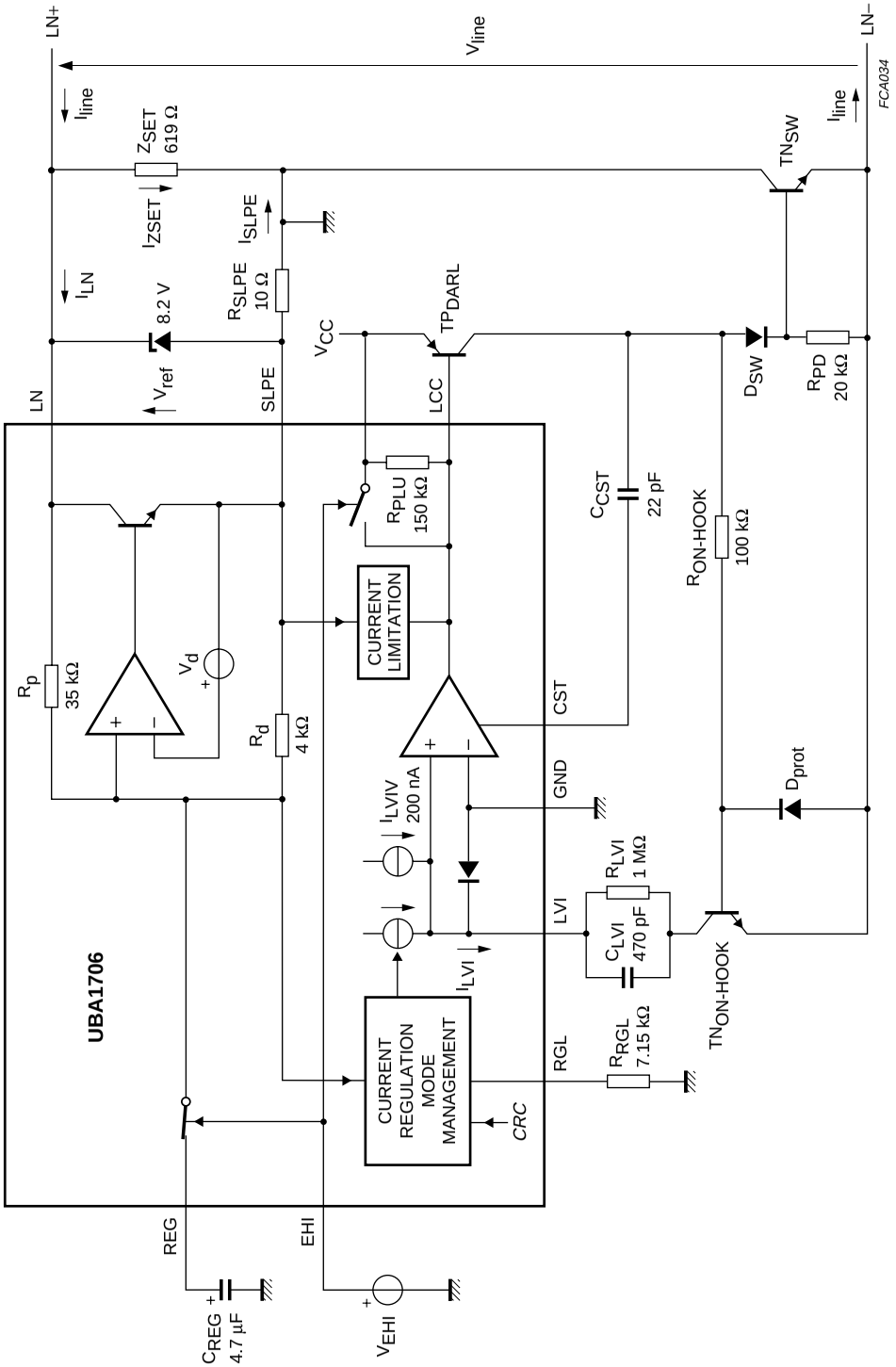
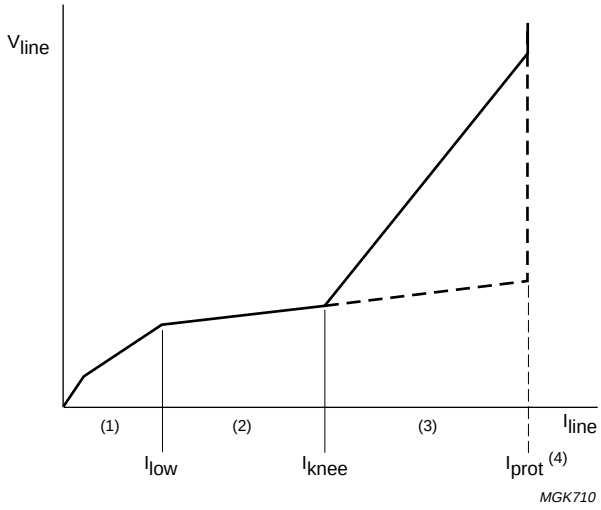



Fig.6 Line interrupter management and DC mask regulation configuration.

Bit names are given in italics.

The UBA1706 offers the possibility to choose two kinds of regulations for the DC characteristic between line terminals LN+ and LN– (see Fig.7):

- Voltage regulation mode
- Current regulation mode.




(1) Low voltage area.
(2) Small slope (determined by $R_{SLPE}$).
(3) Small slope (dashed line; determined by $R_{SLPE}$) in voltage regulation mode.
High slope (full line; determined by $R_{SLPE}$, $R_{LVI}$ and $R_{RGL}$) in current regulation mode.
(4) Current limitation.

Fig.7 General form of the DC mask as a function of the regulation mode.

The regulation mode is selected by bit CRC via the serial interface.

The DC mask regulation is realised by adjusting the DC voltage $V_{CE}$ ($TN_{SW}$) across pin GND and line terminal LN– as a function of the line current.

*Voltage regulation mode*

In the voltage regulation mode (bit CRC at logic 0), the $V_{CE}$ ($TN_{SW}$) voltage is fixed by means of a 200 nA DC constant current $I_{LVIV}$ flowing through $R_{LVI}$.

Therefore, $V_{CE}$ ($TN_{SW}$) $\cong R_{LVI} \times I_{LVIV}$ = 200 mV in a typical application (see Fig.15).

The slope $\Delta V_{line}/\Delta I_{line}$ of the $V_{line}$, $I_{line}$ characteristic is $R_{REGV} \cong R_{SLPE}$.

*Current regulation mode*

In current regulation mode (bit CRC at logic 1), when the line current is lower than $I_{knee}$ = 35 mA (with $Z_{SET}$ = 619 Ω), $V_{CE}$ ($TN_{SW}$) is fixed by means of a 200 nA DC constant current $I_{LVIV}$ flowing through $R_{LVI}$. When the line current is higher than 35 mA, an additional current (proportional to the line current) flows through $R_{LVI}$. As a result, $TN_{SW}$ works as a DC voltage source increasing with the line current. $V_{CE}$ ($TN_{SW}$) can be calculated as follows:

$$V_{CE}(TN_{SW}) \cong R_{LVI} \times \left( \frac{R_{SLPE}}{R_{RGL}} \times (I_{line} - I_{knee}) + I_{LVIV} \right)$$

Where:

$I_{line}$ = line current

$R_{RGL}$ = resistor connected at pin RGL.

In a typical application (see Fig.15), the slope $\Delta V_{line}/\Delta I_{line}$ of the $V_{line}$, $I_{line}$ characteristic is determined by the ratio of the resistors connected at pins SLPE, LVI and RGL, as follows:

$$R_{REGC} \cong R_{SLPE} + R_{LVI} \times \frac{R_{SLPE}}{R_{RGL}} = 1400\ \Omega .$$

*Current limitation*

Whatever the selected mode is, the line current is limited to approximately 145 mA; this current is sensed on SLPE. For this purpose, the external Zener diode must be connected between pins LN and SLPE. The speech function no longer operates in this condition.

ELECTRONIC HOOK SWITCH CONTROL (PIN EHI)

The electronic hook switch input (EHI) controls the state of transistor $TP_{DARL}$. When the voltage applied at pin EHI is LOW, transistor $TP_{DARL}$ is turned off. The voltage at pin LCC is pulled up to supply voltage ($V_{CC}$). Transistors $TN_{SW}$ and $TN_{ON\text{-}HOOK}$ are also turned off by means of a pull-down resistor ($R_{PD}$). When the voltage applied at pin EHI is HIGH, transistor $TP_{DARL}$ is driven by the operational amplifier at pin LCC and the regulation mode selected is operating. An internal 165 kΩ pull-up resistor is connected between pins LCC and $V_{CC}$.

Input EHI can also be used for pulse dialling or register recall (timed loop break). During line breaks (the voltage at pin EHI is LOW or open-circuit), the voltage regulator is switched off and the capacitor at pin REG is internally disconnected to prevent its discharge. As a result, the voltage stabilizer will have negligible switch-on delay after line interruptions. This minimizes the contribution of the IC to the current waveform during pulse dialling or register recall.

When the UBA1706 is in power-down mode (bit PD at logic 1), transistor $TP_{DARL}$ is forced off whatever the voltage applied at pin EHI.

### SET IMPEDANCE

In the audio frequency range, the dynamic impedance between pins LN and GND (illustrated in Fig.8) is mainly determined by the $Z_{SET}$ impedance. The impedance introduced by the external $TN_{SW}$ transistor connected between pins GND and LN– is negligible.

### TRANSMIT AMPLIFIER (PINS TXI+ AND TXI–)

The UBA1706 has symmetrical transmit inputs TXI+ and TXI–. The input impedance between pins TXI+ or TXI– and GND is 21 kΩ. The voltage gain from pins TXI+ or TXI– to pin LN is set at 11.6 dB with 600 Ω line load ($Z_{line}$) and 619 Ω set impedance. The inputs are biased at $2 \times V_d \cong 1.4$ V, with $V_d$ representing the diode voltage. AGC is provided on this amplifier for line loss compensation.

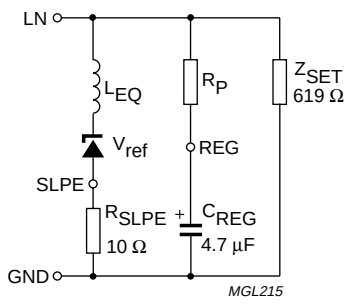
### RECEIVE AMPLIFIER (PINS RXI AND RXO; BIT RXM)

The receive amplifier (see Fig.9) has one input (RXI) and one output (RXO). The input impedance between pins RXI and GND is 21 kΩ.

The rail-to-rail output stage is designed to drive a 500 μA peak current. The output impedance at pin RXO is approximately 100 Ω.

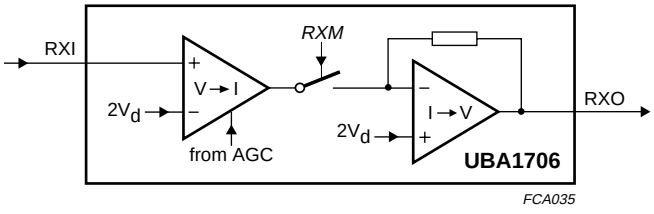
The voltage gain from pin RXI to pin RXO is set at 37.9 dB. This gain value compensates typically the attenuation of the anti-sidetone network (see Fig.10). The output and the input are biased at $2 \times V_d \cong 1.4$ V.

AGC is provided on this amplifier for line loss compensation. This amplifier can be muted by activating the receive mute function (bit RXM at logic 1).




$L_{eq} = C_{REG} \times R_{SLPE} \times R_P$
$R_P$ = internal resistance = 35 kΩ.

Fig.8 Equivalent impedance between pins LN and GND.




Bit names are given in italics.

Fig.9 Receive amplifier.

SIDETONE SUPPRESSION

The UBA1706 anti-sidetone network comprising $Z_{SET}//Z_{line}$, $R_{ast1}$, $R_{ast2}$, $R_{ast3}$, $R_{SLPE}$ and $Z_{bal}$ (see Fig.10) suppresses the transmitted signal in the received signal. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = Z_{SET} \times (R_{ast2} + R_{ast3})$$

$$k = \frac{(R_{ast2} \times (R_{ast3} + R_{SLPE}))}{(R_{ast1} \times R_{SLPE})}$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor ‘k’ is chosen to meet the compatibility with a standard capacitor from the E6 or E12 range for $Z_{bal}$.

In practice, $Z_{line}$ varies considerably with the line type and the line length.

Therefore, the value chosen for $Z_{bal}$ should be for an average line length, which gives satisfactory sidetone suppression with short and long lines.

The suppression also depends on the accuracy of the match between $Z_{bal}$ and the impedance of the average line.

The anti-sidetone network for the UBA1706 (see Fig.15) attenuates the receiving signal from the line by 38 dB before it enters the receiving amplifier. The attenuation is almost constant over the whole audio frequency range. A Wheatstone bridge configuration (see Fig.11) may also be used.

More information on the balancing of an anti-sidetone bridge can be obtained in our publication *“Applications Handbook for Wired Telecom Systems, IC03b”*.

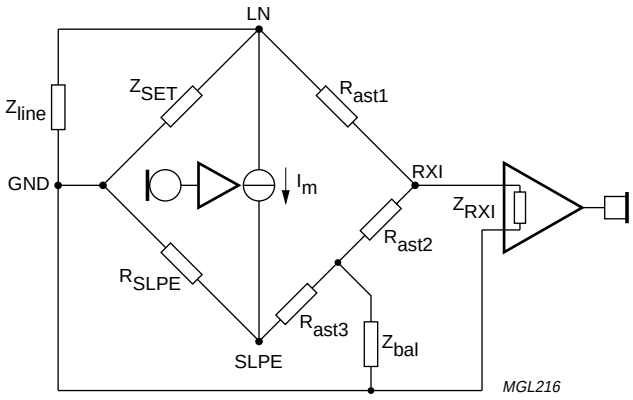



Fig.10 Equivalent circuit of UBA1706 anti-sidetone bridge.

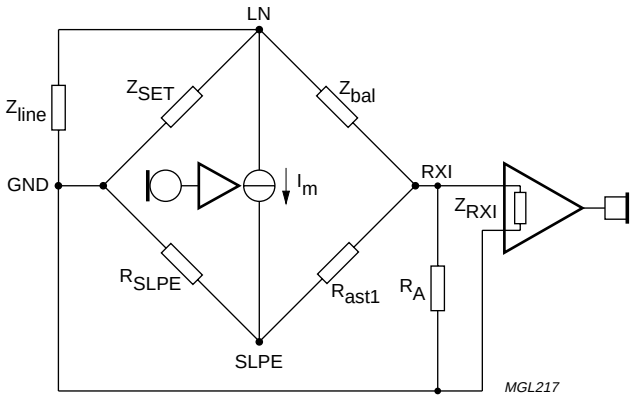



Fig.11 Equivalent circuit of an anti-sidetone network in a Wheatstone bridge configuration.

AUTOMATIC GAIN CONTROL (PIN AGC; BITS RAGC1, RAGC2, SAGC AND AGC)

The UBA1706 performs automatic line loss compensation. The AGC varies the gain of the transmit amplifier and the gain of the receive amplifier in accordance with the DC line current. The control range is 6.5 dB (which corresponds roughly to a line length of 5.5 km for a 0.5 mm diameter twisted-pair copper cable with a DC resistance of 176 Ω/km and an average attenuation of 1.2 dB/km).

When the line current is greater than $I_{stop}$, the voltage gains are minimum. When the line current is less than $I_{start}$, the voltage gains are maximum.

When the AGC pin is connected to pin GND, the start line current ($I_{start}$) can be chosen between 22.5 and 29.5 mA via bits RAGC1 and RAGC2 through the serial interface. Two values for the $I_{stop}/I_{start}$ ratio (slope of the AGC) are possible via bit SAGC through the serial interface. When bit SAGC is at logic 0 then $I_{stop} = 2.7 \times I_{start}$ (optimized for voltage regulation mode). When SAGC is at logic 1 then $I_{stop} = 1.9 \times I_{start}$ (optimized for current regulation mode).

An external resistor $R_{AGC}$ (connected between pins GND and AGC) enables the $I_{start}$ and $I_{stop}$ line currents to be increased (the ratio between $I_{start}$ and $I_{stop}$ is not affected by this external resistor). Therefore, internal and external adjustments of the AGC allow optimization of the IC for many configurations of exchange supply voltage and feeding bridge resistance.

Part of the line current flows into the $Z_{SET}$ impedance network. The IC has been optimized for $Z_{SET}$ = 619 Ω. Changing this 619 Ω value slightly modifies $I_{stop}$ and $I_{start}$ line currents as well as the value of the two AGC slopes.

The AGC function can be disabled by setting the AGC bit to logic 0 via the serial interface or by leaving pin AGC open-circuit. In this case, both of the voltage gains are maximum.

**General purpose switches (pins SWI1 and SWI2; bits SWC1 and SWC2)**

The UBA1706 is equipped with two general purpose open-collector switches, which short circuit pins SWI1 and SWI2 to ground. These switches are controlled by bits SWC1 and SWC2, respectively, and have an operating voltage limited to 12 V. The outputs have to be current biased. For a bias current between 2 and 20 mA, the AC impedance is 30 Ω maximum.

**Serial interface (pins DATA, CLK and EN)**

A simple 3-wire unidirectional serial bus is used to program the circuit. The three wires of the bus are EN, CLK and DATA. The data sent to the device is loaded in bursts framed by EN. Programming clock edges (falling edges) and their appropriate data bits are ignored until EN goes HIGH. The programmed information is loaded into the addressed register when EN returns to LOW or left open-circuit.

During normal operation, EN should be kept LOW. Only the last seven bits serially clocked into the device are retained within the programming register.

Additional leading bits are ignored and no check is made on the number of clock pulses. New programming data can always be captured during global power-down (bit PD at logic 1).

Data is entered with the most significant bit first. The leading six bits make up the data field (bits D0 to D5) while the trailing two bits are the address field (bits ADO and AD1). The first bit entered is D5, the last bit AD0. This organisation allows the transmission of only the number of bits of the addressed register.

Figure 13 shows the serial timing diagram. Table 1 gives the list of registers.

When the supply voltage $V_{CC}$ drops below 2.5 V, all register files are set to the initial state (see Table 1) defined by the power-up reset. At start-up, the circuit is in power-down mode.

When the IC is used in a noisy environment, it is advised to periodically refresh the content of registers**.**

**Table 1** Register description; note 1

| BIT NAME | FUNCTION | POLARITY | DATA | ADDRESS | STATE AT POWER-UP RESET |
|---|---|---|---|---|---|
| **Register 0: general purpose switches state and DC mask regulation mode** | | | | | |
| SWC1 | SWI1 output connection | 0: SWI1 switched-off | D0 | (AD1, AD0) = (0,0) | 0 |
| | | 1: SWI1 switched-on | | | |
| SWC2 | SWI2 output connection | 0: SWI2 switched-off | D1 | | 0 |
| | | 1: SWI2 switched-on | | | |
| un | unused | must be set to logic 0 | D2 | | 0 |
| un | unused | must be set to logic 0 | D3 | | 0 |
| CRC | current regulation mode | 0: voltage regulation | D4 | | 0 |
| | | 1: current regulation | | | |
| **Register 1: automatic gain control** | | | | | |
| RAGC1 | AGC range selection 1 | | D0 | (AD1, AD0) = (0,1) | 0 |
| RAGC2 | AGC range selection 2 | | D1 | | 0 |
| SAGC | AGC slope selection | 0: 2.7 type slope; note 2 | D2 | | 0 |
| | | 1: 1.9 type slope; note 2 | | | |
| AGC | line loss compensation mode | 0: AGC inhibited | D3 | | 0 |
| | | 1: AGC enabled | | | |
| **Register 2** | | | | | |
| unused, in case of programming register 2 data must be set to: 000100 (D5; D0) | | | | (AD1, AD0) = (1,0) | – |
| **Register 3: mute functions and power-down** | | | | | |
| un | unused | must be set to logic 1 | D0 | (AD1, AD0) = (1,1) | 0 |
| RXM | receive amplifier mute | 0: amplifier enabled | D1 | | 0 |
| | | 1: amplifier muted | | | |
| PD | reduced consumption mode | 0: normal operating mode | D2 | | 1 |
| | | 1: power-down mode | | | |
| un | unused | must be set to logic 1 | D3 | | 0 |

**Notes**

1. For full software compatibility, the registers have the same addresses as for the UBA1707.
2. See Section “Automatic gain control (pin AGC; bits RAGC1, RAGC2, SAGC and AGC)”.

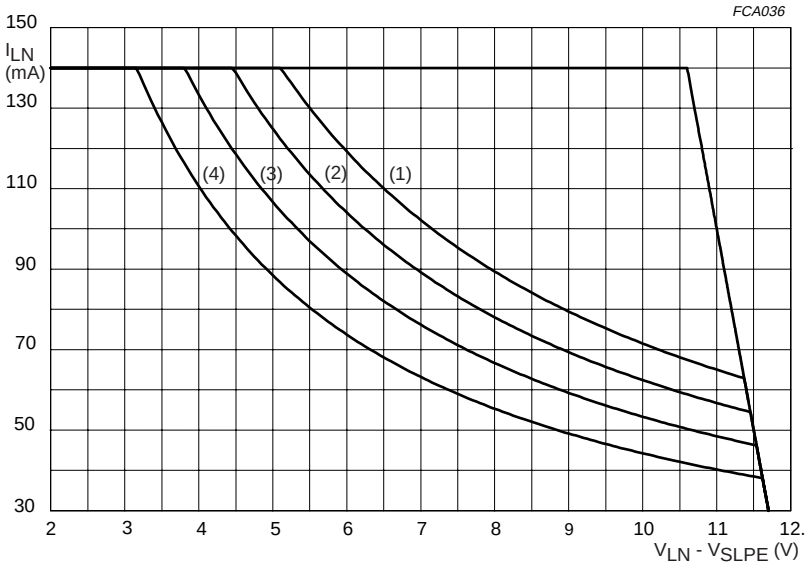
**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | GND – 0.4 | 5.5 | V |
| $V_{LN}$ | positive continuous line voltage on pin LN | | GND – 0.4 | 12.0 | V |
| | repetitive line voltage during switch-on or line interruption | | GND – 0.4 | 13.2 | V |
| $V_{SWIn}$ | voltage on pins SWI1 and SWI2 | continuous | GND – 0.4 | 12.0 | V |
| | | during switching | GND – 0.4 | 13.2 | V |
| $V_{n(max)}$ | maximum voltage on all other pins | | GND – 0.4 | $V_{CC}$ + 0.4 | V |
| $I_{LN}$ | current sunk by pin LN | see Fig.12 | – | 150 | mA |
| $I_{SWIn}$ | continuous current sunk by pins SWI1 and SWI2 | bit SWCn = 1 | – | 20 | mA |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = 75 °C; see Fig.12 | – | 454 | mW |
| $T_{stg}$ | IC storage temperature | | –40 | +125 | °C |
| $T_{amb}$ | ambient temperature | | –25 | +75 | °C |
| $T_j$ | junction temperature | | – | +125 | °C |

**THERMAL CHARACTERISTICS**

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 100 | K/W |




(1) $T_{amb}$ = 45 °C; $P_{tot}$ = 727 mW
(2) $T_{amb}$ = 55 °C; $P_{tot}$ = 636 mW
(3) $T_{amb}$ = 65 °C; $P_{tot}$ = 545 mW
(4) $T_{amb}$ = 75 °C; $P_{tot}$ = 454 mW

The line current value can be calculated from the $I_{LN}$ value as follows:

$$I_{line} = \frac{I_{LN} \times (R_{SET} + R_{SLPE}) + V_{LN} - V_{SLPE}}{R_{SET}}$$ where $R_{SET}$ is the resistive part of $Z_{SET}$.

Fig.12 Safe operating area.

## CHARACTERISTICS

$I_{line}$ = 15 mA; $V_{CC}$ = 3.3 V; $R_{SLPE}$ = 10 Ω; AGC pin connected to GND; $Z_{line}$ = 600 Ω; $Z_{SET}$ = 619 Ω; EHI = HIGH; f = 1 kHz; $T_{amb}$ = 25 °C; bit AGC at logic 1, all other configuration bits at logic 0; measured in test circuit of Fig.14; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supply (pins $V_{CC}$ and GND; bit PD)** | | | | | | |
| $V_{CC}$ | supply voltage | | 3.0 | – | 5.5 | V |
| $I_{CC}$ | current consumption from pin $V_{CC}$ | | – | 2.2 | 3.2 | mA |
| $I_{CC(pd)}$ | current consumption from pin $V_{CC}$ in power-down mode | bit PD = 1 | – | 110 | 150 | μA |
| **Line interface (pins LN, SLPE and REG)** | | | | | | |
| DC CHARACTERISTICS | | | | | | |
| $V_{ref}$ | stabilized voltage between pins LN and SLPE | $I_{line}$ = 11 to 140 mA | 2.6 | 2.9 | 3.2 | V |
| $V_{LN}$ | DC line voltage between pins LN and GND | $I_{line}$ = 2 mA | – | 1.2 | – | V |
| | | $I_{line}$ = 4 mA | – | 1.8 | – | V |
| | | $I_{line}$ = 15 mA | 2.7 | 3.0 | 3.3 | V |
| | | $I_{line}$ = 140 mA | – | 4.35 | – | V |
| $V_{LN(Rext)}$ | DC line voltage between pins LN and GND with an external resistor $R_{VA}$ | $R_{VA(SLPE–REG)}$ = 8 kΩ | – | 4.5 | – | V |
| $\Delta V_{LN(T)}$ | DC line voltage variation with temperature referenced to 25 °C | $T_{amb}$ = −25 to +75 °C | – | 8.0 | – | mV |
| **Masks regulation (pins LCC, LVI, CST and RGL; bit CRC)** | | | | | | |
| DC CHARACTERISTICS | | | | | | |
| $I_{LCC(max)}$ | maximum current sunk by pin LCC | | 500 | – | – | μA |
| $R_{int(LCC)}$ | internal resistance between pins $V_{CC}$ and LCC | | – | 165 | – | kΩ |
| *Voltage regulation mode* | | | | | | |
| $I_{LVIV}$ | current sourced from pin LVI | bit CRC = 0 | – | 200 | – | nA |
| *Current regulation mode* | | | | | | |
| $I_{knee}$ | start line current for current regulation mode | bit CRC = 1 | – | 35 | – | mA |
| $R_{REGC}$ | DC mask slope in current regulation mode | $I_{line} > I_{knee}$; $R_{LVI}$ = 1 MΩ; $R_{RGL}$ = 7.15 kΩ; bit CRC = 1 | – | 1.4 | – | kΩ |
| *Current limitation* | | | | | | |
| $I_{prot}$ | current limitation level | | – | 145 | – | mA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Electronic hook-switch control (pin EHI)** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.3 | – | $V_{CC}$ + 0.4 | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 3.0 to 5.5 V | GND – 0.4 | – | $0.3V_{CC}$ | V |
| $I_{bias}$ | input bias current | input level = HIGH | 1 | 2 | 5 | µA |
| **Transmit amplifier (pins TXI+, TXI– and LN)** | | | | | | |
| $\|Z_i\|$ | input impedance | between pins TXI+ and GND or TXI– and GND | – | 21 | – | kΩ |
| | | between pins TXI+ and TXI– | – | 36 | – | kΩ |
| $G_{v(TX)}$ | voltage gain from TXI+/TXI– to LN | $V_{TXI}$ = 50 mV (RMS) | 10.6 | 11.6 | 12.6 | dB |
| $\Delta G_{v(TX)(f)}$ | voltage gain variation with frequency referenced to 1 kHz | f = 300 to 3400 Hz | – | ±0.3 | – | dB |
| $\Delta G_{v(TX)(T)}$ | voltage gain variation with temperature referenced to 25 °C | $T_{amb}$ = –25 to +75 °C | – | ±0.3 | – | dB |
| CMRR | common mode rejection ratio | | – | 65 | – | dB |
| PSRR | power supply rejection ratio | | – | 36 | – | dB |
| $V_{LN(max)(rms)}$ | maximum sending signal (RMS value) | $I_{line}$ = 15 mA; THD = 2% | 1.2 | 1.4 | – | V |
| | | $I_{line}$ = 4 mA; THD = 10% | – | 0.26 | – | V |
| $V_{iTX(max)(rms)}$ | maximum transmit input voltage (RMS value) for 2% THD on pin LN | $I_{line}$ = 15 mA | – | 0.35 | – | V |
| | | $I_{line}$ = 90 mA | – | 0.75 | – | V |
| $V_{no(LN)}$ | noise output voltage at pin LN | pins TXI+ and TXI– short-circuited through 200 Ω in series with 10 µF; psophometrically weighted (P53 curve) | – | –74 | – | dBmp |
| **Receive amplifier (pins RXI and RXO; bit RXM)** | | | | | | |
| $\|Z_i\|$ | input impedance between pins RXI and GND | | – | 21 | – | kΩ |
| $G_{v(RX)}$ | voltage gain from RXI to RXO | $V_{RXI}$ = 2 mV (RMS) | 36.9 | 37.9 | 38.9 | dB |
| $\Delta G_{v(RX)(f)}$ | voltage gain variation with frequency referenced to 1 kHz | f = 300 to 3400 Hz | – | ±0.2 | – | dB |
| $\Delta G_{v(RX)(T)}$ | voltage gain variation with temperature referenced to 25 °C | $T_{amb}$ = –25 to +75 °C | – | ±0.3 | – | dB |
| PSRR | power supply rejection ratio | | – | 68 | – | dB |
| THD | total harmonic distortion | $V_{RXI}$ = 2 mV (RMS) | – | 0.03 | – | % |
| | | $V_{RXI}$ = 12.5 mV (RMS) | – | 2 | – | % |
| | | $V_{RXI}$ = 19.5 mV (RMS); $I_{line}$ = 90 mA | – | 2 | – | % |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{no(RXO)(rms)}$ | noise output voltage at pin RXO (RMS value) | RXI open-circuit; psophometrically weighted (P53 curve) | – | –81 | – | dBVp |
| $\Delta G_{v(RX)(m)}$ | voltage gain reduction from pin RXI to RXO when muted | $V_{RXI}$ = 10 mV (RMS); bit RXM = 1 | – | 80 | – | dB |
| **Automatic gain control (pin AGC; bits RAGC1, RAGC2, SAGC and AGC)** | | | | | | |
| $\Delta G_{v(trx)}$ | gain control range for transmit and receive amplifiers with respect to $I_{line}$ = 15 mA | $I_{line}$ = 90 mA | – | 6.5 | – | dB |
| $I_{start}$ | highest line current for maximum gain | bits RAGC1 = 1; RAGC2 = 1 | – | 22.5 | – | mA |
| | | bits RAGC1 = 1; RAGC2 = 0 | – | 25 | – | mA |
| | | bits RAGC1 = 0; RAGC2 = 1 | – | 27 | – | mA |
| | | bits RAGC1 = 0; RAGC2 = 0 | – | 29.5 | – | mA |
| $I_{stop}$ | lowest line current for minimum gain when $I_{start}$ = 23 mA | bits SAGC = 0; RAGC1 = 1; RAGC2 = 1 | – | 62 | – | mA |
| | | bits SAGC = 1; RAGC1 = 1; RAGC2 = 1 | – | 43 | – | mA |
| $\Delta G_{v(trxoff)}$ | gain variation for transmit and receive amplifiers when AGC is off | bit AGC = 0; $I_{line}$ = 15 to 140 mA | – | – | ±0.2 | dB |
| **Switches (pins SWI1 and SWI2; bits SWC1 and SWC2)** | | | | | | |
| $\lvert Z_{i(off)} \rvert$ | AC impedance between pins SWIn and GND when not selected | bit SWCn = 0 | 700 | – | – | kΩ |
| $\lvert Z_{i(on)} \rvert$ | AC impedance between pins SWIn and GND when selected | 2 mA < $I_{SWIn}$ < 20 mA; bit SWCn = 1 | – | – | 30 | Ω |
| **Serial interface (pins DATA, CLK and EN)** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.3 | – | $V_{CC}$ + 0.4 | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 3 to 5.5 V | GND – 0.4 | – | $0.3V_{CC}$ | V |
| $I_{bias}$ | input bias current | input level = HIGH | 1 | 2 | 5 | µA |
| $C_i$ | input capacitance at pins DATA, CLK and EN | | – | 4 | – | pF |

**SERIAL BUS TIMING CHARACTERISTICS**

$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| **Serial programming clock; pin CLK** | | | | |
| $f_{clk}$ | clock frequency | 0 | 300 | kHz |
| **Enable programming; pin EN** | | | | |
| $t_{START}$ | delay to falling clock edge | 1 | – | µs |
| $t_{END}$ | delay from last rising clock edge | 0.1 | – | µs |
| $t_{W(min)}$ | minimum inactive pulse width | 1.5 | – | µs |
| $t_{SU;\ EN}$ | enable set-up time to next clock edge | 0.1 | – | µs |
| **Serial data; pin DATA** | | | | |
| $t_{SU;\ DATA}$ | input data to clock set-up time | 2 | – | µs |
| $t_{HD;\ DATA}$ | input data to clock hold time | 2 | – | µs |

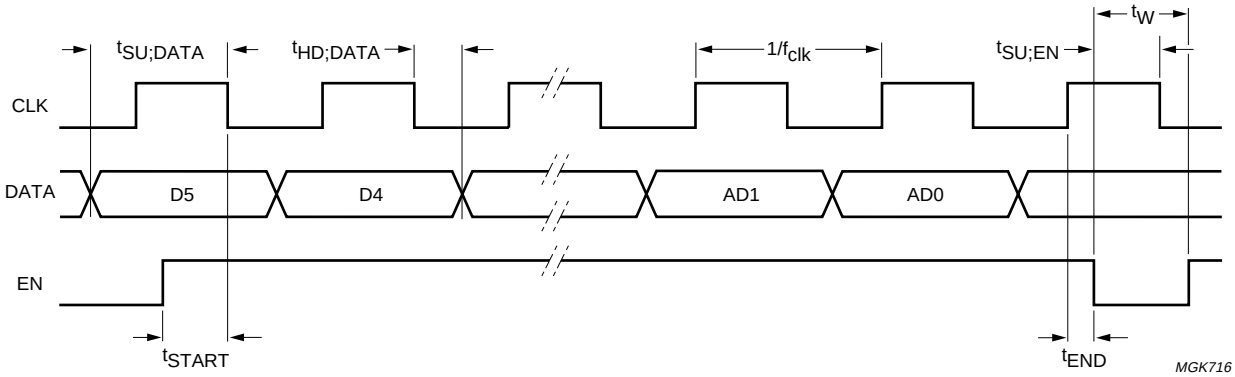



Fig.13 Serial bus timing diagram.

## TEST AND APPLICATION INFORMATION

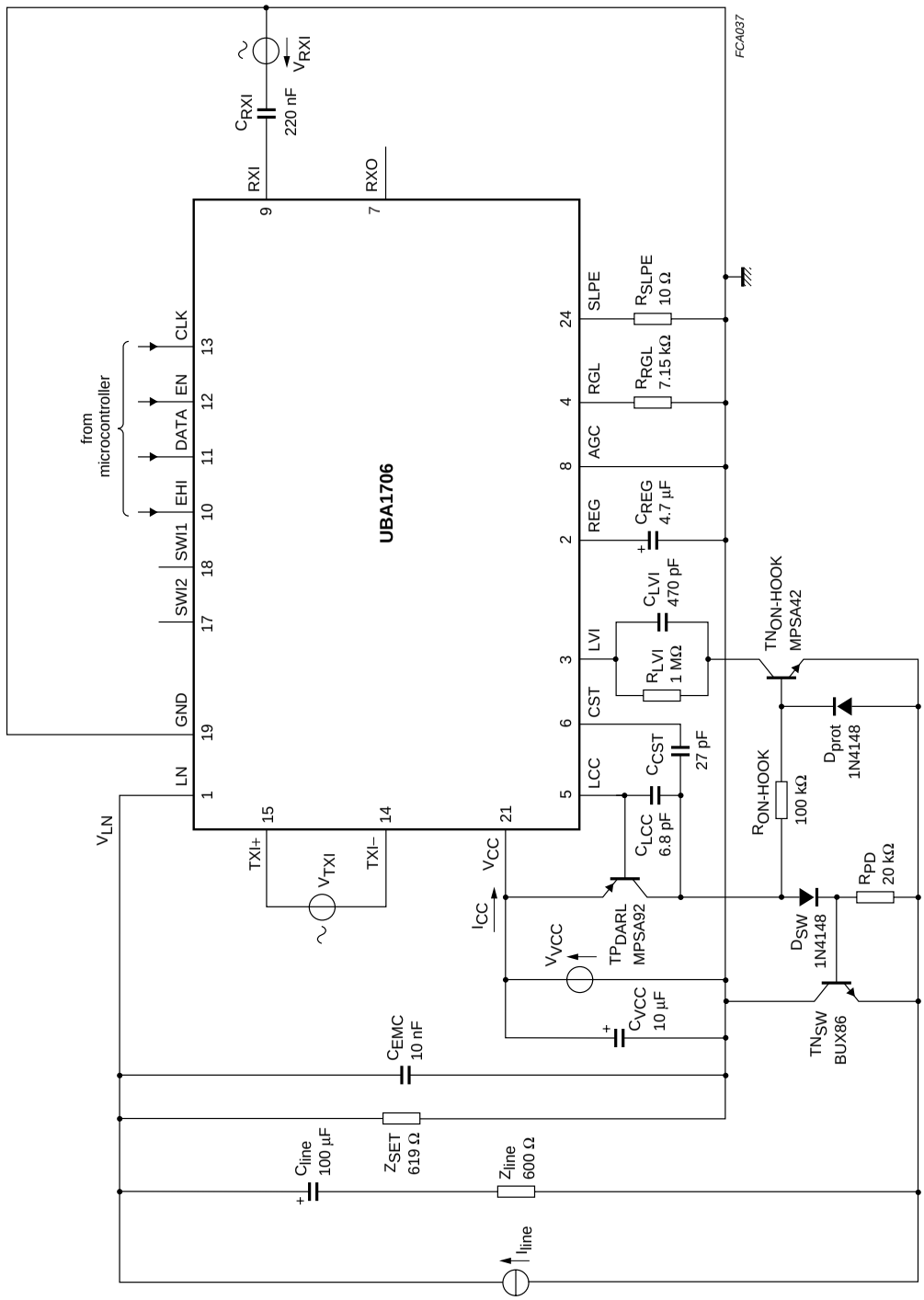



Fig.14 Test circuit.

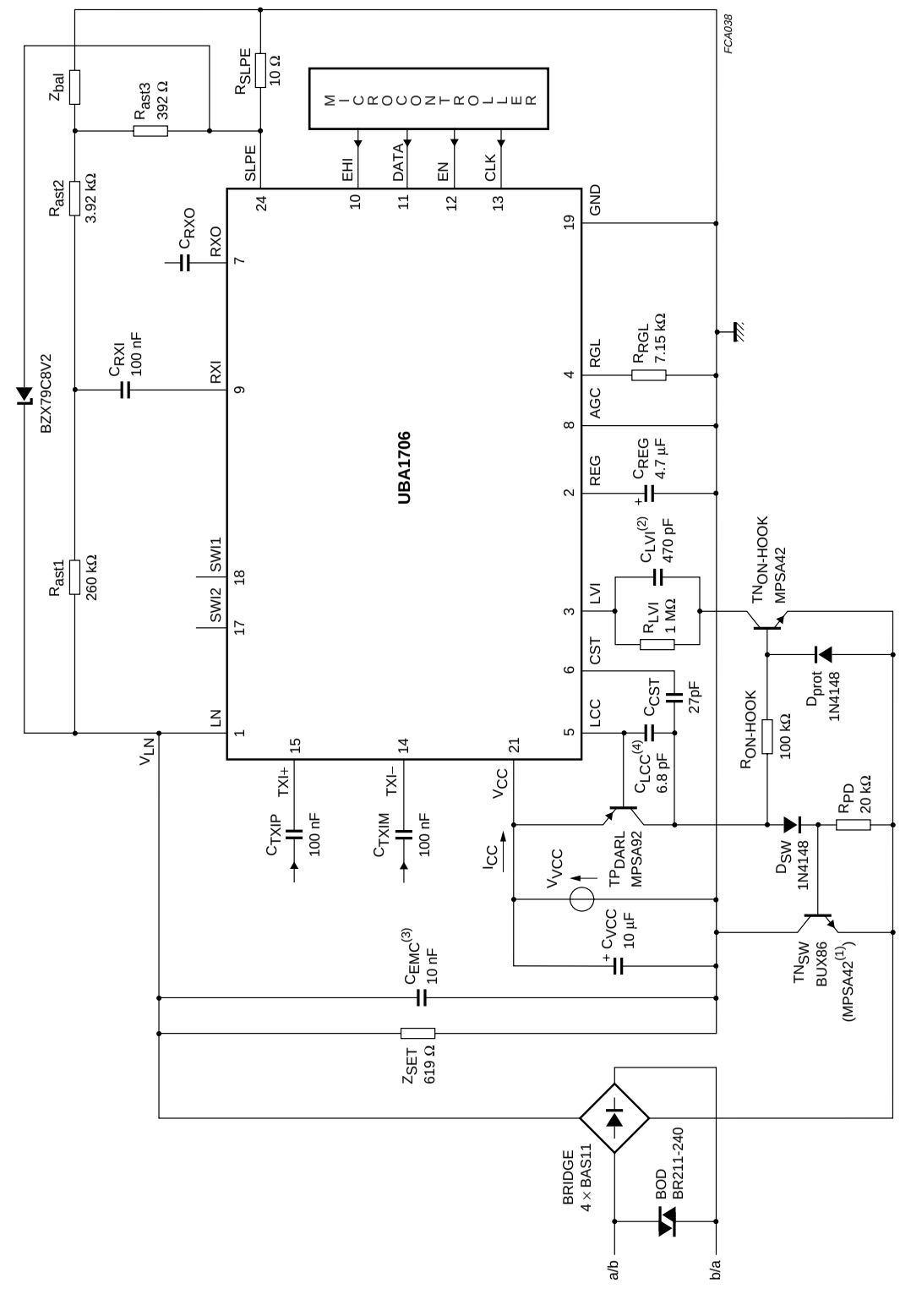
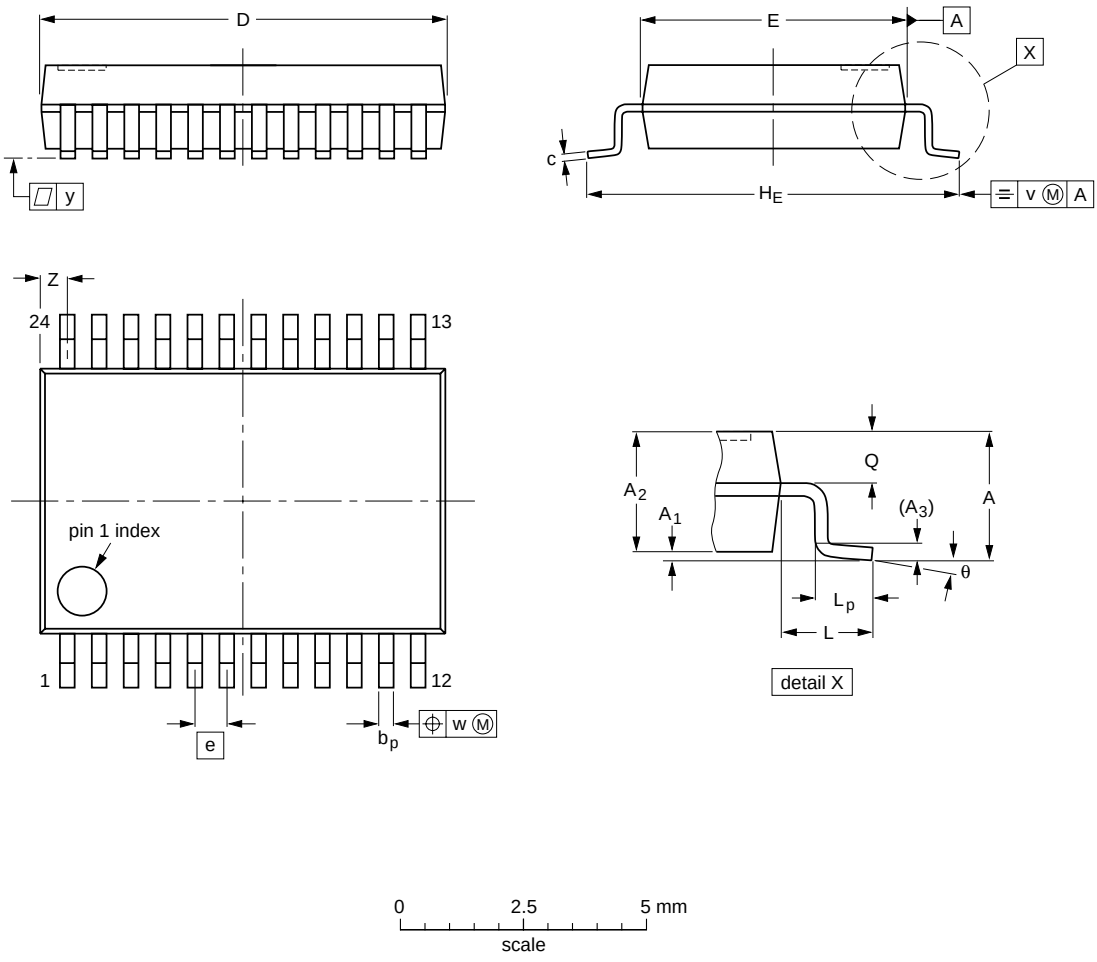



Fig.15 Typical application.

(1) In case of low line current in voltage regulation mode.
(2) Only required in current regulation mode.
(3) To improve EMC performance; necessary for stability.
(4) To improve stability only in current regulation mode.

## PACKAGES OUTLINE

**SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm** **SOT340-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.0 | 0.21<br>0.05 | 1.80<br>1.65 | 0.25 | 0.38<br>0.25 | 0.20<br>0.09 | 8.4<br>8.0 | 5.4<br>5.2 | 0.65 | 7.9<br>7.6 | 1.25 | 1.03<br>0.63 | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 0.8<br>0.4 | $8^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT340-1 | | MO-150AG | | | | ~~93-09-08~~<br>95-02-04 |

## SOLDERING

### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

**Suitability of surface mount IC packages for wave and reflow soldering methods**

| PACKAGE | SOLDERING METHOD | |
|---|---|---|
| | WAVE | REFLOW(1) |
| BGA, SQFP | not suitable | suitable |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable(2) | suitable |
| PLCC(3), SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended(3)(4) | suitable |
| SSOP, TSSOP, VSO | not recommended(5) | suitable |

**Notes**

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

**DEFINITIONS**

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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