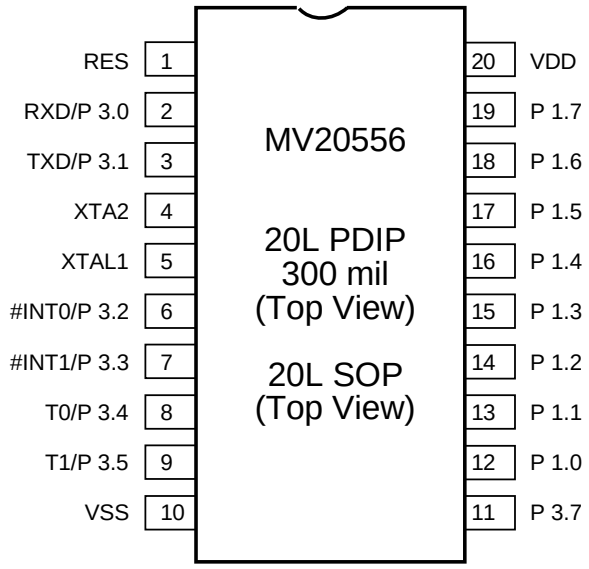
Features

- General 8051 instruction family compatible
- Operate at voltage 5.0V.
- No External Memory is supported
- 8 bit bus I/O ports
- 4 K byte ROM
- 128 byte RAM
- 128 byte depth stack
- Two 16 bit Timers (Event Counters)
- 15 programmable I/O pins
- Five interrupt sources
- Programmable serial UART channel
- Direct LED drive output
- Bit operation instructions
- Page free jumps
- 8 - bit Unsigned Division
- 8 - bit Unsigned Multiply
- BCD arithmatic
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- A full duplex serial I/O port
- Working at 16/25/40 MHz Clock
- Full static operation: 3 MHz through 16 MHz

Description

The MVI MV20556 is an 8 - bit single chip microcontroller. It provides hardware features and powerful instruction set that are necessary to make it a versatile and cost effective controller for mouse applications which needs up to 4K byte internal memory either for program or for data and mixed.
A serial input / output port is provided for I/O expansion, Inter - processor communications, full duplex UART.

Pin Configuration



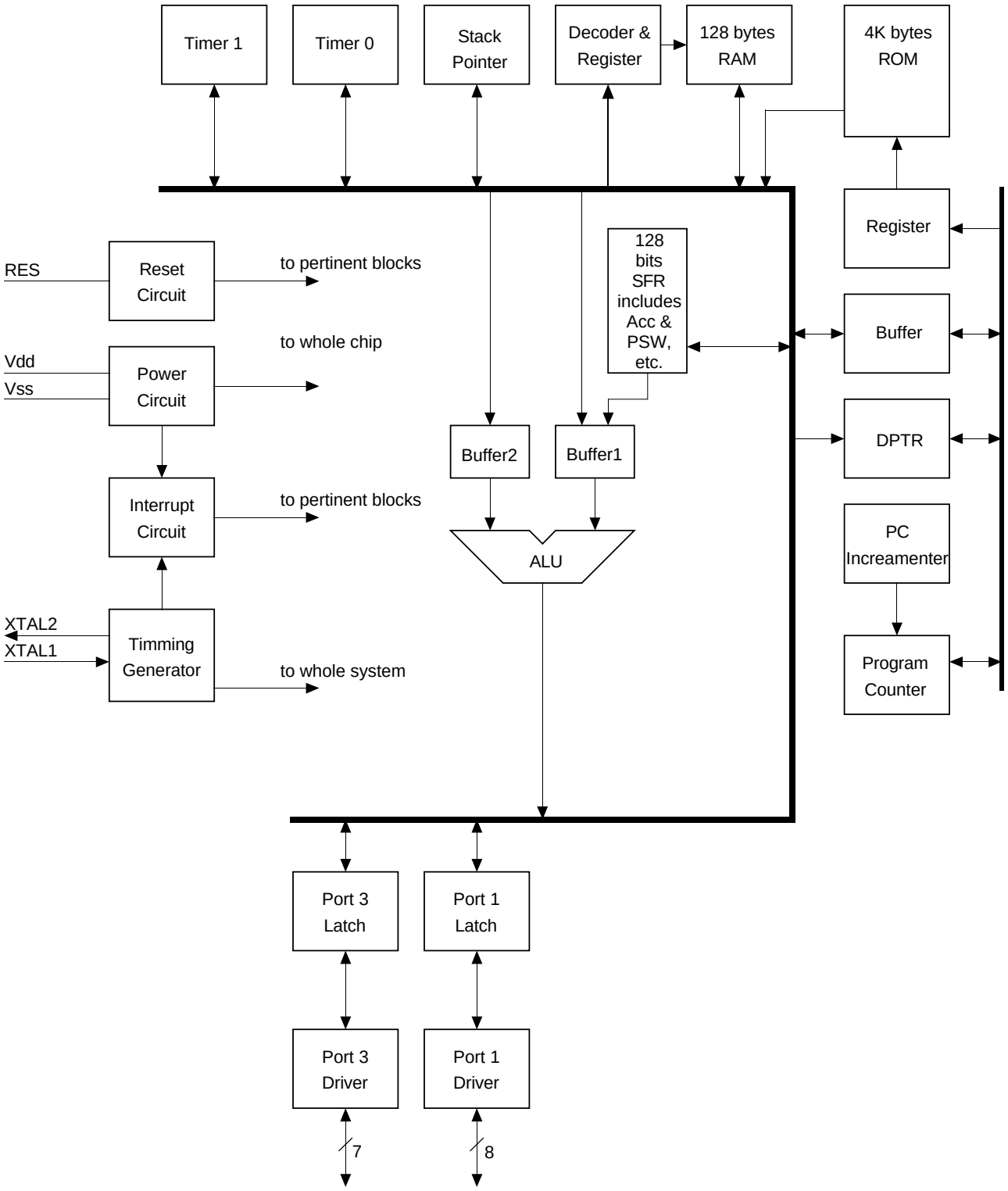
Ordering Information

MV20556ajk - pqrs

a: process identifier. { C:=COMS }
jk: working clock in MHz. { 16 }
pqr: production code { 001, ..., 999 }
s: package type. { P: 20L 300 mil PDIP }

Postfix	Package	Pin/Pad Configuration	Dimension	Logo Size at Top Marking
blank	dice	page 25	page 25	-
N	20L PDIP	page 1	page 23	4.5 x 3.8 mm
S	20L SOP	page 1	page 24	4.0 x 3.4 mm

Block Diagram



Pin Descriptions

20L PDIP Pin#		20L SOP Pin#	dice Pad#	Symbol	Active	I/O	Names
1		1	4	RES		i	Reset
2		2	5	RXD/P3.0		i/o	bit 0 of Port 3 & Receive data
3		3	6	TXD/P3.1		i/o	bit 1 of Port 3 & Transmit data
4		4	7	XTAL2		i	Crystal out
5		5	8	XTAL1		o	Crystal in
6		6	9	#INT0/P3.2	L/-	i/o	bit 2 of Port 3 & low true Interrupt 0
7		7	10	#INT1/P3.3	L/-	i/o	bit 3 of Port 3 & low true Interrupt 1
8		8	11	T0/P3.4		i/o	bit 4 of Port 3 & external input to Timer 0
9		9	12	T1/P3.5		i/o	bit 5 of Port 3 & external input to Timer 1
10		10	13-15	VSS		i/o	Sink Voltage, Ground
11		11	17	P3.7		i/o	bit 7 of Port 3
12		12	18	P1.0		i/o	bit 0 of Port 1
13		13	19	P1.1		i/o	bit 1 of Port 1
14		14	20	P1.2		i/o	bit 2 of Port 1
15		15	21	P1.3		i/o	bit 3 of Port 1
16		16	22	P1.4		i/o	bit 4 of Port 1
17		17	23	P1.5		i/o	bit 5 of Port 1
18		18	24	P1.6		i/o	bit 6 of Port 1
19		19	1	P1.7		i/o	bit 7 of Port 1
20		20	2, 3	VDD		i/o	Drive Voltage, +5 Vcc

Signal Descriptions

VSS
Circuit ground potential.

VDD
+5V power supply during operation.

PORT 1
Port 1 is an 8-bit quasi-bidirectional I/O port.
There is a pull-up resistance when operating at either input or output.

PORT 3
Port 3 is an 7-bit quasi-bidirectinal I/O port. It also contains the interrupt and timer as well as serial port pins that are used by various options. The output latch corresponding to a secondary function must be programmed to one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:
- RXD/data (P3.0). Serial port's transmitter data input (asynchronous) or data input/output (asynchronous).
- TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or data input/output (asynchronous).
- #INT0 (P3.2). Interrupt 0 input or gate control input for counter 0.
- #INT1 (P3.3). Interrupt 1 input or gate control input for counter 1.
- T0 (P3.4). Input to counter 0.
- T1 (P3.5). Input to counter 1.

There is a pull-up resistance when operating at either input or output.

RES
A low to high transition on this pin (V IH1) while the oscillator is not running resets the MV20556. Holding high signal (higher than V IH1) on this pin for two machine cycles (24 clocks) or longer while the oscillator is running, resets the device.

XTAL 1
Input to the oscillator's high gain amplifier. A crystal or external source can be used.

XTAL 2
Output from the oscillator's amplifier. Required when a crystal is used.

Function Overall

The CPU of MV20556 manipulates versatile operands in four memory spaces. They are 4 KB program ROM, 128-byte internal Data RAM, 20 SFRs and 16-bit program counter.

The Internal Data Memory address space is further divided into the 128-byte Internal Data RAM and 128-byte Special Function Register (SFR) address spaces shown in latter Figures. Four Register Banks (each with eight registers), 128 addressable bits, and the stack reside in the Internal Data RAM. The stack depth is limited only by the available Internal Data RAM and its location is determined by the 8-bit Stack Pointer. All registers except the Program Counter and the four 8-Register Banks reside in the Special Function Register address space.

These memory mapped registers include arithmetic registers, pointers, I/O ports, and registers for the interrupt system, timers and serial channel. 128 bit locations in the SFR address space are addressable as bits. The MV20556 contains 128 bytes of Internal Data RAM and 20 SFRs.

The MV20556 provides a non-paged Program Memory address space to accommodate relocatable code. Conditional branches are performed relative to the Program Counter. The register-indirect jump permits branching relative to a 16-bit base register with an offset provided by an 8-bit index register. Sixteen-bit jumps and calls permit branching to any location in the contiguous 4K Program Memory address space.

The MV20556 has five methods for addressing source operands: Register, Direct, Register-Indirect, Immediate, and Base-Register-plus Index-Registe -Indirect Addressing. The first three methods can be used for addressing destination operands. Most instructions have a "destination, source" field that specifies the data type, addressing methods and operands involved. For operations other than moves, the destination operand is also a source operand.

Any register in the four 8-Register Banks can be accessed through Register, Direct, or Register-Indirect Addressing; the 128 bytes of Internal Data RAM through Direct or Register-Indirect Addressing; and the Special Function Registers through Direct Addressing. External Data Memory is accessed through Register-Indirect Addressing. Look-Up-Tables resident in Program Memory can be accessed through Base-Register-plus Index-Register-Indirect Addressing.

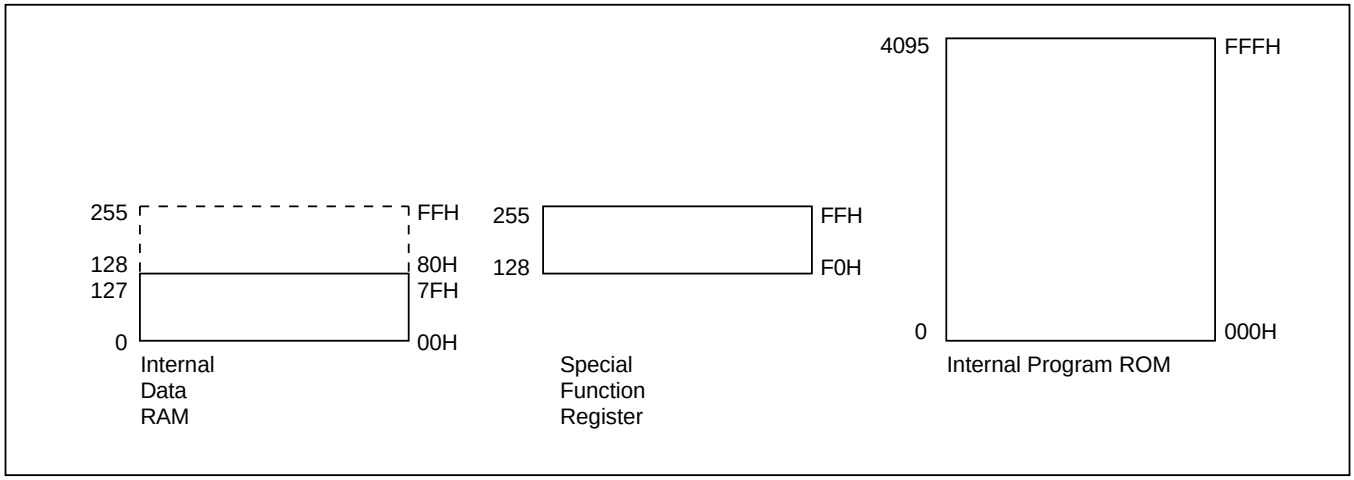
The MV20556 is classified as an 8-bit machine since the internal ROM, RAM, Special Function Registers, Arithmetic/Logic Unit and external data bus are each 8 bits wide. The MV20556 performs operation on bit, nibble, byte and double-byte data types.

The MV20556 has extensive facilities for byte transfer, logic, and integer arithmetic operations. It excells at bit handling since data transfer, logic and conditional branch operantions can be performed directly on Boolean variables.

Memory Map Overall

The CPU of MV20556 is able to access three memory areas. They are:

(1) 128 bytes data RAM addressed at 00H through 7FH;
(2) 20 SFRs addressed at 80H through FFH;
(3) 4,096 bytes program ROM addressed at 000H through FFFH.
Be noted, MCU MV20556 builds all accessible memory inside, it is unable to access external memory.



Internal Memory Map

Memory Map Details

Internal RAM

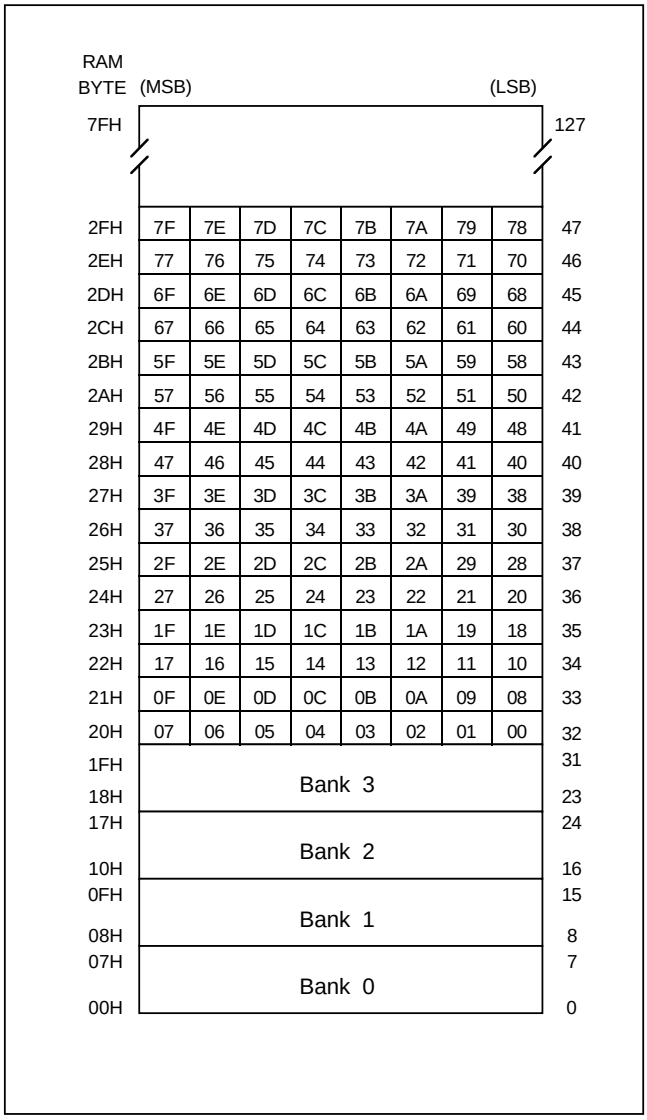
The MV20556 contains a 128-byte Internal Data RAM (Which includes registers R7-R0 in each of four Banks), and twenty memory-mapped Special Function Registers.

Internal Data RAM

The Internal Data RAM provides a convenient 128-byte scratch pad memory.

Register Banks

There are four Register Banks within the Internal Data RAM. Each Register Bank contains registers R7-R0.



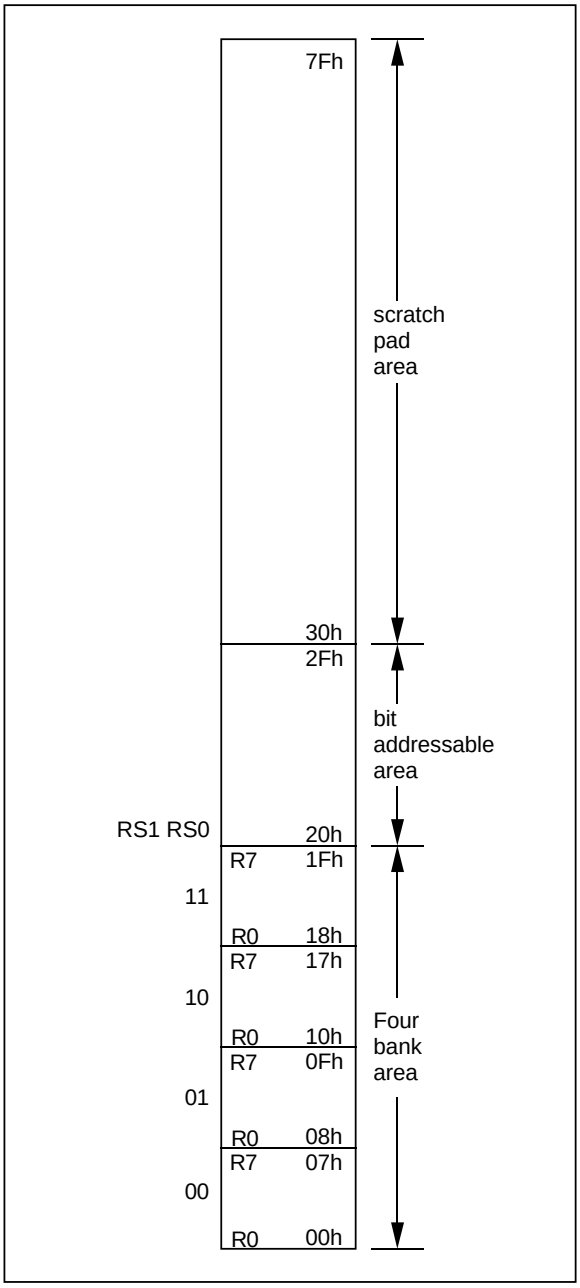
128B RAM Bit Address

128 Addressable Bits

There are 128 addressable software flags in the Internal Data RAM. They are located in the 16 byte locations starting at byte address 32 and ending with byte location 47 of the RAM address space.

Stack

The stack may be located anywhere within the Internal Data RAM address space. The stack may be as large as 128 bytes on the MV20556.



128B RAM Memory Map

Memory Map Details (Cont'd)

Special Function Registers (SFR)

The Special Function Registers include arithmetic registers (Acc, B, PSW), pointers (SP, DPH, DPL) and registers that provide an interface between the CPU and the on-chip peripheral functions. These are also 128 addressable bits within the Special Function Registers. The memory-mapped locations of these registers and bits are shown in right side figure.

Acc Register

The Acc register is the accumulator.

B Register

The B register is dedicated during multiply and divide and serves as both a source and a destination. During all other operations the B register is simply another location of the Special Function Register space.

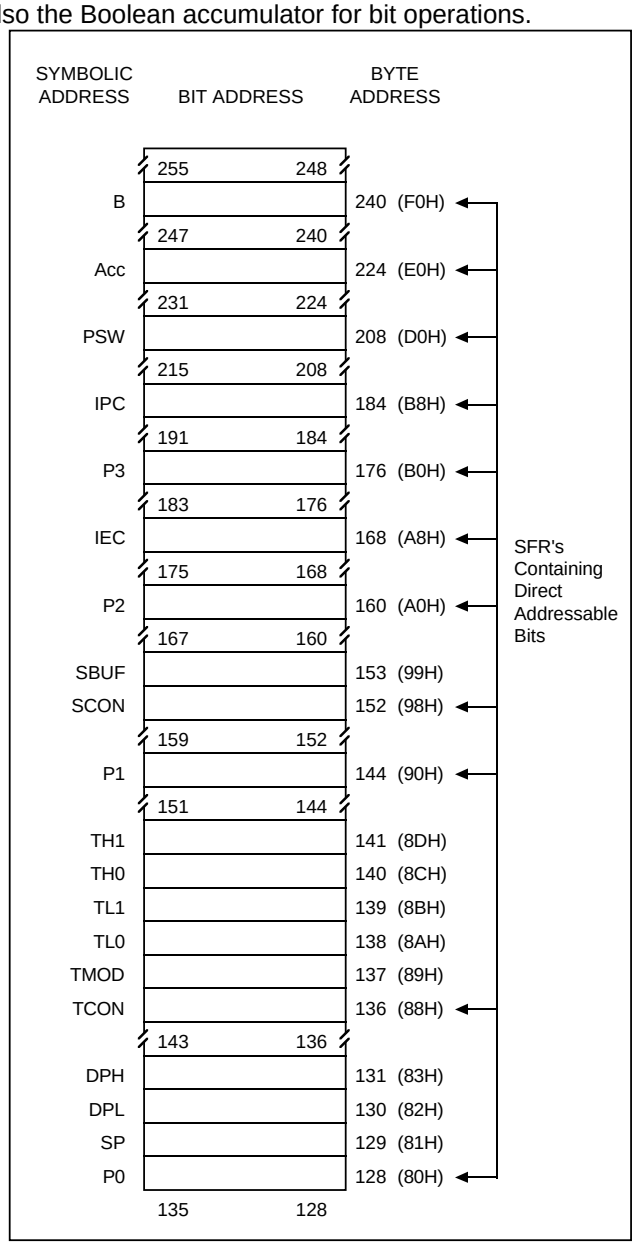
Direct Byte Address	Bit Addresses (MSB)							(LSB)	Hardware Register Symbol
240	F7	F6	F5	F4	F3	F2	F1	F0	B
224	E7	E6	E5	E4	E3	E2	E1	E0	Acc
	CY	AC	FO	RS1	RS0	OV		P	
208	D7	D6	D5	D4	D3	D2	D1	D0	PSW
				PS	PT1	PX1	PT0	PX0	
184	-	-	-	BC	BB	BA	B9	B8	IP
176	B7	B6	B5	B4	B3	B2	B1	B0	P3
	EA			ES	ET1	EX1	ET0	EX0	
168	AF	-	-	AC	AB	AA	A9	A8	IE
160	A7	A6	A5	A4	A3	A2	A1	A0	P2
	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	
152	9F	9E	9D	9C	9B	9A	99	98	SCON
144	97	96	95	94	93	92	91	90	P1
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
136	8F	8E	8D	8C	8B	8A	89	88	TCON
128	87	86	85	84	83	82	81	80	P0

SFR Bit Address

Program Status Word Register

The carry (CY), auxiliary carry (AC), user flag 0 (F0), register bank select (RS0 and RS1), overflow (OV) and parity (P) flags reside in the Program Status Word (PSW) Register. These flags are bit-memory-mapped within the byte-memory-mapped PSW. The PSW flags record processor status information and control the operation of the processor.

The CY, AC, and OV flags generally reflect the status of the latest arithmetic operations. The P flag always reflects the parity of the Acc register. The carry flag is also the Boolean accumulator for bit operations.



SFR Memory Map

Memory Map Details (Cont'd)

Program Status Word Register(Cont'd)
F0 is a general purpose flag which is pushed onto the stack as part of a PSW save. The two Register Bank select bits (RS1 or RS0) determine which one of the four Register Banks is selected.

Stack Pointer
The 8-bit Stack Pointer (SP) contains the address at which the last byte was pushed onto the stack. This is also the address of the next byte that will be popped. The SP is incremented during a push. SP can be read or written to under software control.

Data Pointer (High) and Data Pointer (Low)
The 16-bit Data Pointer (DPTR) register is the concatenation of registers DPH (data pointer's high-order byte) and DPL (data pointer's low-order byte). The DPTR is used in Register-Indirect Addressing to move Program Memory constants, to move External Data Memory variables, and to branch over the 64K Program Memory address space.

Interrupt Priority Register
The Interrupt Priority (IPC) register contains the control bits to set an interrupt to a desired level. A bit set to a one gives the particular interrupt a high priority listing.

Interrupt Enable Register
The Interrupt Enable (IEC) register stores the enable bits for each of the five interrupt sources. Also included is a global enable/disable bit of the interrupt system.

Timer/Counter Mode Register
Within the Times Mode (TMOD) register are the bits that select which operations each timer/counter will do.

Timer/Counter Control Register
The timer/counters are controlled by the Timer/Counter Control (TCON) register bits. The start/stop bits for the timer/counters along with the overflow and interrupt request flags are mapped in TCON.

Timer/Counter 1 (High), Timer/Counter 1 (Low), Timer/Counter 0 (High), Timer/Counter 0 (Low)
There are four register locations for the two 16-bit timer/counters. These registers can be read or written to, to give the programmer easy access to the timer/counters. TH1 and TH0 refer to the 8 high-order bits of timer/counter 1 and 0, respectively. TL1 and TL0 refer to the low-order bits of both timer/counter 1 and 0.

Serial Control Register
The Serial Data Buffer (SBUF) register is used to hold serial port input or output data depending on whether the serial port is receiving or transmitting data.

PSW definition

MSB							LSB
CY	AC	F0	RS1	RS0	OV	-	P

CY	PSW.7	Carry flag
AC	PSW.6	Auxiliary carry flag
F0	PSW.5	Flag 0 available to the user for general purpose
RS1	PSW.4	Register bank selector bit 1.
RS0	PSW.3	Register bank selector bit 0.
OV	PSW.2	Overflow flag
-	PSW.1	Usable as a general purpose flag
P	PSW.0	Parity flag. Set/clear by hardware at each instruction cycle to indicate an odd/ even number of "1" bus in the accumulator

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

Interrupt System

A sophisticated multiple-source, two-priority-level, nested interrupt system is provided. The interrupt system is shown as below diagram. The interrupt request flag and program memory location of interrupt service program is shown in table on next page.

- Five interrupt sources
- Each interrupt can be individually enabled/disabled
- Enabled interrupts can be globally enabled/disabled
- Each interrupt can be assigned to either of two priority levels
- Each interrupt vectors to a separate location in program memory
- Interrupt nesting to two levels
- External interrupt requests can be programmmed to be level- or transition- activated

Interrupt Overall

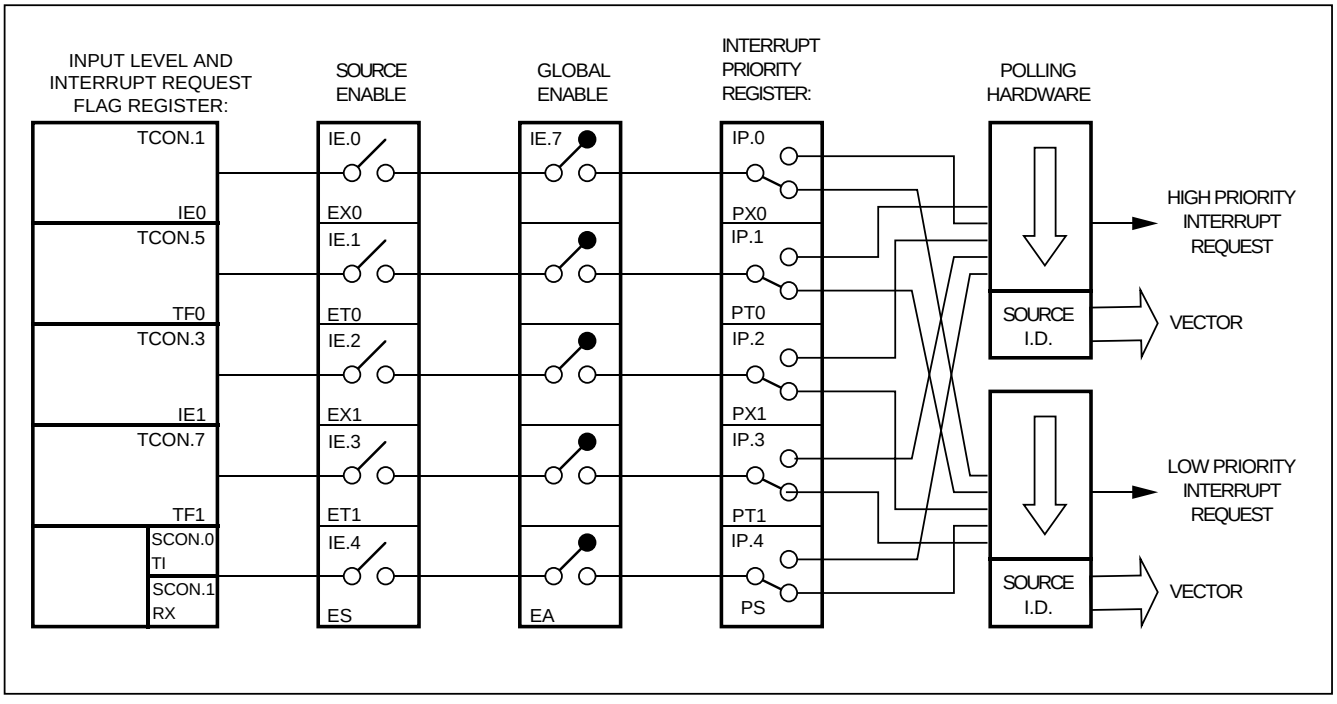
External events and the real-time driven onchip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a sophisticated multiple-source, two-priority-level, nested interrupt system is provided. Interrupt response latency ranges from 3µs to 7µs when using a 12 MHz crystal.

The MV20556 acknowledges interrupt requests from five sources: Two from external sources via the #INT0 and INT1 pins, one from each of the two internal counters and one from the serial I/O port. Each interrupt vectors to a separate location in Program Memory for its service program. Each of the five sources can be assigned to either of two priority levels and can be independently enabled and disabled. Additionally all enabled sources can be globally disabled or enabled. Each external interrupt is programmable as either level- or transition-activated and is active-low to allow the "wire or-ing" of several interrupt sources to the input pin. The interrupt system is shown diagrammatically in below figure.

Interrupt System Functional Description

Interrupts result in a transfer of control to a new program location. The program servicing the request begins at this address. In the MV20556 there are five hardware sources that can generate an interrupt request. The starting address of the interrupt service program for each interrupt source is shown in table on next page.

A resource requests an interrupt by setting its associated interrupt request flag in the TCON or SCON register, as detailed in following table. The interrupt request will be acknowledged if its interrupt enable bit in the Interrupt Enable register is set and if it is the highest priority resource requesting an interrupt. A resource's interrupt priority level is established as



Interrupt System(Cont'd)

Interrupt System Functional Description (Cont'd)

high or low by the polarity of a bit in the Interrupt Priority register. These bit assignments are shown in IP definition. Setting the resource's associated bit to a one (1) programs it to the higher level. The priority of multiple interrupt requests occurring simultaneously and assigned to the same priority level is also shown in below table.

The servicing of a resources's interrupt request occurs at the end of the instruction-in-progress. The processor transfers control to the starting address of this resource's interrupt service program and begins execution. Within the Interrupt Enable register (IE) there are six addressable flags. Five flags enable/disable the five interrupt sources when set/cleared. Setting/clearing the sixth flag permits a global enable/disable of each enabled interrupt request.

Setting/clearing a bit in the Interrupt Priority register (IP) establishes its associated interrupt request as a high/low priority (Table on next page). If a low-priority level interrupt is being serviced, a high-priority level interrupt will interrupt it. However, an interrupt source cannot interrupt a service program of the same or higher level.

The processor records the active priority level(s) by setting internal flip-flop(s). One of these non-addressable flip-flops is set while a low-level interrupt is being serviced. The other flip-flop is set while the high-level interrupt is being serviced. The appropriate flip-flop is set when the processor transfers control to the service program. The flip-flop corresponding to the interrupt level being serviced is reset when the processor executes an RETI Instruction.

To summarize, the sequence of events for an interrupt is: A resource provokes an interrupt by setting its associated interrupt request bit to let the processor know an interrupt condition has occurred. The CPU's internal hardware latches the interrupt request near the falling-edge of ALE internal signal in the tenth (10th), twenty-second (22nd), thirty-fourth (34th) and forty-six (46th) oscillator period of the instruction-in-progress. The interrupt request is conditioned by bits in the interrupt enable and interrupt priority registers. The processor acknowledges the interrupt by setting one of the two internal "priority-level active" flip-flops and performing a hardware subroutine call. The call pushes the PC (but not the PSW) onto the stack and, for most sources, clears the interrupt request flag. The service program is then executed. Control is returned to the main program when the RETI instruction is executed. The RETI instruction also clears one of the internal "priority-level active" flip-flops.

Most interrupt request flags (IE0, IE1, TF0 and TF1) are cleared when the processor transfers control to the first instruction of the interrupt service program. The TI and RI interrupt request flags are the exceptions and must be cleared as part of the serial port's interrupt service program.

The process whereby a high-level interrupt request interrupt a low-level interrupt service program is called nesting. In this case the address of the next instruction in the low-priority service program is pushed onto the stack, the stack pointer is incremented by two (2) and processor control is transferred to the Program Memory location of the first instruction of the high-level service program. The last instruction of the high-priority interrupt service program must be an RETI instruction. This instruction clears the high "priority-level-active" flip-flop. RETI also returns processor control to the next instruction of the low-level interrupt service program. Since the lower "priority-level-active" flip-flop has remained set, high priority interrupts are re-enable while further low priority interrupts remain disabled.

Interrupt Source	Request Flag	Bit Location	Priority Flags	Start address	
				Decimal	HEX
External Request 0	IE0	TCON.1	.0 (highest)	3	0003H
Internal timer 0/ counter 0	TF0	TCON.5	.1	11	000Bh
External request 1	IE1	TCON.3	.2	19	0013H
Internal timer 1/ counter 1	TF1	TCON.7	.3	27	001Bh
Internal Serial Port (Xmit)	TI	SCON.1	.4	35	0023h
Internal Serial Port (Rcvr)	RI	SCON.0	(lowest)		

Interrupt flags & addresses

Interrupt System(Cont'd)

The highest-priority interrupt request gets serviced at the end of the instruction-in progress unless the request is made in the last fourteen oscillator periods of the instruction-in-progress. Under this circumstance, the next instruction will also execute before the interrupt's subroutine call is made. The first instruction of the service program will begin execution twenty-four oscillator periods (the time required for the hardware subroutine call) after the completion of the instruction-in-progress or, under the circumstances mentioned earlier, twenty-four oscillator periods after the next instruction.

Thus, the greatest delay in response to an interrupt request is 86 oscillator periods (approximately 7μsec @ 12 MHz). Examples of the best and worst case conditions are illustrated in right side table.

External Interrupts

The external interrupt request inputs (#INT0 and #INT1) can be programmed for either transition-activated or level-activated operation. Control of the external interrupts is provided by the four low-order bits of TCON. When IT0 and IT1 are set to one (1), interrupt requests on #INT0 and #INT1 are transition-activated (high-to-low); or else they are low-level activated. IE0 and IE1 are the interrupt request flags. These flags are set when their corresponding interrupt request inputs at #INT0 and #INT1, respectively, are low when sampled by the MV20556 and the transition activated scheme is selected by IT0 and IT1. When IT0 and IT1 are programmed for level-activated interrupts, the IE0 and IE1 flags are not affected by the inputs #INT0 and INT1, respectively.

Transition-Activated Interrupts

The external interrupt request inputs (#INT0 and #INT1) can be programmed for high-to-low transition-activated operation. For transition-activated operation, the input must remain low for greater than twelve oscillator periods, but need not be synchronous with the oscillator. It is internally latched by the MV20556 near the falling-edge of ALE during an instruction's tenth, twenty-second, thirty-fourth and forty-sixth oscillator periods and, if the input is low, IE0 or IE1 is set.

The upward transition of a transition- activated input may occur at any time after the twelve oscillator period latching time, but the input must remain high for twelve oscillator periods before reactivation.

Level-Activated Interrupt

The external interrupt request inputs (#INT0 and #INT1)can be programmed for level-activated operation. The input is sampled by the MV20556 near the falling-edge of internal signal ALE during the instruction's tenth (10th), twenty-second (22nd), thirty-fourteen (34th) and forty-sixth (46th) oscillator periods.

MSB							LSB
EA	-	-	ES	ET1	EX1	ET0	EX0

EA	IE.7	Disable all interrupts. If EA=0, no interrupt will be acknowledged. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit. Cleared by software to disable all interrupts, independent of the state of IE. 4-IE.0
-	IE.6	Reserve for future use.
-	IE.5	Reserve for future use.
ES	IE.4	Enable Serial port control bit. Set/cleared by software to enable/disable interrupts from TI or RI flags.
ET1	IE.3	Enable or disable the timer 1 overflow interrupt. Set/cleared by software to enable/disable interrupts from timer/counter 1
EX0	IE.2	Reserve for future use. Enable External interrupt 1 control bit. Set/cleared by software to enable/disable interrupts from INT1.
ET0	IE.1	Enable or disable the timer 0 overflow interrupt. Set/cleared by software to enable/disable interrupts from timer/counter 0
EX1	IE.0	Enable External interrupt 0 control bit. Set/cleared by software to enable/disable interrupts from INT0

IE definition

Interrupt System (Cont'd)

that occurs fourteen oscillator periods before the end of the instruction in progress, an interrupt subroutine call is made. The level-activated input need be low only during the sampling that occurs fourteen oscillator periods before the end of the instruction-in-progress and may remain low during the entire execution of the service program. However, the input must be raised before the service program completes to avoid possible envoking a second interrupt.

MSB							LSB
-	-	-	PS	PT1	PX1	PT0	PX0

-	IP.7	Reserve for future use.
-	IP.6	Reserve for future use.
-	IP.5	Reserve for future use.
PS	IP.4	Serial Port Priority control bit. Set/cleared by software to specify high/low priority interrupts for Serial port.
PT1	IP.3	Defines the idle or power down mode interrupt priority level. Set/cleared by software to specify high/low priority interrupts for timer/counter1.
PX0	IP.2	External interrupt 1 Priority control bit. Set/cleared by software to specify high/low priority interrupts for INT1.
PT0	IP.1	Defines the timer 0 interrupt priority level. Set/cleared by software to specify high/low priority interrupts for timer/counter0.
PX1	IP.0	External interrupt 0 Priority control bit. Set/cleared by software to specify high/low priority interrupts for INT0.

IP definition

Timer/Counter

Timer/Counter Overall

The MV20556 contains two 16-bit counters for measuring time internals, measuring pulse widths, counting events and generating precise, periodic interrupt requests. Each can be programmed independently to operate as an 8048 8-bit timer with divide by 32 prescaler or as an 8-bit counter with divide by 32 prescaler (Mode 0), as a 16-bit time-interval or event counter (Mode 1), or as an 8-bit time-interval or event counter with automatic reload upon overflow (Mode 2).

Additionally, counter 0 can be programmed to a mode that divides it into one 8-bit time-internal or event counter and one 8-bit time-interval counter (Mode 3). When counter 0 is in Mode 3, counter 1 can be programmed to any of the three aforementioned modes, although it cannot set an interrupt request flag or generate an interrupt. This mode is useful because counter 1's overflow can be used to pulse the serial port's transmission-rate generator. Along with their multiple operating modes and 16-bit precision, the counters can also handle very high input frequencies. These range from 3 MHz to 40 MHz (for 3 MHz to 40 MHz crystal) when programmed for an input that is a division by 12 of the oscillator frequency and from 0 Hz to an upper limit of 1 MHz (for 25 MHz crystal) when programmed for external inputs. Both internal and external inputs can be gated to the counter by a second external source for directly measuring pulse widths.

The counters are started and stopped under software control. Each counter sets its interrupt request flag when it overflows from all ones to all zeros (or auto-reload value). The operating modes and input sources are summarized in right side Figures.

Counter 1/Timer 1

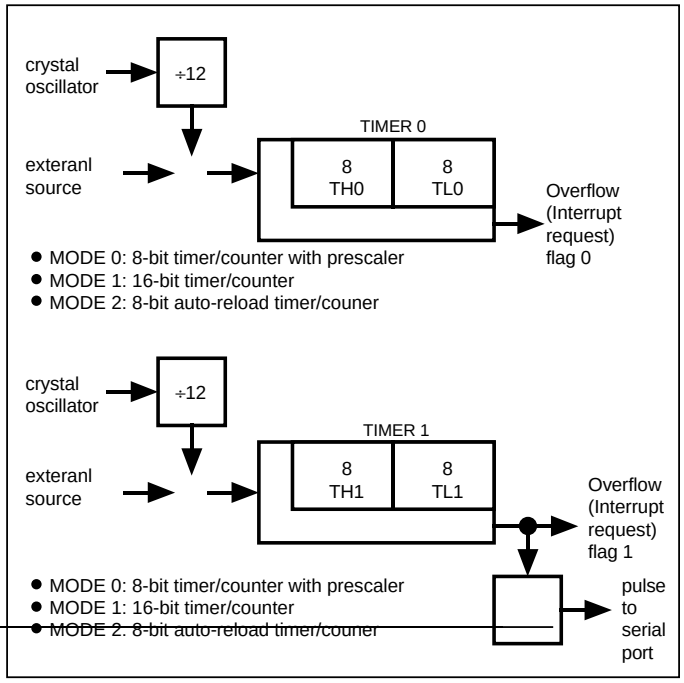
Counter 1/Timer 1 can be configured in one of four modes by software program code on the fly:

Mode 0: 8-bit timer/counter with prescaler
Provides an 8-bit counter with a divide-by-32 prescaler or an 8-bit timer with a divideby-32 prescaler.

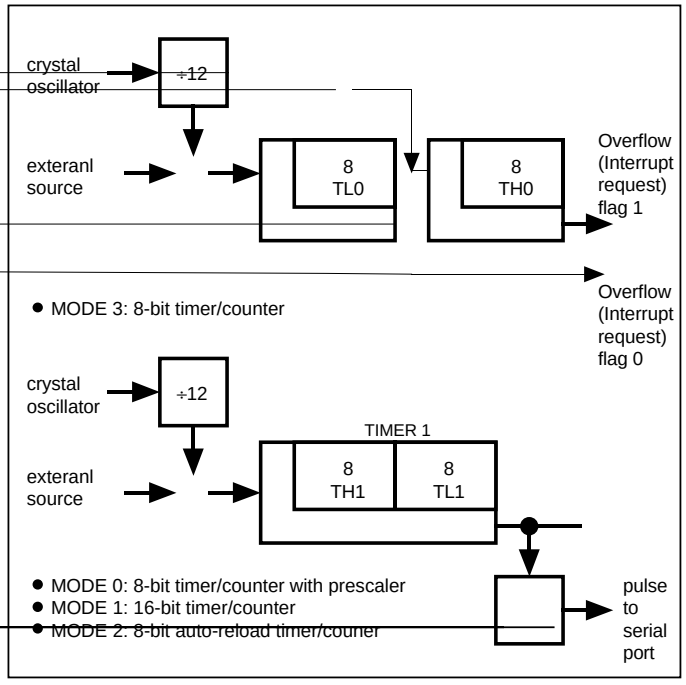
Mode 1: 16-bit timer/counter
Configures counter 1 as a 16-bit timer/counter.

Mode 2: 8-bit auto-reload timer/counter
Configures counter 1 as an 8-bit auto-reload timer/counter. TH1 holds the reload value. TL1 is incremented. The value in TH1 is reload onto TL1 when TL1 overflows from all ones.

Mode 3: Prevents incrementing of timer/counter
When counter 1's mode is reprogrammed to mode 3 (from mode 0, 1 or 2), it disables the incrementing of



Mode 0, 1 and 2



Mode 3

Timer/Counter (Cont'd)

the counter. This mode is provided as an alternative to use TR1 bit (TCON.6) to start and stop counter 1. The serial port receives a pulse each time that counter 1 overflows. The standard UART modes divide this pulse rate to generate the transmission rate.

mode 3: stop

Counter 0/Timer 0

Counter 0/Timer 0 can also be configured in one of four modes software program code on the fly:

Mode 0-2:
Mode 0-2 are the same as those for counter 1.

Mode 3: 8-bit timer/counter (TL1)
In mode 3, the configuration of TH0 is not affected by the bits in TMOD or TCON. It is configured solely as an 8-bit timer that is enabled for incrementing by TCON's TR1 bit. Upon TH0's overflows, the TF1 flag gets set. Thus, neither TR1 nor TF1 is available to counter 1 when counter 0 is in mode 3. The function of TR1 can be done by placing counter 1 in mode 3, so only the function of TF1 is actually given up by counter 1. In mode 3, TL0 is configured as an 8-bit timer/counter and is controlled, as usual, by the GATE (TMOD.3), C/#T(TMOD.2), TR0 (TCON.4) and TF0 (TCON.5) control bits.

Configuring of Timer/Counter
The use of the timer/counters is determined by two 8-bit registers, TMOD (timer mode) and TCON (timer control). The input to the counter circuitry from an external reference (for use as a counter), or from the on-chip oscillator (for use as a counter), or from the on-chip oscillator (for use as a timer), depending on whether TMOD's C/#T bit is set or cleared, respectively. When used as a timer base, the on-chip oscillator frequency is divided by twelve (12) before being input to the counter circuitry. When TMOD's Gate bit is set (1), the external reference input (T1, T0) or the oscillator input is gated to the counter conditional upon a second external input (#INT0, #INT1) being high. When the Gate bit is zero (0), the external reference or oscillator input is unconditionally enabled. In either case, the normal interrupt function of #INT0 and #INT1 is not affected by the counter's operation. If enabled, an interrupt will occur when the input at #INT0 or #INT1 is low. The counters are enabled for incrementing when TCON's TR1 and TR0 bits are set. When the counters overflow the TF1 and TF0 bits in TCON get set and interrupt requests are generated. The functions of the bits in TCON are shown in below table. The functions of the bits in TMOD are shown in table on next page.

Operation
The counter circuitry counts up to all 1's and then overflows to either 0's or the reload value. Upon overflow, TF1 or TF0 gets set. When an instruction

MSB							LSB
TF1	TR1	TF0	TR0	-	-	IDF	-

TF1	TCON.7	Timer 1 overflow flag. Set by hardware when the timer/counter 1 overflows. Cleared by hardware as processor vectors to the interrupt service routine.
TR1	TCON.6	Timer 1 run control bit. Set/cleared by software to turn timer/counter 1 ON/OFF.
TF0	TCON.5	Timer 0 overflow flag. Set by hardware when the timer/counter 0 overflows. Cleared by hardware as processor vectors to the interrupt service routine.
TR0	TCON.4	Timer 0 run control bit. Set/cleared by software to turn timer/counter 0 ON/OFF.
IE1	TCON.3	Interrupt 1 edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT1	TCON.2	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
IE0	TCON.1	Interrupt 0 edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT0	TCON.0	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

TCON definition

Timer/Counter (Cont'd)

changes the timer's mode or alters its control bits, the actual change occurs at the end of the instruction's execution.

The T1 and T0 inputs are sampled near the falling-edge of ALE in the tenth(10th), twenty-second(22nd), thirty-fourth(34th) and forty-sixth(46th) oscillator periods of the instruction-in-progress. They are also sampled in the twenty-second oscillator period of MOVX despite the absence of internal signal ALE. Thus, an external reference's high and low times must each be a minimum of twelve oscillator periods in duration. There is a twelve oscillator period delay from when a toggled input (transition from high to low) is sampled to when the counter is ineremented.

Reading/Reloading

The timer/counters can be read and reloaded on the fly. However, the 16-bit timer/counters must be read and loaded as two 8-bit bytes. During a read the potential "phasing error" can be programmed around, as follows:

```
RTC   MOV   A, TH0
      MOV   B, TL0
      CJNE  A, TH0, RTC
```

Timer 1				Timer 0			
MSB							LSB
GATE	C/#T	M1	M0	GATE	C/#T	M1	M0

GATE	When TRx (in TCON) is set and GATE=1, TIMER/COUNTERx will run only while INTx pin is high (hardware control). When GATE=0, TIMER/COUNTERx will run only while TRx=1 (software control).
C/#T	Timer or counter selector. Cleared for timer operation (input from internal system clock). Set for counter operation (input form Tx input pin).
M1	Mode selector bit.
M0	Mode selector bit.

M1	M0	Operating mode
0	0	Mode 0. (13-bit timer, by prescaled.)
0	1	Mode 1. (16-bit timer/counter)
1	0	Mode 2. (8-bit auto-load timer/counter)
1	1	Mode 3. (TL0 is an 8-bit timer/counter controlled by the standard timer 0 control bits. TH0 is an 8-bit timer and is controlled by timer 1 control bits.)
1	1	Mode 3. (Timer/counter 1 stopped).

TMOD definition

External Interface

Reset

Processor initialization is accomplished with acitivation of the RES pin. To reset the processor, this pin should be held high for at least twenty-four oscillator periods. Upon powering up, RES should be held high for at least 1 ms after the power supply stabilizes to allow the oscillator to stabilize. Upon receipt of RES, the processor ceases instruction execution and remains dormant for the duration of the pulse. The pins assume their initialization states within 2 machine cycles clocks. The low-going transition then initiates a sequence which requires approximately twelve oscillator periods to execute before ALE(internal signal) is generated and normal operation commences with the instruction at absolute location 0000H. This sequence ends with registers initialized as shown in right table.

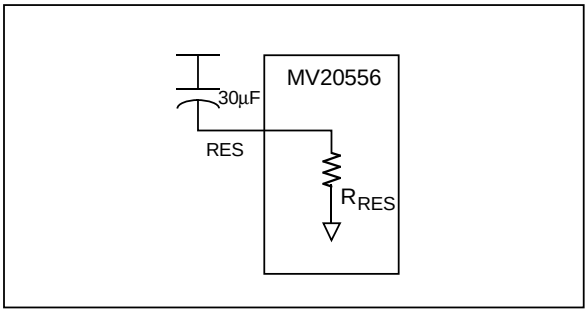
When the processor is reset all ports are immediately written with ones (1's).

The Schimitt-trigger input has a small internal pull down resistor which permits power-on reset (as shown in right to Figure) using only a small capacitor tied to VDD. A conventional external reset circuit, such as that in right Figure, can also be used.

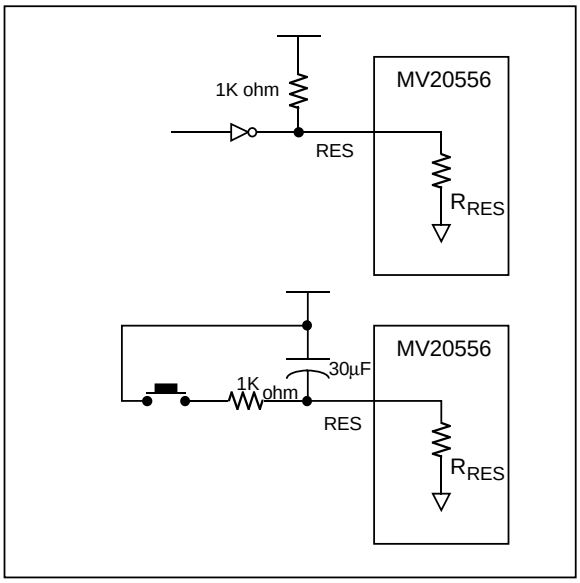
I OL

Output low current.

For port 1 and port 3, MV20556 provided I OL up to 18mA per pin typicallly at VOL=0.45V. User are free to choose any one of these 15 pins to perform this high current sink capability. But they are restricted: no more than 80 mA I OLs for all output pins.



Power-on Reset



External Reset

Register	Content after Reset at Power on	Content after Reset while running
PC	0000H	0000H
SP	07H	07H
PSW	00H	00H
DPH, DPL	00H	00H
A, B	00H	00H
IP	E0H or 00H	E0H or 00H
IE	60H or 00H	60H or 00H
SCON	00H	00H
TMOD	00H	00H
TCON	00H	00H
TH1, TH0	00H	00H
TL1, TL0	00H	00H
SBUF	indeterminate	indeterminate
Port 1 & 3	FFH (*1)	FFH (*1)
Internal RAM	indeterminate	unchanged

*1 configures all i/o pins as inputs

Register vs Reset

External Interface (Cont'd)

Idle Mode

During idle mode, the CPU is stopped but below blocks are kept functioning:clock generator, RAM, timer/ counters, serial port and interrupt block.

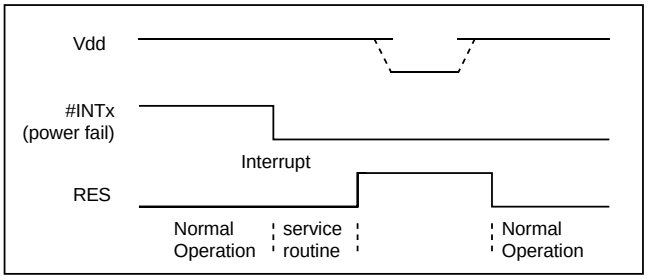
During idle mode, the CPU is stopped but below blocks are kept functioning: clock generator, RAM, timer/ counters, serial port and interrupt block. To save power consumption, user's software program can invoke this mode. The on-chip data RAM retains the values during this mode, but the processor stops executing instructions. In Idle mode (IDL=1), the oscillator continues to run and the interrput, and timer blocks continue to be clocked but the clock signal is gated off to the CPU. The activities of the CPU no longer exist unless waiting for an interrupt request.

-An instruction that sets flag (PCON.0) causes that to be the last instruction executed before going into the Idle Mode.

-In the Idle Mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer function.

-The CPU status is entirely preserved in its:
the Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data during Idle mode.

-There are two ways to terminate the Idle Mode.
1) By interrupt
Activation of any enabled interrupt will cause flag (PCON.0) to be cleared by hardware, termination the Idle Mode. After the program wakes up, the PC value will point as interrupt vector (if enable IE register) and execute interrupt service routine then return to PC+1 address after the program wakes up.
2) By hardware reset
Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 clocks) to complete the reset. All SFR and PC value will be cleared to reset value.
After the program wakes up, the PC value will be 0023h (if enable IE register) and execute interrupt service routine and then returns to PC+1 address after the program wakes up.



Power Down Mode

It saves the RAM content, stops the clock generator and disables every other blocks' function until the coming hardware reset. To save even more power consumption, user's software program can invoke this mode. The SFRs and the on-chip data RAM retain their values during this mode, but the porcessor stops executing instructions. In Power-Down mode (PD=1) the oscillator is frozen.

-An instruction that sets flag (PCON.1) causes that to be the last instruction executed before going into the Power Down Mode.

-In the Power Down Mode, the on-chip oscillator is stopped.
With the clock frozen, all functions are stopped, but the on-chip RAM and Special Function Registers are held.

-Reset redefines all the SFRs, but does not change the on-chip RAM.

-There is only one way to terminate the Power Down Mode - by hardware reset.
All SFR and PC value will be cleared to reset value.
After the program wakes up, the PC value will be 0023h (if enable IE register) and execute interrupt service routine and then returns to PC+1 address after the program wakes up.

-Care must be taken, however, to ensure that Vdd is not reduced before the Power Down Mode is invoked, and that Vdd is restored to its normal operating level before the Power Down Mode is terminated.

-The hardware reset must be held active long enough to allow the oscillator to restart and stabilize.

Data can be maintained valid in the Internal Data RAM while the remainder of the MV20556 is powered down. When powered down, the MV20556 consumes about 10% of normal operating power. During normal operation both the CPU and the internal RAM derive their power from VDD. However, the internal RAM will derive its power from RES when the voltage on VDD is more than a diode drop below that on RES.

When a power-supply failure is imminent, the user's system generates a "power-failure" signal to interrupt the

Mode	Program memory	Port 3
Idle	Internal	Data
Power Down	Internal	Data

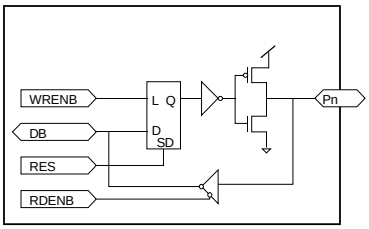
External Interface (Cont'd)

processor via #INT0 or #INT1. This power-failure signal must be early enough to allow the MV20556 before VDD falls below its operating limit. The program servicing the power-failure interrupt request must save any important data and machine status into Internal Data RAM. The service program must also enable the backup power supply to the RES pin. Applying power to the RES pin resets the MV20556 and retains the internal RAM data valid as the VDD power supply falls below limit. Normal operation resumes when RES is returned low. Figure on last page left column shows the waveforms for the power-down sequence.

Timing Generation

Timing generation for the MV20556 completely self-contained, except for the frequency reference which can be a crystal or external clock source. The on-board oscillator is a parallel anti-resonant circuit with a frequency range of 3 M to 40 MHz. The XTAL2 pin is the output of a high-gain amplifier, while XTAL1 is its input. A crystal connedted between XTAL1 and XTAL2 provides the feedback and phase shift required for oscillation. The 3 to 40 MHz range is also accomodated when an external TTL compatible clock is applied to XTAL1 as the frequency source.

The I/O Circuit



P1, P3

Absolute Maximal Rating

Symbol	Name	Rating	Unit
V_{DD} - Vss	DC supply Voltage	-0.5 - +7.0	V
V_{IN}	Input voltage	Vss-0.3 - V_{DD}+0.3	V
V_{OUT}	output voltage	Vss - V_{DD}	
T(Operating)	Operating Temperature	0 - +70	°C
T(Storage)	Storage Temperature	-55 - +125	°C

* Note: Operation beyond Absolute Maximal Rating can adversely affect device reliability.

Operating Conditions

Symbol	Description	Min.	Typ.	Max	Unit	Test Condition
T A	Ambient temperature under bias	0	25	70	°C	
Vdd	Supply voltage	4.5	5.0	5.5	V	Vss=0V
fosc 16	Oscillator Frequency of MV20556C16	3	16	16	MHz	
fosc 25	Oscillator Frequency of MV20556C25	3	25	25	MHz	
fosc 40	Oscillator Frequency of MV20556C40	3	40	40	MHz	

DC Characteristics

(16 MHz, typical operating conditions)

Symbol	Parameter	Valid	Min.	Typ.	Max	Unit	Test Conditions
VIL	Input Low Voltage		-0.5		0.2Vcc-0.1	V	
VIH	Input High Voltage	* note 2	0.2Vc+0.9		Vcc+0.5	V	
VIH1	Input High Voltage	XTAL, RES	0.7Vcc		Vcc+0.5	V	
VOH	Output High Voltage	Port 1,3	2.4			V	IOH=-60uA
			0.9Vcc			V	IOH=-10uA
I IL	Logical 0 Input Cruuent	Ports 1,3			-50	uA	Vin=0.45V
I TL	Logical 1 To 0 Transition Current	Ports 1,3			-650	uA	Vin=2V
I LI	Input Leakage Current	Port 1			10	uA	0.45<Vin<Vcc
I OL	Output Low Current	Port 1,3		18		mA	V OL=0.45V
I OL1+3	Output low current of 15 pins	Port 1 & 3			80	mA	
R RES	Reset Pulldown R		50		150	Kohm	
C IO	Pin Capacitance				10	pF	Freq=1MHz, Ta=25 ℃
I CC	Power Supply Current	Vdd		5	8	mA	Active mode, 16MHz
		Vdd		3	5	mA	Idle mode, 16MHz
		Vdd			1	uA	Power down mode

Note 2:=Except XTAL, RES

DC Characteristics at 25 MHz

to be available

DC Characteristics at 40 MHz

to be available

AC Characteristics

(16 MHz, typical operating conditions)

Symbol	Parameter	Valid Cycle	Min.	Typ.	Max	Unit	Remarks
T CHCL	Clock fall time					nS	
T CLCX	Clock low time					nS	
T CLCH	Clock rise time					nS	
T CHCX	Clock high time					nS	
T CLCL	Clock period			62		nS	
T SCLK	serial port clock cycle					uS	
T QVCH	Output data Setup to clock rise					nS	
T CHQX	Output data hold after clock rise					nS	
T CHDV	Clock rise to input data valid					nS	
T CHDX	Input data hold after clock rise					nS	
T POR	Power On reset time	Power on				nS	
T WAKE	Oscillator wake up time	Power Down Mode				nS	
T RES	Reset pulse width	Running		1.5		uS	24* T CLCH

AC Characteristics

(25 MHz, typical operating conditions)

Symbol	Parameter	Valid Cycle	Min.	Typ.	Max	Unit	Remarks
T CHCL	Clock fall time					nS	
T CLCX	Clock low time					nS	
T CLCH	Clock rise time					nS	
T CHCX	Clock high time					nS	
T CLCL	Clock period			40		nS	
T SCLK	serial port clock cycle					uS	
T QVCH	Output data Setup to clock rise					nS	
T CHQX	Output data hold after clock rise					nS	
T CHDV	clock rise to input data valid					nS	
T CHDX	Input data hold after clock rise					nS	
T POR	Power On reset time	Power on				nS	
T WAKE	Oscillator wake up time	Power Down Mode				nS	
T RES	Reset pulse width	Running		960		nS	24* T CLCH

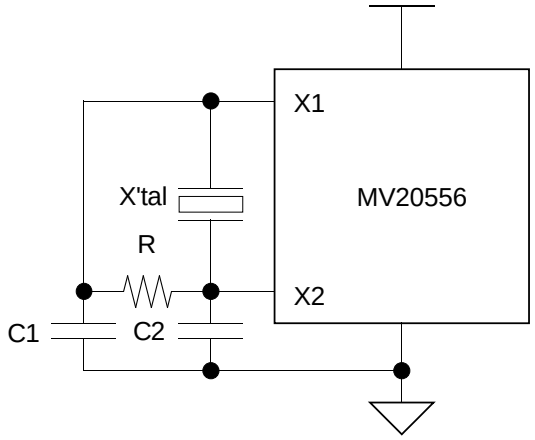
AC Characteristics

(40 MHz, typical operating conditions)

Symbol	Parameter	Valid Cycle	Min.	Typ.	Max	Unit	Remarks
T CHCL	Clock fall time					nS	
T CLCX	Clock low time					nS	
T CLCH	Clock rise time					nS	
T CHCX	Clock high time					nS	
T CLCL	Clock period			25		nS	
T SCLK	serial port clock cycle					uS	
T QVCH	Output data Setup to clock rise					nS	
T CHQX	Output data hold after clock rise					nS	
T CHDV	clock rise to input data valid					nS	
T CHDX	Input data hold after clock rise					nS	
T POR	Power On reset time	Power on				nS	
T WAKE	Oscillator wake up time	Power Down Mode				nS	
T RES	Reset pulse width	Running		600		nS	24* T CLCH

Application Reference

X'tal	3 MHz	6 MHz	16 MHz	25 MHz	40 MHz
C1	39 pF	39 pF	30 pF	15 pF	5 pF
C2	39 pF	39 pF	30 pF	15 pF	5 pF
R	open	open	open	62 Kohm	4700 ohm



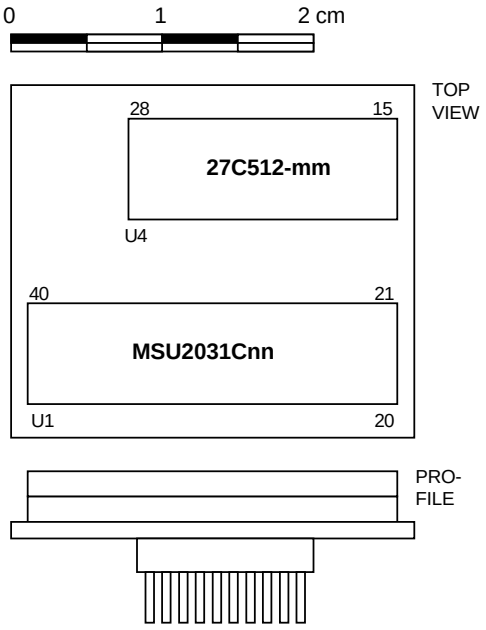
Emulation Board

Model number: M9257

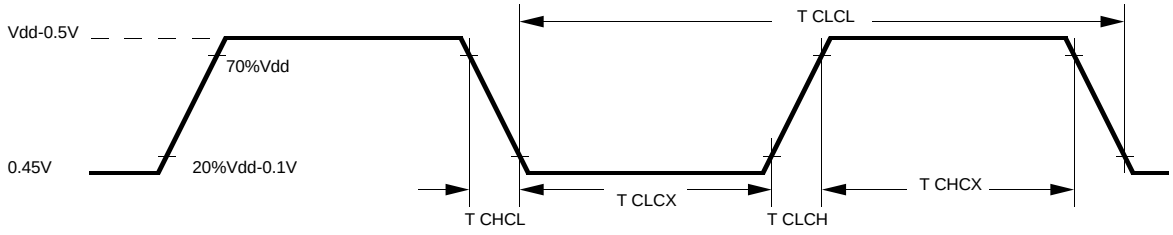
Two layers

- There is a 74373 chip soldered under chip 27C512
- The 4 KB program code should be programmed into the first 4 KB address location of EPROM 27C512-150 which is inserted into U4 location.
- When applying at different working clock, this M9257 demands different speed of EPROM chip

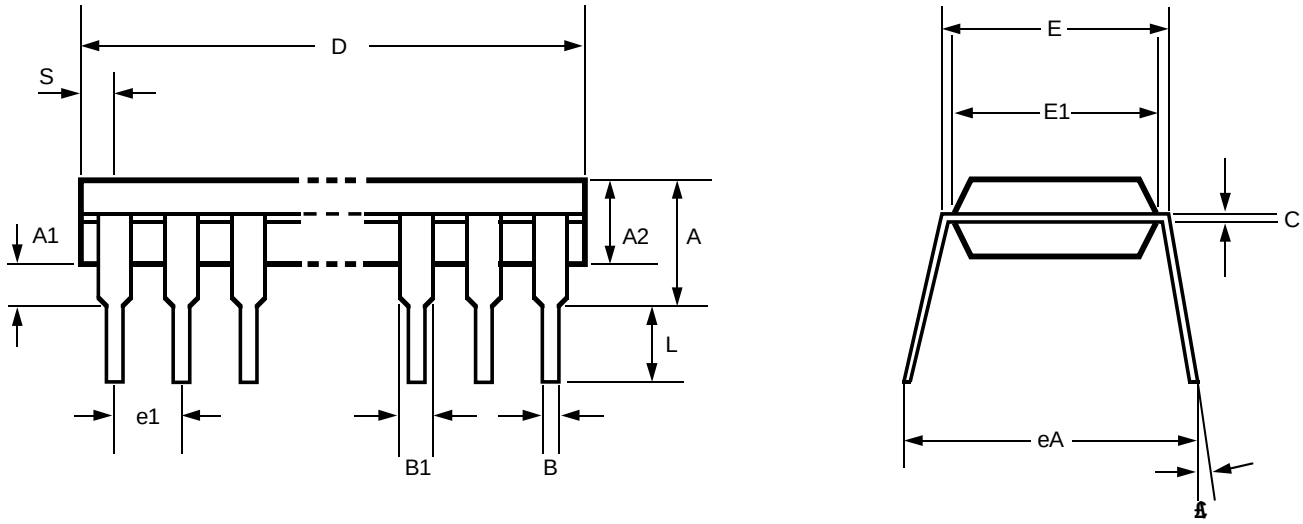
16 MHz: 27C512-200 or faster
25 MHz: 27C512-100 or faster
40 MHz: 27C512-60 or faster



Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



20L 300mil PDIP Information

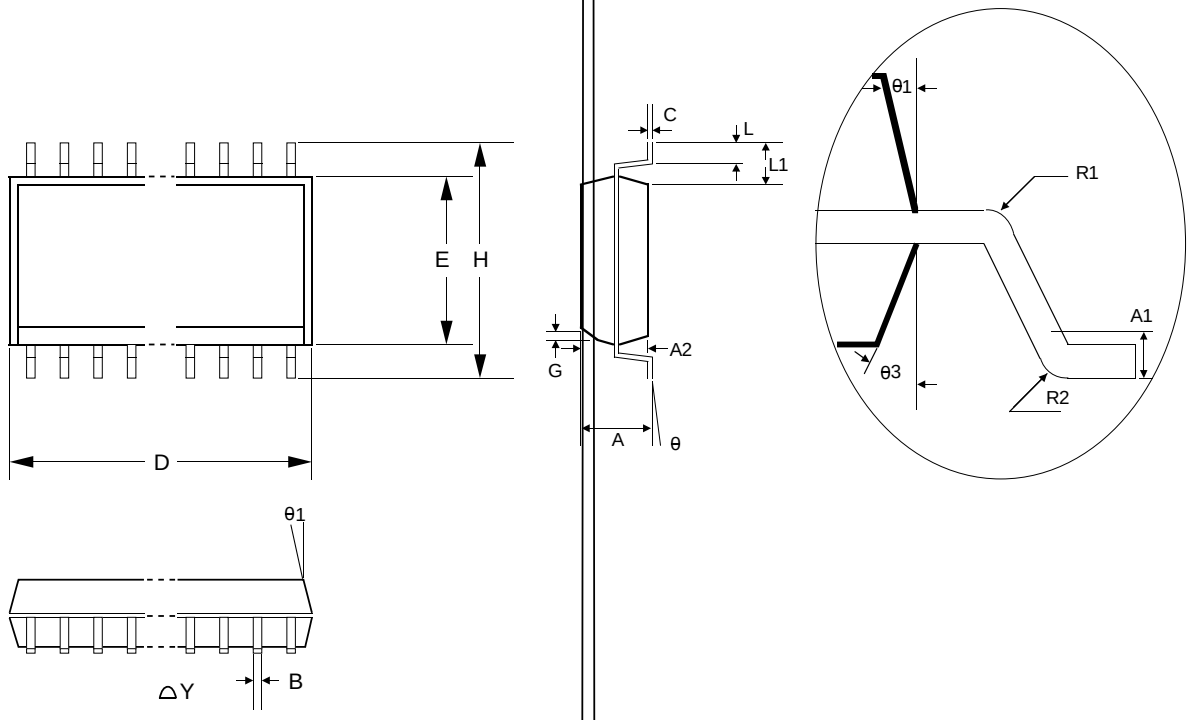


Note:

1. Dimension D Max & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimenseion D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/ infrusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visual inspection spec.

Symbol	Dimension Inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.175	- / 4.45
A1	0.010 / -	0.25 / -
A2	0.125 / 0.135	3.18 / 3.43
B	0.016 / 0.022	0.41 / 0.56
B1	0.058 / 0.064	1.47 / 1.63
C	0.008 / 0.014	0.20 / 0.36
D	- / 1.040	- / 26.42
E	0.290 / 0.310	7.37 / 7.87
E1	0.245 / 0.255	6.22 / 6.48
e1	0.090 / 0.110	2.29 / 2.79
L	0.120 / 0.140	3.05 / 3.58
α	0°/ 15°	0°/ 15°
eA	0.335 / 0.375	8.51 / 9.53
S	- / 0.075	- / 1.91

20L Small Outline Gull Wing Package



Note:

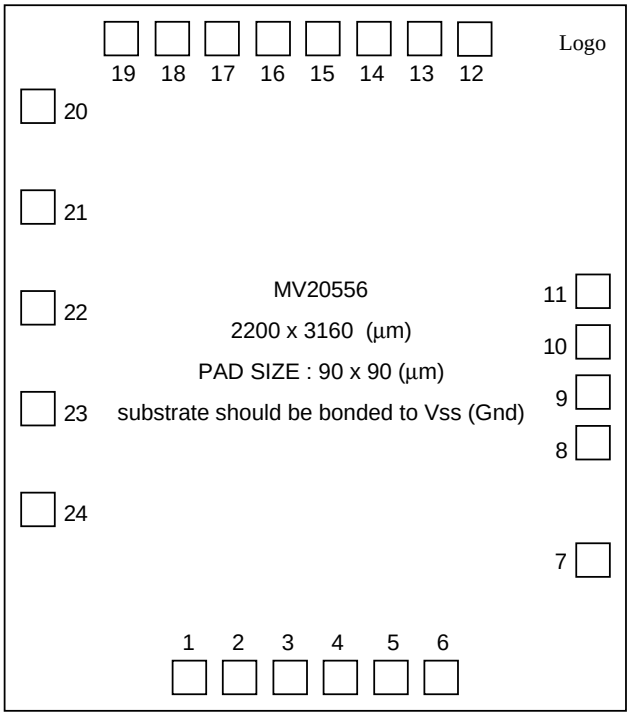
1. Dimension D does not include mold flash, protrustions or gate burrs. Allowance protrusion is 0.25mm per side. Dimensions E does not include inter-lead flash or protrusions.

Symbol	Dimension in Inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.100	2.36 / 2.64
A1	0.004 / 0.012	0.10 / 0.30
A2	0.091	2.31
B	0.013 / 0.020	0.33 / 0.51
C	0.007 / 0.011	0.18 / 0.21
D	0.496 / 0.508	12.60 / 12.94
E	0.291 / 0.299	7.39 / 7.51
e	0.050	1.27
G	0.020 x 45°	-
H	0.394 / 0.419	10.01 / 10.64
L	0.015 / 0.050	0.38 / 1.21
L1		
R1		
R2		
θ	0° / 8°	as left
θ1	7° REF	as left
θ3	7° REF	as left
C	0.004	0.10

Bonding Information

Index	PAD-NAME	X-COORD	Y-COORD
1	P0.7	540	168
2	VDD	738	168
3	VDD	889	168
4	RES	1085	168
5	RxD / P3.0	1306	168
6	TxD / P3.1	1527	168
7	XTAL2	1934	632
8	XTAL1	1934	954
9	#INT0 / P3.2	1934	1186
10	#INT1 / P3.3	1934	1413
11	T0 / P3.4	1934	1638
12	T1 / P3.5	1735	2244

Index	PAD-NAME	X-COORD	Y-COORD
13	VSSGND	1536	2244
14	VSSGND	1385	2244
15	VSSGND	1234	2244
16	NC	1037	2244
17	P3.7	816	2244
18	P1.0	595	2244
19	P1.1	374	2244
20	P1.2	168	1906
21	P1.3	168	1678
22	P1.4	168	1453
23	P1.5	168	1226
24	P1.6	168	1001



pid 256* 11/96 (6)
pid 256** 07/97 (27)

Taiwan
#1 Creation Road I,
Science - based Industrial Park,
Hsinchu, 30077
Taiwan, ROC
"audio_reply@mosel.com.tw"
TEL: 886-3-577-0055
FAX: 886-3-577-2788
FAX: 886-3-578-4732
Mdm: 886-3-578-0493

Taipei
7F, #102 Section 3,
Ming Chung E. Road,
Taipei,105
Taiwan, ROC

TEL: 886-2-545-1213
FAX: 886-2-545-1214
Mdm: 886-2-545-1464

China
(Vitelic HKG ShenZhen)
Room #209
San Da building,
#19 ZhenHua Road,
Futian, ShenZhen city,
P.R.China

TEL: 86-755-334-5766
FAX: 86-755-332-3995
Mdm: 86-755-332-3995

Hongkong
#19 Dai Fu Street,
Taipo Industrial Estate,
Taipo, N.T.
Hongkong
TEL: 852-2388-8277(MKO)
TEL: 852-2665-4883
FAX: 852-2664-2406
FAX: 852-2770-8011(MKO)
Mdm: 852-2388-0244

U.S.A.
#3910 North First Street,
San Jose,
CA. 65134-1501
U.S.A.

TEL: 1-408-433-6000
FAX: 1-408-433-0952

Japan
Room 302, Annex-G,
Higashi-Nakano,
Nakano-Ku, Tokyo 164
Japan

TEL: 81-3-3365-2851
FAX: 81-3-3365-2836

http:\\www.moselvitelic.com

3-digit production code
filled by MVI only

To: Mosel Vitelic Inc.
886-3-5772788
Attn: Sales & Marketing Department

Product Request Form

We hereby request MVI to start producing MV20556 which is specified below .

Please send us the product code and a hardcopy of data code as well as data code file duplicated on floppy diskette. No further confirmation is necessary.

Production will start automatically once you receive our data code and verify that the checksum is match.

Mass Production of the captioned device shall be done in accordance with the purchase order(s) issued by us or a company specified by us. All terms and conditions are based on the development agreement and/or contract signed between MVI and us.

Data Code Descriptions	
Code Length	
File Length	
File Name	
Checksum	h
Unused Data Byte	☐ 00h filled ☐ FFh filled
Format	☐ HEX format ☐ Binary code format
Media	☐ EPROM ☐ 8751 chip ☐ File on Floppy ☐ E-mail file

IC descriptions

☐ Dice form ☐ 20L-SOP ☐ 20L-PDIP

☐ 16 MHz ☐ 25 MHz ☐ 40 MHz

Top Marking (fill only for packaged)

☐ Use MVI logo, date code and part number
☐ Use my specifications as described below

Specify below fields only for customer top marking

Date code location descriptions

☐ Use regular date code as MVI's
☐ Leave it as blank
☐ use right side five letters ☐☐☐☐☐

Logo Specifications

☐ Leave it blank
☐ Use my specifications as attachment

Part number specified, less than 15 digits

☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐

Phone # : _____ Fax # : _____

Company Name : _____

Signature : _____

Name (Typed) : _____

Position Title : _____

Department, Section : _____

Signature Date : _____

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886-3-5772788
Attn: Sales & Marketing Department

Logo Top Marking Request & spec.

We hereby request MVI to have our logo printed on top of the device package. Below is the specification of our logo in 20:1 scale base. This logo diagram is clear enough and is able to be shrunk directly to fit into available top marking area described on page.

Phone # : _____ Fax # : _____

Company Name : _____

Signature : _____

Name (Typed) : _____

Position Title : _____

Department, Section : _____

Signature Date : _____