

# 8-bit Proprietary Microcontroller

CMOS

## F<sup>2</sup>MC-8L MB89601R Series

### MB89601R/603/P601/PV620

#### ■ DESCRIPTION

The MB89601R series is compact one-chip microcontrollers using the F<sup>2</sup>MC-8L\* CPU core for which can operate at low voltage but at high speed. The microcontrollers contain peripheral functions such as timers, a serial interface and an external interrupt and are applicable to welfare products, especially portable devices required savings in board space.

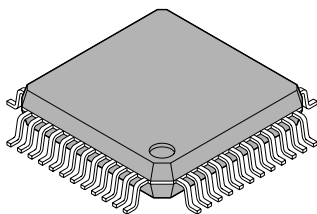
\*: F<sup>2</sup>MC stands for FUJITSU Flexible Microcontroller.

#### ■ FEATURES

- High-speed processing at low voltage  
Minimum execution time: 0.5  $\mu$ s/3.5 V at 8 MHz
- F<sup>2</sup>MC-8L family CPU core
- Timer  
8-bit PWM timer (also usable as a reload timer)
- Serial interface  
Switchable transfer direction allows communication with various equipment.
- External interrupt  
Capable of wake-up from low-power consumption modes (with an edge detection function)
- Low-power consumption modes  
Stop mode (Oscillation stops to minimize the current consumption.)  
Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)

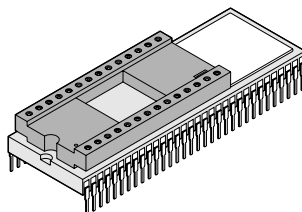
#### ■ PACKAGE

48-pin Plastic SQFP



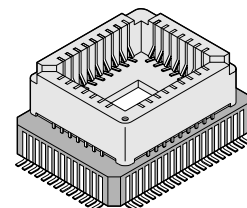
(FPT-48P-M05)

64-pin Ceramic MDIP



(MDP-64C-P02)

64-pin Ceramic MQFP



(MQP-64C-P01)

# MB89601R Series

## ■ PRODUCT LINEUP

| Part number<br>Parameter         | MB89601R   | MB89603                             | MB89P601  | MB89PV620*1  |
|----------------------------------|--|-------------------------------------|---|--|
| Classification                   | Mass production products<br>(mask ROM products)  |                                     | One-time PROM<br>product  | Piggyback/evaluation<br>product (for evaluation<br>and development)  |
| ROM size<br>(internal ROM)       | 4 K × 8 bits<br>(internal mask ROM)  | 8 K × 8 bits<br>(internal mask ROM) | 4 K × 8 bits<br>(external ROM, programming<br>with general-purpose<br>EPROM programmer) | 32 K × 8 bits<br>(external ROM)  |
| RAM size                         | 80 × 8 bits  |                                     |   | 1 K × 8 bits   |
| CPU functions                    | Number of instructions: 136<br>Instruction bit length: 8 bits<br>Instruction length: 1 to 3 bytes<br>Data bit length: 1, 8, 16 bits<br>Minimum execution time: 0.5 μs/8 MHz<br>Interrupt processing time: 4.5 μs/8 MHz                         |                                     |   |  |
| Ports                            | Input ports: 1 (also serve as peripherals.)<br>Output ports: none<br>I/O ports (N-ch open-drain): 8 (3 ports also serve as peripherals)<br>Output ports (CMOS): none<br>I/O ports (CMOS): 24 (1 port also serves as peripherals.)<br>Total: 33 |                                     |   | 5 (4 ports also serve as<br>peripherals.)<br>8 (8 ports also serve as<br>peripherals.)<br>8 (4 ports also serve as<br>peripherals.)<br>8 (8 ports also serve as<br>peripherals.)<br>24 (24 ports also serve<br>as<br>peripherals.)<br>53 |
| 8-bit PWM timer                  | 8-bit reload timer operation (toggled output capable, operating clock cycle: 0.5 to 8 μs)<br>8-bit resolution PWM operation (conversion cycle: 128 to 2048 μs)   |                                     |   |  |
| 8-bit pulse-width<br>count timer | none   |                                     |   | 8-bit timer operation<br>8-bit reload timer<br>operation<br>8-bit pulse-width<br>measurement operation   |
| 16-bit timer/counter             | none   |                                     |   | 16-bit timer operation<br>16-bit event counter   |
| 8-bit serial I/O                 | 8 bits<br>LSB first/MSB first selectability<br>One clock selectable from four transfer clocks<br>(one external shift clock, three internal shift clocks: 1.0 μs, 4.0 μs, 16.0 μs)  |                                     |   | SI/O × 2 channels  |
| 8-bit A/D converter              | none   |                                     |   | 8-bit resolution × 8<br>channels<br>A/D conversion mode<br>Sense mode<br>Reference voltage<br>input  |
| External interrupt               | Edge selection, interrupt vector, source flag<br>Rising edge/falling edge selectability<br>Used also for wake-up from stop/sleep modes.<br>(Edge detection is also permitted in stop mode.)  |                                     |   | External interrupt × 4<br>channels   |

(Continued)

(Continued)

| Part number<br>Parameter | MB89601R              | MB89603        | MB89P601 | MB89PV620*1                        |
|--------------------------|-----------------------|----------------|----------|------------------------------------|
| Standby mode             | Sleep mode, stop mode |                |          |                                    |
| Process                  | CMOS                  |                |          |                                    |
| Operating voltage*1      | 2.2 V to 6.0 V        | 2.7 V to 6.0 V |          |                                    |
| EPROM for use            | —                     |                |          | MBM27C256A-20TV<br>MBM27C256A-20CZ |

\*1: The piggyback/evaluation product is applicable to the MB89620 series.

\*2: Varies with conditions such as the operating frequency. (See section “■ Electrical Characteristics.”)

## ■ PACKAGE AND CORRESPONDING PRODUCTS

| Package     | MB89601R<br>MB89603<br>MB89P601 | MB89PV620 |
|-------------|---------------------------------|-----------|
| DIP-48P-M05 | ○                               | ×         |
| MDP-64C-P02 | ×                               | ○         |
| MQP-64C-P01 | ×                               | ○         |

○ : Available    × : Not available

Note: For more information about each package, see section “■ Package Dimensions.”

## ■ DIFFERENCES AMONG PRODUCTS

### 1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89601R, MB89603, MB89P601, upper than 0140<sub>H</sub> of each register bank cannot be used.
- The stack area, etc., is set at the upper limit of the RAM.
- External area is used.

### 2. Current Consumption

- In the case of the MB89PV620, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

However, the current consumption in sleep/stop modes is the same. (For more information, see sections “■ Electrical Characteristics” and “■ Example Characteristics.”)

### 3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

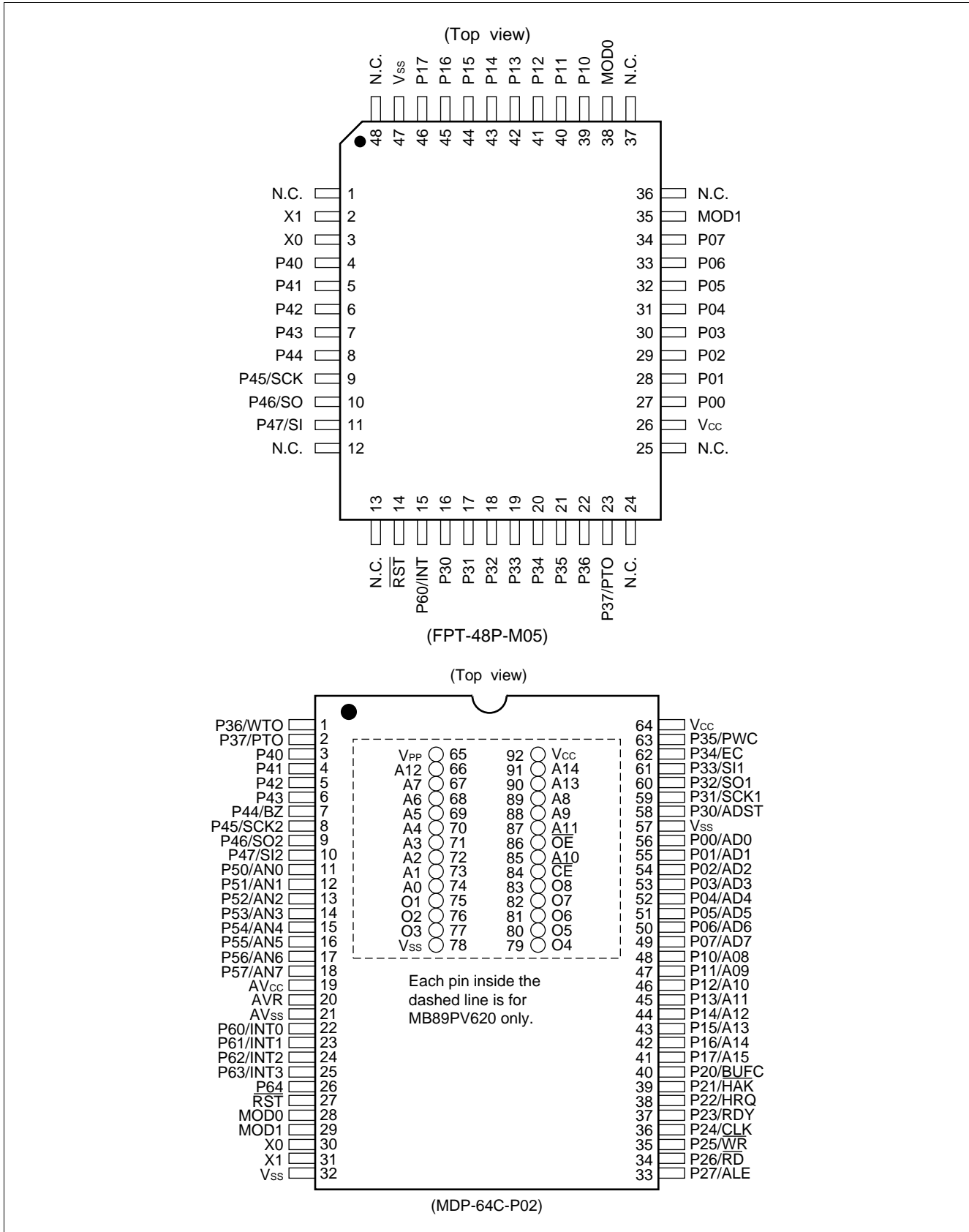
Before using options check “■ Mask Options.”

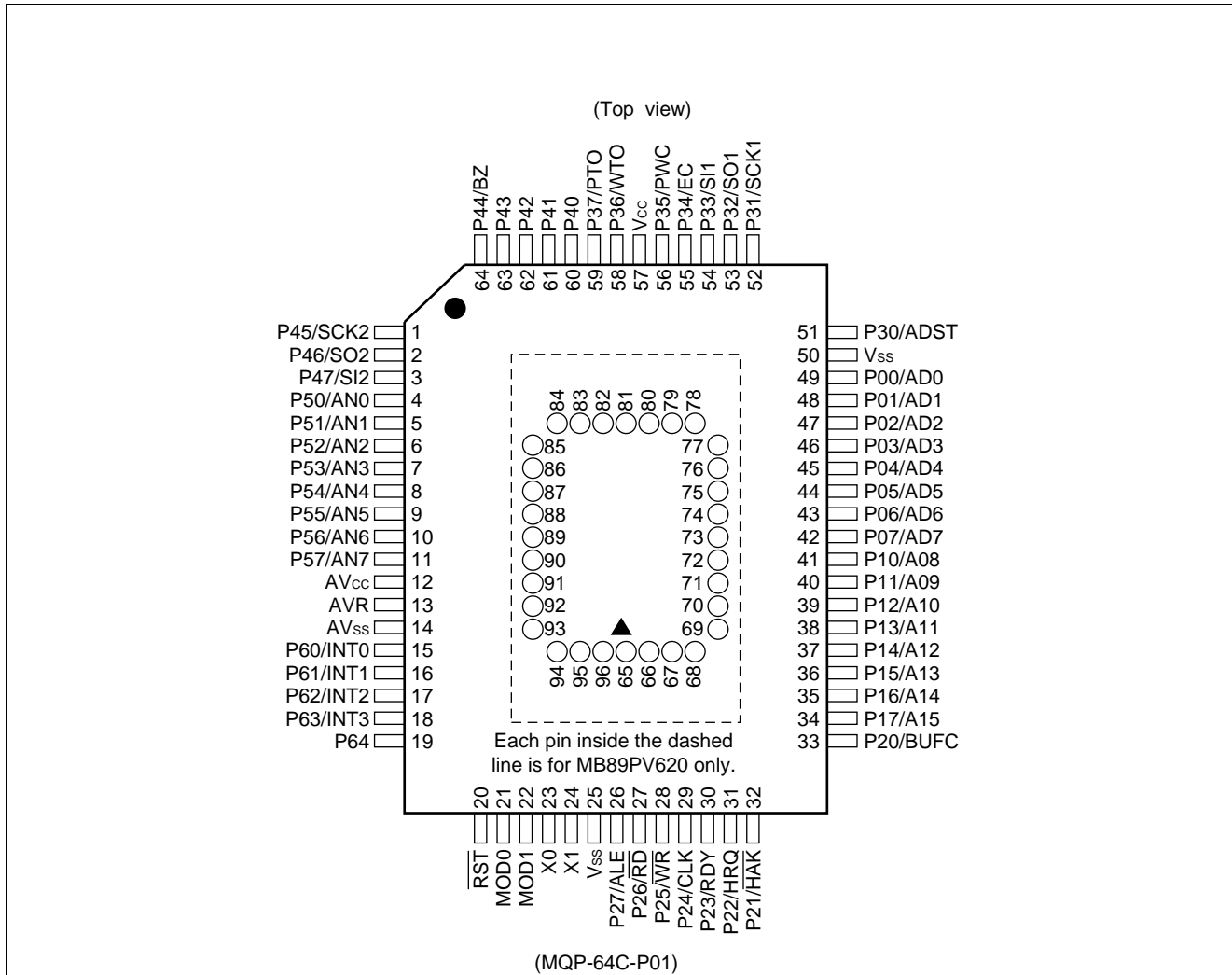
Take particular care on the following point:

- Options are fixed on the MB89PV620 and MB89P601.

# MB89601R Series

## PIN ASSIGNMENT





• Pin assignment on package top (MB89PV620 only)

| Pin no. | Pin name        | Pin no. | Pin name        | Pin no. | Pin name        | Pin no. | Pin name        |
|---------|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|
| 65      | N.C.            | 73      | A2              | 81      | N.C.            | 89      | $\overline{OE}$ |
| 66      | V <sub>PP</sub> | 74      | A1              | 82      | O4              | 90      | N.C.            |
| 67      | A12             | 75      | A0              | 83      | O5              | 91      | A11             |
| 68      | A7              | 76      | N.C.            | 84      | O6              | 92      | A9              |
| 69      | A6              | 77      | O1              | 85      | O7              | 93      | A8              |
| 70      | A5              | 78      | O2              | 86      | O8              | 94      | A13             |
| 71      | A4              | 79      | O3              | 87      | $\overline{CE}$ | 95      | A14             |
| 72      | A3              | 80      | V <sub>SS</sub> | 88      | A10             | 96      | V <sub>CC</sub> |

N.C.: Internally connected. Do not use.

# MB89601R Series

## ■ PIN DESCRIPTION

- MB89601R/603/P601

| Pin no.<br>SQFP*                    | Pin name                | Circuit type | Function  |
|-------------------------------------|-------------------------|--------------|---|
| 3                                   | X0                      | A            | Crystal oscillator pins   |
| 2                                   | X1                      |              |   |
| 38                                  | MOD0                    | B            | Operating mode selection pins<br>Connect directly to V <sub>SS</sub> .  |
| 35                                  | MOD1                    |              |   |
| 14                                  | $\overline{\text{RST}}$ | C            | Reset I/O pin<br>This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L". |
| 27 to 34                            | P00 to P07              | D            | General-purpose I/O ports   |
| 39 to 46                            | P10 to P17              |              |   |
| 16 to 22                            | P30 to P36              | E            | General-purpose I/O ports<br>This port is a hysteresis input type.<br>A software pull-up resistor is provided as an option.   |
| 23                                  | P37/PTO                 |              | General-purpose I/O port<br>This port is a hysteresis input type.<br>Also serves as the toggle output for the 8-bit PWM timer.<br>A software pull-up resistor is provided as an option.   |
| 4 to 8                              | P40 to P44              | G            | N-ch open-drain I/O port<br>This port is a hysteresis input type.   |
| 9                                   | P45/SCK                 |              | N-ch open-drain I/O port<br>This port is a hysteresis input type.<br>Also serves as the clock I/O for the serial I/O.   |
| 10, 11                              | P46/SO,<br>P47/SI       |              | N-ch open-drain I/O port<br>This port is a hysteresis input type.<br>Also serves as the data output for the serial I/O.   |
| 15                                  | P60/INT                 | I            | General-purpose input-only port<br>Also serves as an external interrupt input.<br>This port is a hysteresis input type.   |
| 26                                  | V <sub>CC</sub>         | —            | Power supply pin  |
| 47                                  | V <sub>SS</sub>         | —            | Power supply (GND) pin  |
| 1, 12, 13,<br>24, 25, 36,<br>37, 48 | N.C.                    | —            | Be sure to leave them open.   |

\* : FPT-48P-M05

# MB89601R Series

• MB89PV620

| Pin no.  |          | Pin name                     | Circuit type | Function  |
|----------|----------|------------------------------|--------------|---|
| MDIP*1   | MQFP*2   |                              |              |   |
| 30       | 23       | X0                           | A            | Crystal oscillator pins   |
| 31       | 24       | X1                           |              |   |
| 28       | 21       | MOD0                         | B            | Operating mode selection pins<br>Connect directly to V <sub>CC</sub> or V <sub>SS</sub> .   |
| 29       | 22       | MOD1                         |              |   |
| 27       | 20       | $\overline{\text{RST}}$      | C            | Reset I/O pin<br>This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L". |
| 56 to 49 | 49 to 42 | P00/AD0 to P07/AD7           | D            | General-purpose I/O ports<br>When an external bus is used, this port function as multiplex pins of lower address output and data I/O.   |
| 48 to 41 | 41 to 34 | P10/A08 to P17/A15           | D            | General-purpose I/O ports<br>When an external bus is used, this port function as a upper address output.  |
| 40       | 33       | P20/BUFC                     | F            | General-purpose output-only port<br>When an external bus is used, this port can also be used as a buffer control output by setting the BCTR.  |
| 39       | 32       | P21/ $\overline{\text{HAK}}$ | F            | General-purpose output-only port<br>When an external bus is used, this port can also be used as a hold-acknowledge by setting the BCTR.   |
| 38       | 31       | P22/HRQ                      | D            | General-purpose output-only port<br>When an external bus is used, this port can also be used as a hold request input by setting the BCTR.   |
| 37       | 30       | P23/RDY                      | D            | General-purpose output-only port<br>When an external bus is used, this port functions as a ready input.   |
| 36       | 29       | P24/CLK                      | F            | General-purpose output-only port<br>When an external bus is used, this port functions as a clock output.  |
| 35       | 28       | P25/ $\overline{\text{WR}}$  | F            | General-purpose output-only port<br>When an external bus is used, this port functions as a write signal output.   |
| 34       | 27       | P26/ $\overline{\text{RD}}$  | F            | General-purpose output-only port<br>When an external bus is used, this port functions as a read signal output.  |

(Continued)

\*1: MDP-64C-P02

\*2: MQP-64C-P01

# MB89601R Series

(Continued)

| Pin no. |          | Pin name   | Circuit type | Function  |
|---------|----------|------------|--------------|---|
| MDIP*1  | MQFP*2   |            |              |   |
| 33      | 26       | P27/ALE    | F            | General-purpose output-only port<br>When an external bus is used, this port functions as an address latch signal output.                        |
| 58      | 51       | P30/ADST   | E            | General-purpose I/O port<br>Also serves as the external activation input for the A/D converter.<br>This port is a hysteresis input type.        |
| 59      | 52       | P31/SCK1   | E            | General-purpose I/O port<br>Also serves as the clock I/O for the serial I/O 1.<br>This port is a hysteresis input type.                         |
| 60      | 53       | P32/SO1    | E            | General-purpose I/O port<br>Also serves as the data output for the serial I/O 1.<br>This port is a hysteresis input type.                       |
| 61      | 54       | P33/SI1    | E            | General-purpose I/O port<br>Also serves as the data input for the serial I/O 1.<br>This port is a hysteresis input type.                        |
| 62      | 55       | P34/EC     | E            | General-purpose I/O port<br>Also serves as the external clock input for the 16-bit timer/counter.<br>This port is a hysteresis input type.      |
| 63      | 56       | P35/PWC    | E            | General-purpose I/O port<br>Also serves as the measured-pulse input for the 8-bit pulse width-counter.<br>This port is a hysteresis input type. |
| 1       | 58       | P36/WTO    | E            | General-purpose I/O port<br>Also serves as the toggle output for the 8-bit pulse-width counter.<br>This port is a hysteresis input type.        |
| 2       | 59       | P37/PTO    | E            | General-purpose I/O port<br>Also serves as the toggle output for the 8-bit PWM timer.<br>This port is a hysteresis input type.                  |
| 3 to 6  | 60 to 63 | P40 to P43 | G            | N-ch open-drain I/O ports<br>This port is a hysteresis input type.  |
| 7       | 64       | P44/BZ     | G            | N-ch open-drain I/O port<br>Also serves as a buzzer output.<br>This port is a hysteresis input type.  |
| 8       | 1        | P45/SCK2   | G            | N-ch open-drain I/O port<br>Also serves as the clock I/O for the serial I/O 2.<br>This port is a hysteresis input type.                         |
| 9       | 2        | P46/SO2    | G            | N-ch open-drain I/O port<br>Also serves as the data output for the serial I/O 2.<br>This port is a hysteresis input type.                       |

(Continued)

\*1: MDP-64C-P02

\*2: MQP-64C-P01



# MB89601R Series

(Continued)

| Pin no.   |           | Pin name                | Circuit type | Function   |
|-----------|-----------|-------------------------|--------------|--|
| MDIP*1    | MQFP*2    |                         |              |  |
| 10        | 3         | P47/SI2                 | G            | N-ch open-drain I/O port<br>Also serves as the data I/O for the serial I/O 2.<br>This port is a hysteresis input type.   |
| 11 to 18  | 4 to 11   | P50/AN0 to<br>P57/AN7   | H            | N-ch open-drain output-only ports<br>Also serves as the analog input for the A/D converter.                              |
| 22 to 25  | 15 to 18  | P60/INT0 to<br>P63/INT3 | I            | General-purpose input-only ports<br>Also serves as an external interrupt input.<br>This port is a hysteresis input type. |
| 26        | 19        | P64                     | I            | General-purpose input-only port<br>This port is a hysteresis input type.   |
| 64        | 57        | V <sub>CC</sub>         | —            | Power supply pin   |
| 32,<br>57 | 25,<br>50 | V <sub>SS</sub>         | —            | Power supply (GND) pins  |
| 19        | 12        | AV <sub>CC</sub>        | —            | A/D converter power supply pin   |
| 20        | 13        | AVR                     | —            | A/D converter reference voltage input pin  |
| 21        | 14        | AV <sub>SS</sub>        | —            | A/D converter power supply pin.<br>Use this port at the same voltage as V <sub>SS</sub> .                                |

\*1: MDP-64C-P02

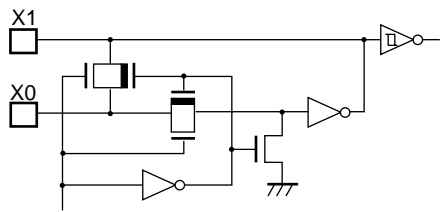
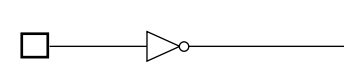
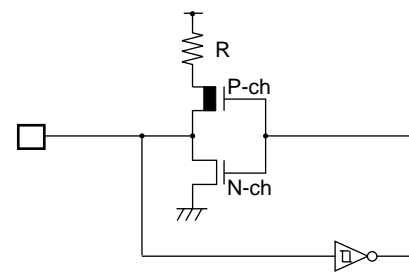
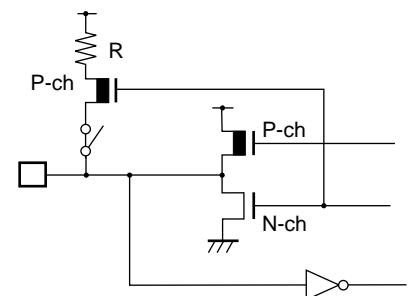
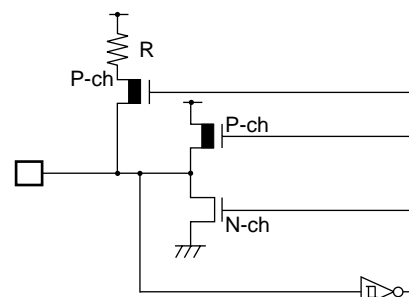
\*2: MQP-64C-P01

# MB89601R Series

• External EPROM pins (MB89PV620 only)

| Pin no. |                      | Pin name        | I/O | Function   |
|---------|----------------------|-----------------|-----|--|
| MDIP    | MQFP                 |                 |     |  |
| 65      | 66                   | V <sub>PP</sub> | O   | "H" level output pin                                     |
| 66      | 67                   | A12             | O   | Address output pins                                      |
| 67      | 68                   | A7              |     |  |
| 68      | 69                   | A6              |     |  |
| 69      | 70                   | A5              |     |  |
| 70      | 71                   | A4              |     |  |
| 71      | 72                   | A3              |     |  |
| 72      | 73                   | A2              |     |  |
| 73      | 74                   | A1              |     |  |
| 74      | 75                   | A0              |     |  |
| 75      | 77                   | O1              | I   | Data input pins  |
| 76      | 78                   | O2              |     |  |
| 77      | 79                   | O3              |     |  |
| 78      | 80                   | V <sub>SS</sub> | O   | Power supply (GND) pin                                   |
| 79      | 82                   | O4              | I   | Data input pins  |
| 80      | 83                   | O5              |     |  |
| 81      | 84                   | O6              |     |  |
| 82      | 85                   | O7              |     |  |
| 83      | 86                   | O8              |     |  |
| 84      | 87                   | $\overline{CE}$ | O   | ROM chip enable pin<br>Outputs "H" during standby.       |
| 85      | 88                   | A10             | O   | Address output pin                                       |
| 86      | 89                   | $\overline{OE}$ | O   | ROM output enable pin<br>Outputs "L" at all times.       |
| 87      | 91                   | A11             | O   | Address output pins                                      |
| 88      | 92                   | A9              |     |  |
| 89      | 93                   | A8              |     |  |
| 90      | 94                   | A13             |     |  |
| 91      | 95                   | A14             | O   |  |
| 92      | 96                   | V <sub>CC</sub> | O   | EPROM power supply pin                                   |
| —       | 65<br>76<br>81<br>90 | N.C.            | —   | Internally connected pins<br>Be sure to leave them open. |

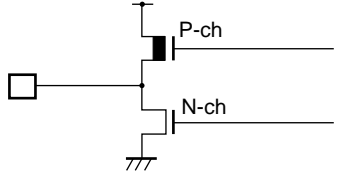
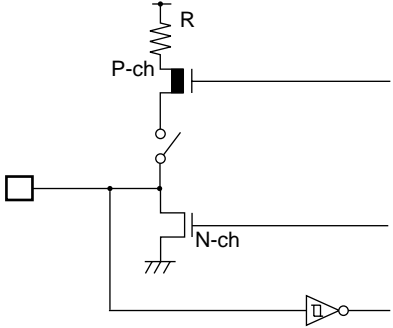
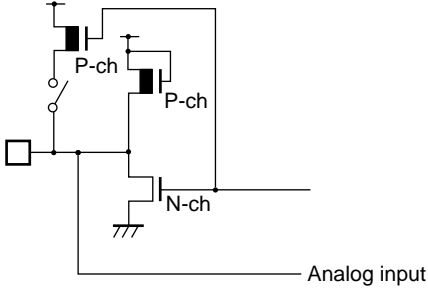
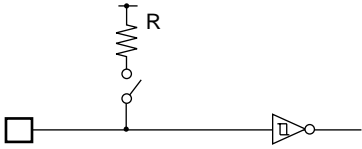
## ■ I/O CIRCUIT TYPE

| Type | Circuit   | Remarks   |
|------|---|---|
| A    |  <p>Standby control signal</p> | <ul style="list-style-type: none"> <li>At an oscillation feedback resistor of approximately 1 MΩ/5.0 V</li> </ul>                             |
| B    |                                |   |
| C    |                               | <ul style="list-style-type: none"> <li>At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V</li> <li>Hysteresis input</li> </ul> |
| D    |                              | <ul style="list-style-type: none"> <li>CMOS I/O</li> <li>Pull-up resistor optional (MB89601R/603 only)</li> </ul>                             |
| E    |                              | <ul style="list-style-type: none"> <li>CMOS output</li> <li>Hysteresis input</li> <li>Software pull-up resistor optional</li> </ul>           |

(Continued)

# MB89601R Series

(Continued)

| Type | Circuit   | Remarks   |
|------|---|---|
| F    |    | <ul style="list-style-type: none"> <li>• CMOS output</li> </ul>   |
| G    |    | <ul style="list-style-type: none"> <li>• N-ch open-drain output</li> <li>• Hysteresis input</li> <li>• Pull-up resistor optional (MB89601R/603 only)</li> </ul> |
| H    |  | <ul style="list-style-type: none"> <li>• N-ch open-drain output</li> <li>• Analog input</li> <li>• Pull-up resistor optional</li> </ul>                         |
| I    |  | <ul style="list-style-type: none"> <li>• Hysteresis input</li> <li>• Pull-up resistor optional (MB89601R/603 only)</li> </ul>                                   |

## ■ HANDLING DEVICES

### 1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to input and output pins other than P40 to P47, P60 or if higher than the voltage which shows on section “■ Electrical Characteristics” is applied between  $V_{CC}$  and  $V_{SS}$ .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

### 2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

### 3. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

### 4. Power Supply Voltage Fluctuations

Although  $V_{CC}$  power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that  $V_{CC}$  ripple fluctuations (P-P value) will be less than 10% of the standard  $V_{CC}$  value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

### 5. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

# MB89601R Series

## ■ PROGRAMMING TO THE EPROM ON THE MB89P601

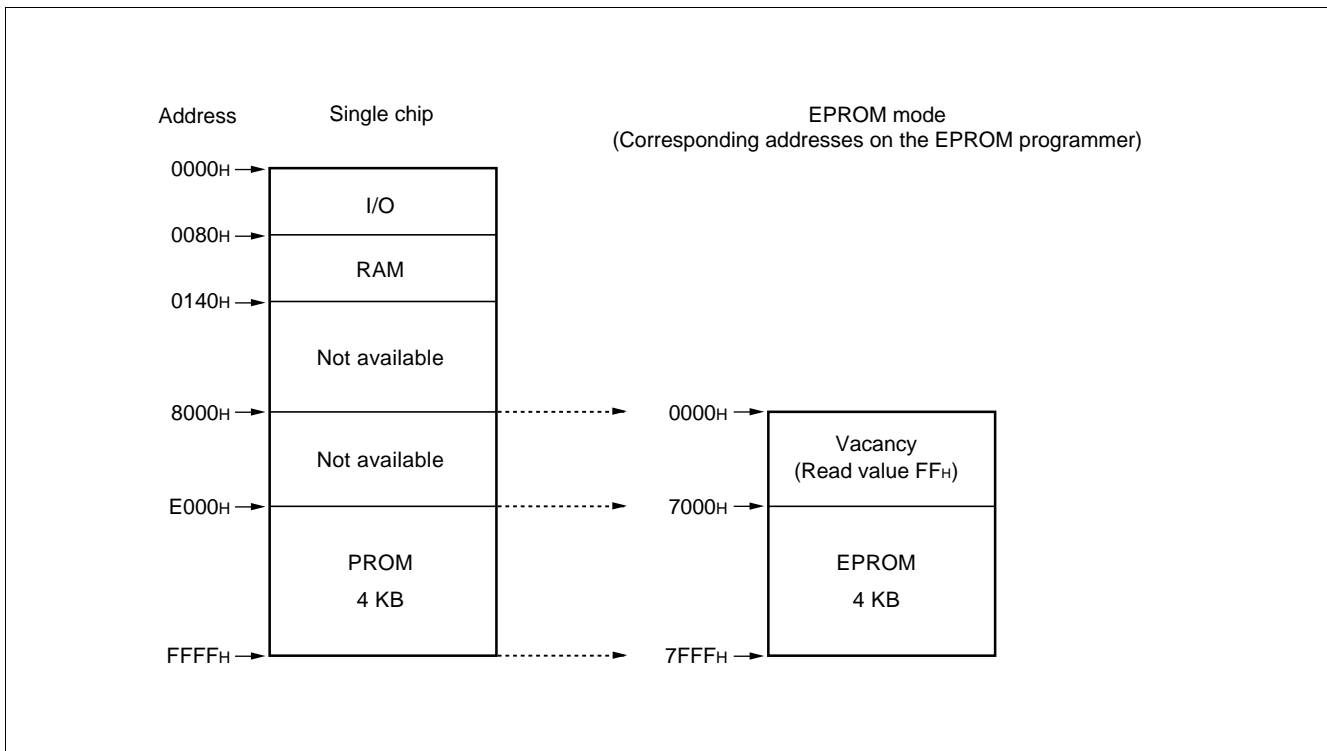
The MB89P601 is an OTPROM version of the MB89601R series.

### 1. Features

- 4-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

### 2. Memory Space

Memory space in each mode such as 4-Kbyte PROM is diagrammed below.



### 3. Programming to the EPROM

In EPROM mode, the MB89P601 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

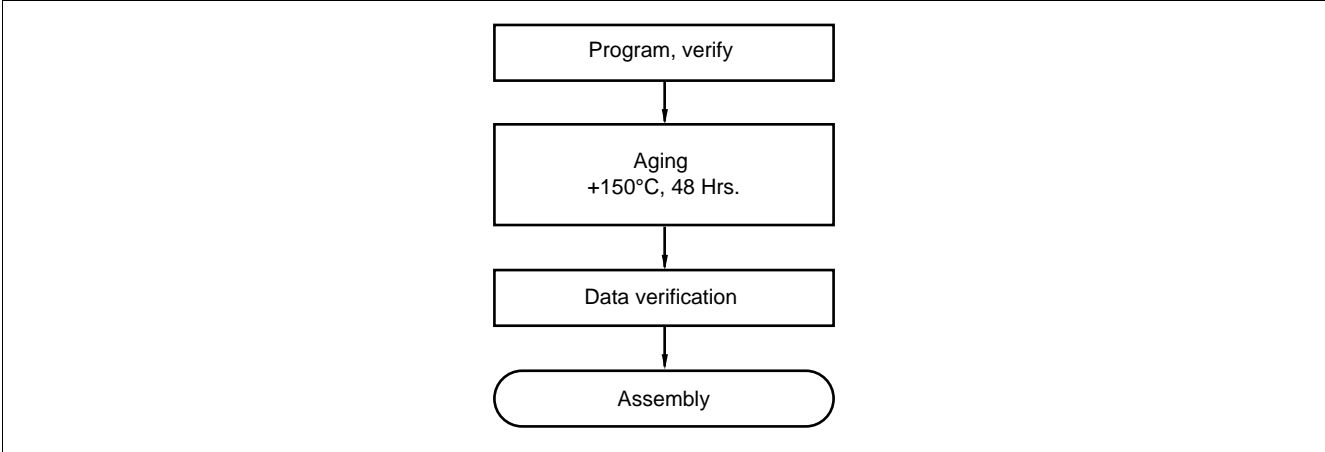
When the operating ROM area for a single chip is 32 Kbytes (8000<sub>H</sub> to FFFF<sub>H</sub>) the PROM can be programmed as follows:

#### • Programming procedure

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 7000<sub>H</sub> to 7FFF<sub>H</sub> (note that addresses E000<sub>H</sub> to FFFF<sub>H</sub> while operating as a single chip assign to 7000<sub>H</sub> to 7FFF<sub>H</sub> in EPROM mode).
- (3) Program to 0000<sub>H</sub> to 7FFF<sub>H</sub> with the EPROM programmer.

## 4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



## 5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

## 6. EPROM Programmer Socket Adapter

| Package     | Compatible socket adapter |
|-------------|---------------------------|
| FPT-48P-M05 | ROM-48QF-28DP-8L          |

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760  
Note: Connect the adapter jumper pin to V<sub>ss</sub> when using.

# MB89601R Series

## ■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

### 1. EPROM for Use

MBM27C256A-20TV, MBM27C256A-20CZ

### 2. Programming Socket Adapter

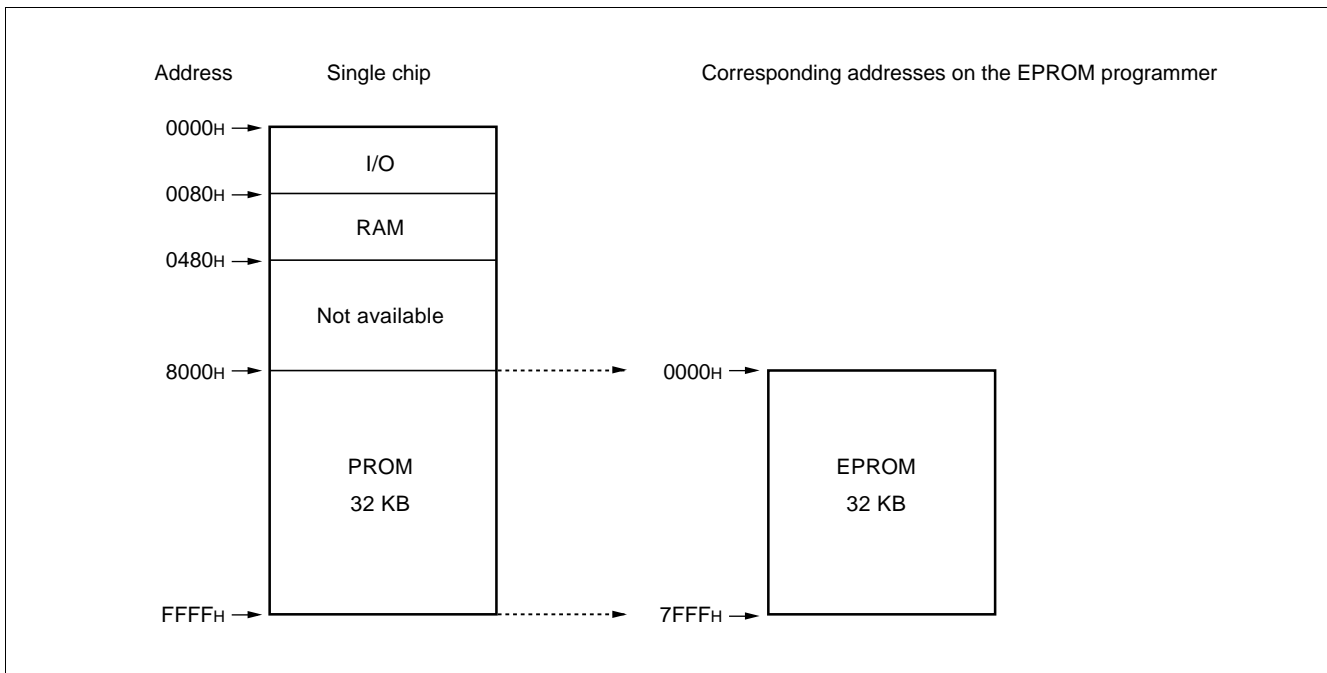
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

| Package           | Adapter socket part number |
|-------------------|----------------------------|
| LCC-32(Rectangle) | ROM-32LC-28DP-YG           |

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

### 3. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, is diagrammed below.

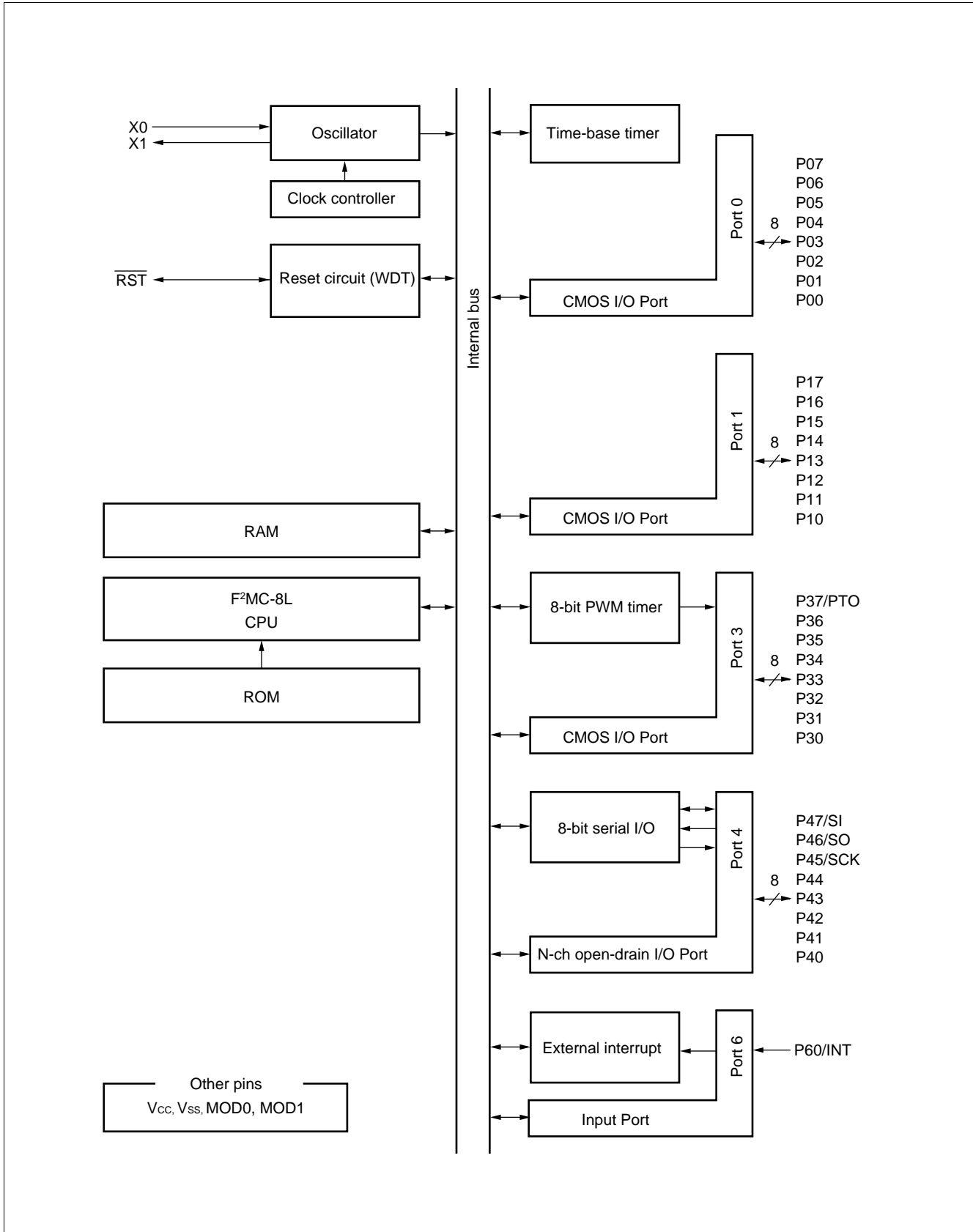


### 4. Programming to the EPROM

- (1) Set the EPROM programmer to the MBM27C256A.
- (2) Load program data into the EPROM programmer at 0006H to 7FFFH.
- (3) Program to 0000H to 7FFFH with the EPROM programmer.



## ■ BLOCK DIAGRAM

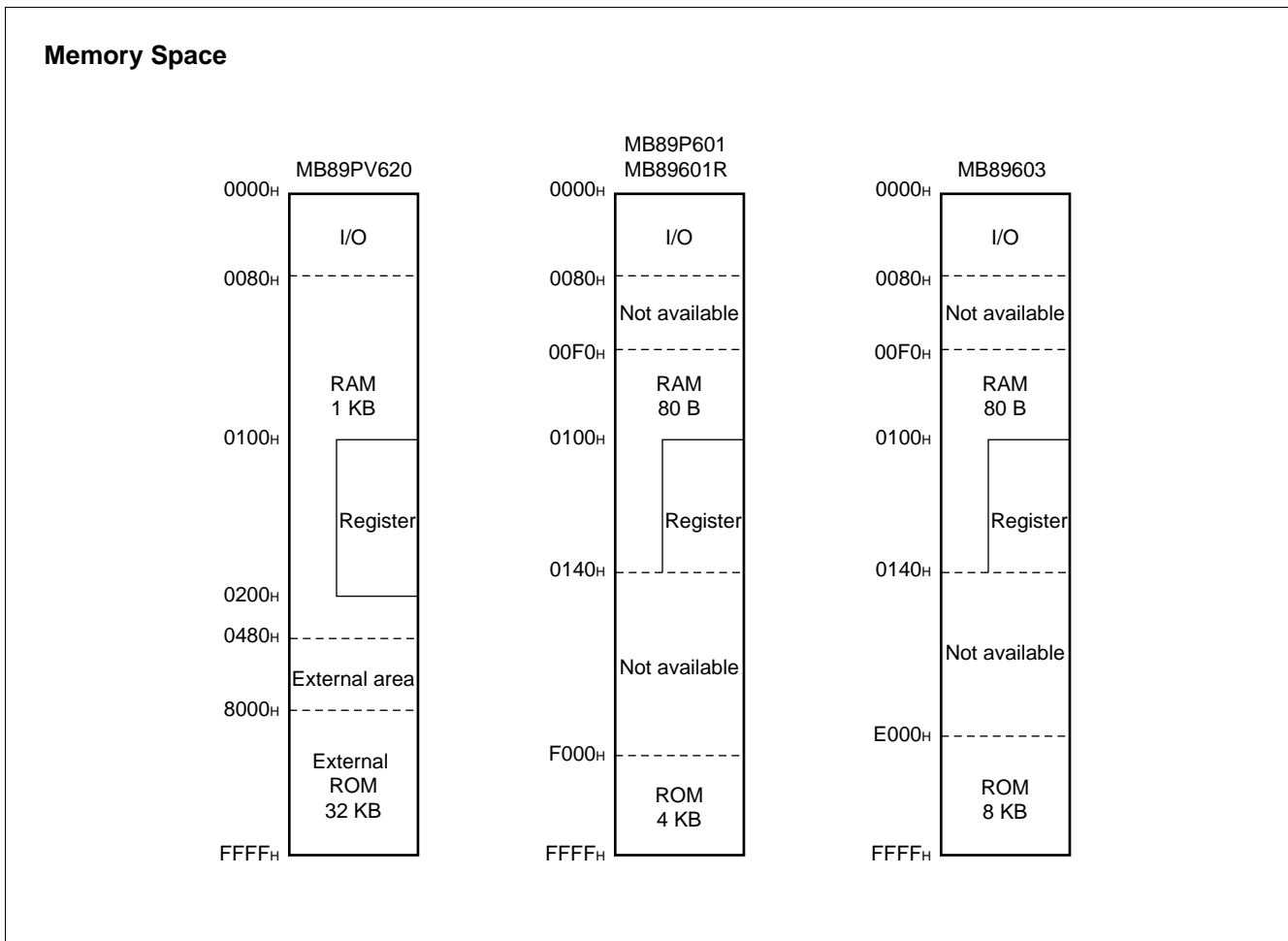


# MB89601R Series

## ■ CPU CORE

### 1. Memory Space

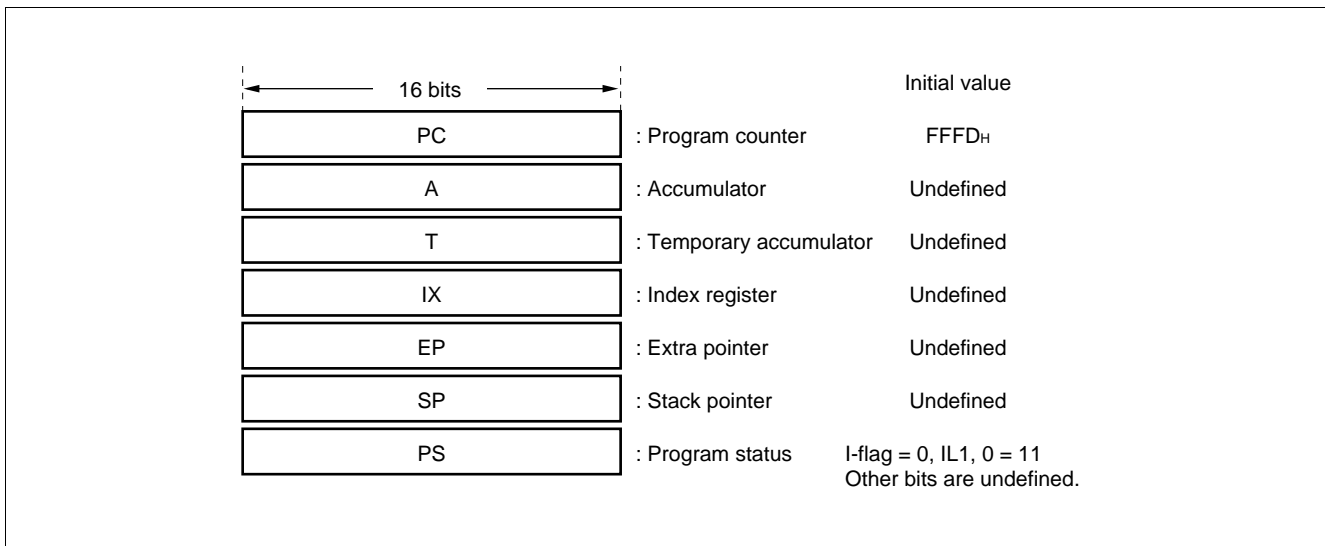
The microcontrollers of the MB89601R series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89601R series is structured as illustrated below.



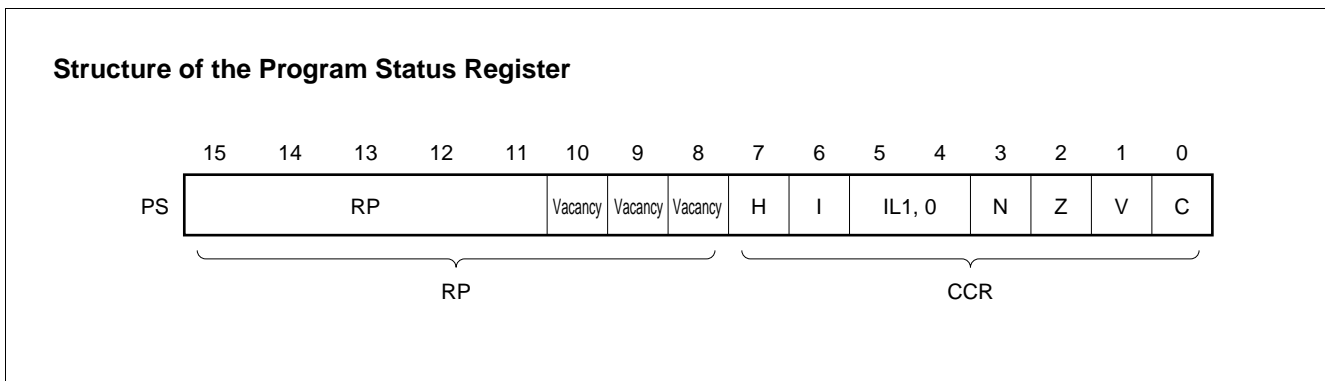
## 2. Registers

The F<sup>2</sup>MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

- Program counter (PC): A 16-bit register for indicating instruction storage positions
- Accumulator (A): A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Temporary accumulator (T): A 16-bit register which performs arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.
- Index register (IX): A 16-bit register for index modification
- Extra pointer (EP): A 16-bit pointer for indicating a memory address
- Stack pointer (SP): A 16-bit register for indicating a stack area
- Program status (PS): A 16-bit register for storing a register pointer, a condition code

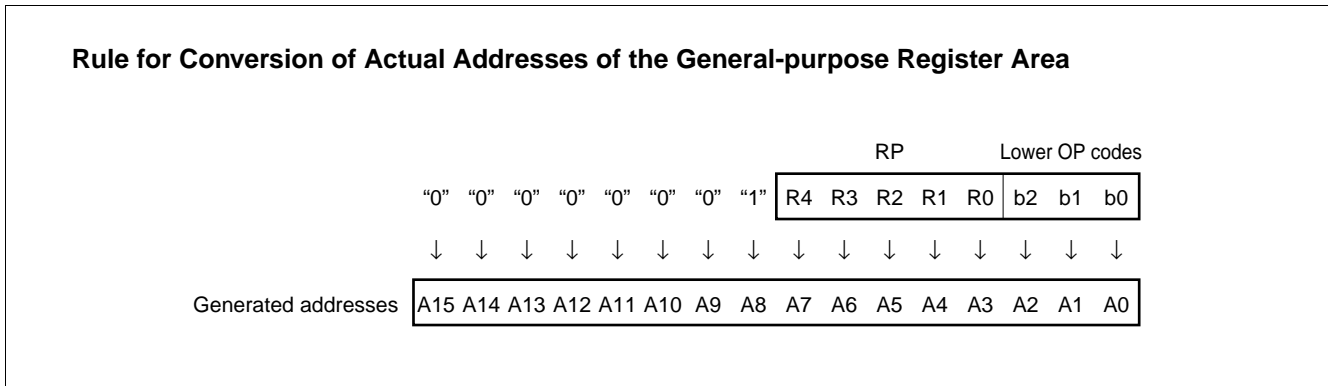


The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)



# MB89601R Series

The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

- H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.
- I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.
- IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

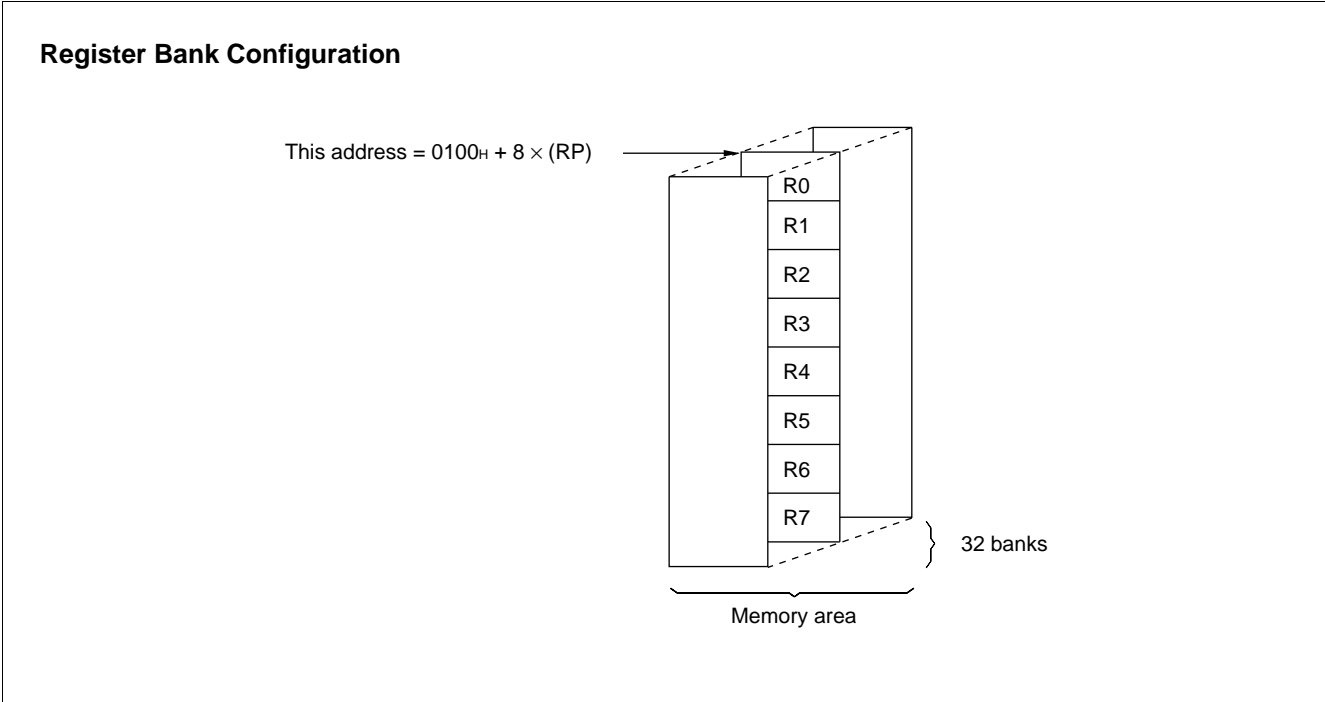
| IL1 | ILO | Interrupt level | High-low                             |
|-----|-----|-----------------|--------------------------------------|
| 0   | 0   | 1               | High<br>↑<br>↓<br>Low = no interrupt |
| 0   | 1   |                 |                                      |
| 1   | 0   | 2               |                                      |
| 1   | 1   | 3               |                                      |

- N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.
- Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.
- V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.
- C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to 32 banks can be used on the architecture, but only 8 banks can be used on the MB89601R series due to the restricted internal RAM size. The bank currently in use is indicated by the register bank pointer (RP).



Note: For software development, take care that the usable register banks on the MB89601R/603 are different from that on the MB89PV620. On the MB89PV620, up to 32 banks can be used.

# MB89601R Series

## ■ I/O MAP

| Address | Read/write | Register name | Register description             |
|---------|------------|---------------|----------------------------------|
| 00H     | (R/W)      | PDR0          | Port 0 data register             |
| 01H     | (W)        | DDR0          | Port 0 data direction register   |
| 02H     | (R/W)      | PDR1          | Port 1 data register             |
| 03H     | (W)        | DDR1          | Port 1 data direction register   |
| 04H     | (R/W)      | SPCR          | Port 3 pull-up register          |
| 05H     |            |               | Vacancy                          |
| 06H     |            |               | Vacancy                          |
| 07H     |            |               | Vacancy                          |
| 08H     | (R/W)      | STBC          | Standby control register         |
| 09H     | (R/W)      | WDTC          | Watchdog timer control register  |
| 0AH     | (R/W)      | TBTC          | Clock interrupt control register |
| 0BH     |            |               | Vacancy                          |
| 0CH     | (R/W)      | PDR3          | Port 3 data register             |
| 0DH     | (W)        | DDR3          | Port 3 data direction register   |
| 0EH     | (R/W)      | PDR4          | Port 4 data register             |
| 0FH     |            |               | Vacancy                          |
| 10H     |            |               | Vacancy                          |
| 11H     | (R)        | PDR6          | Port 6 data register             |
| 12H     | (R/W)      | CNTR          | PWM control register             |
| 13H     | (W)        | COMR          | PWM compare register             |
| 14H     |            |               | Vacancy                          |
| 15H     |            |               | Vacancy                          |
| 16H     |            |               | Vacancy                          |
| 17H     |            |               | Vacancy                          |
| 18H     |            |               | Vacancy                          |
| 19H     |            |               | Vacancy                          |
| 1AH     |            |               | Vacancy                          |
| 1BH     |            |               | Vacancy                          |
| 1CH     |            |               | Vacancy                          |
| 1DH     |            |               | Vacancy                          |
| 1EH     | (R/W)      | SMR           | Serial mode register             |
| 1FH     | (R/W)      | SDR           | Serial data register             |

(Continued)

(Continued)

| Address                            | Read/write | Register name | Register description                |
|------------------------------------|------------|---------------|-------------------------------------|
| 20 <sub>H</sub>                    |            |               | Vacancy                             |
| 21 <sub>H</sub>                    |            |               | Vacancy                             |
| 22 <sub>H</sub>                    |            |               | Vacancy                             |
| 23 <sub>H</sub>                    |            |               | Vacancy                             |
| 24 <sub>H</sub>                    | (R/W)      | EIC           | External interrupt control register |
| 25 <sub>H</sub> to 7B <sub>H</sub> |            |               | Vacancy                             |
| 7C <sub>H</sub>                    | (W)        | ILR1          | Interrupt level setting register 1  |
| 7D <sub>H</sub>                    | (W)        | ILR2          | Interrupt level setting register 2  |
| 7E <sub>H</sub>                    | (W)        | ILR3          | Interrupt level setting register 3  |
| 7F <sub>H</sub>                    |            |               | Vacancy                             |

Note: Do not use vacancies.

# MB89601R Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

( $V_{SS} = 0.0\text{ V}$ )

| Parameter                              | Symbol            | Value          |                | Unit | Remarks   |
|--|-------------------|----------------|----------------|------|---|
|  |                   | Min.           | Max.           |      |   |
| Power supply voltage                   | $V_{CC}$          | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V    |   |
| Input voltage                          | $V_{I1}$          | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V    | Except P40 to P47, P60                                    |
|  | $V_{I2}$          | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V    | P40 to P47, P60   |
| Output voltage                         | $V_{O1}$          | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V    | Except P40 to P47   |
|  | $V_{O2}$          | $V_{SS} - 0.3$ | $V_{SS} + 7.0$ | V    | P40 to P47  |
| “L” level maximum output current       | $I_{OL}$          | —              | 20             | mA   |   |
| “L” level average output current       | $I_{OLAV}$        | —              | 4              | mA   | Average value (operating current $\times$ operating rate) |
| “L” level total average output current | $\Sigma I_{OLAV}$ | —              | 40             | mA   | Average value (operating current $\times$ operating rate) |
| “L” level total maximum output current | $\Sigma I_{OL}$   | —              | 100            | mA   |   |
| “H” level maximum output current       | $I_{OH}$          | —              | -20            | mA   |   |
| “H” level average output current       | $I_{OHAV}$        | —              | -4             | mA   | Average value (operating current $\times$ operating rate) |
| “H” level total average output current | $\Sigma I_{OHAV}$ | —              | -20            | mA   | Average value (operating current $\times$ operating rate) |
| “H” level total maximum output current | $\Sigma I_{OH}$   | —              | -50            | mA   |   |
| Power consumption                      | $P_D$             | —              | 300            | mW   |   |
| Operating temperature                  | $T_A$             | -40            | +85            | °C   |   |
| Storage temperature                    | $T_{stg}$         | -55            | +150           | °C   |   |

Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## 2. Recommended Operating Conditions

(V<sub>SS</sub> = 0.0 V)

| Parameter             | Symbol          | Value |      | Unit | Remarks   |
|-----------------------|-----------------|-------|------|------|---|
|                       |                 | Min.  | Max. |      |   |
| Power supply voltage  | V <sub>CC</sub> | 2.2*  | 6.0  | V    | Normal operation assurance range*<br>MB89601R/603 |
|                       |                 | 2.7*  | 6.0  | V    | Normal operation assurance range*<br>MB89P601     |
|                       |                 | 1.5   | 6.0  | V    | Retains the RAM state in stop mode                |
| Operating temperature | T <sub>A</sub>  | -40   | +85  | °C   |   |

\* : These values vary with the operating frequency. See Figure 1.

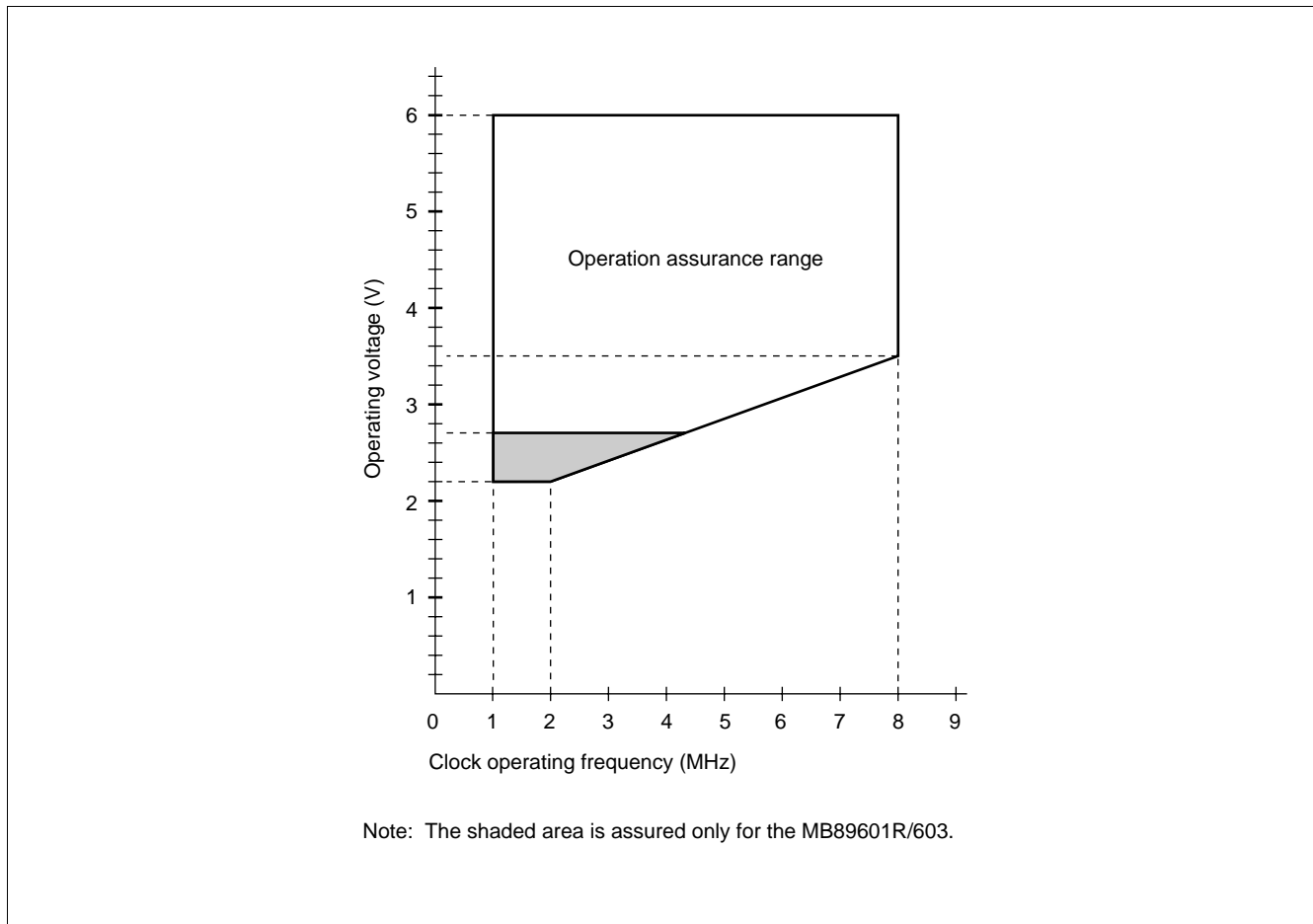


Figure 1 Operating Voltage vs. Clock Operating Frequency

# MB89601R Series

## 3. DC Characteristics

( $V_{CC} = +5.0\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter  | Symbol     | Pin  | Condition                     | Value          |      |                | Unit          | Remarks                  |
|--|------------|--|-------------------------------|----------------|------|----------------|---------------|--------------------------|
|  |            |  |                               | Min.           | Typ. | Max.           |               |                          |
| “H” level input voltage                                | $V_{IH}$   | P00 to P07,<br>P10 to P17  | —                             | $0.7 V_{CC}$   | —    | $V_{CC} + 0.3$ | V             |                          |
|  | $V_{IHS1}$ | P30 to P37,<br>MOD0, MOD1,<br>RST  | —                             | $0.8 V_{CC}$   | —    | $V_{CC} + 0.3$ | V             |                          |
|  | $V_{IHS2}$ | P40 to P47,<br>P60   | —                             | $0.8 V_{CC}$   | —    | $V_{SS} + 6.0$ | V             |                          |
| “L” level input voltage                                | $V_{IL}$   | P00 to P07,<br>P10 to P17  | —                             | $V_{SS} - 0.3$ | —    | $0.3 V_{CC}$   | V             |                          |
|  | $V_{ILS}$  | P30 to P37,<br>MOD0, MOD1,<br>RST,<br>P40 to P47,<br>P60                       | —                             | $V_{SS} - 0.3$ | —    | $0.2 V_{CC}$   | V             |                          |
| Open-drain output pin application voltage              | $V_D$      | P40 to P47   | —                             | $V_{SS} - 0.3$ | —    | $V_{SS} + 6.0$ | V             |                          |
| “H” level output voltage                               | $V_{OH}$   | P00 to P07,<br>P10 to P17,<br>P30 to P37                                       | $I_{OH} = -2.0\text{ mA}$     | 4.0            | —    | —              | V             |                          |
| “L” level output voltage                               | $V_{OL}$   | P00 to P07,<br>P10 to P17,<br>P30 to P37,<br>P40 to P47                        | $I_{OL} = +1.8\text{ mA}$     | —              | —    | 0.4            | V             |                          |
|  | $V_{OL2}$  | RST  | $I_{OL} = +4.0\text{ mA}$     | —              | —    | 0.4            | V             |                          |
| Input leakage current<br>(Hi-z output leakage current) | $I_{LI1}$  | P00 to P07,<br>P10 to P17,<br>P30 to P37,<br>P40 to P47,<br>P60,<br>MOD0, MOD1 | $0.0\text{ V} < V_i < V_{CC}$ | —              | —    | $\pm 5$        | $\mu\text{A}$ | Without pull-up resistor |
| Pull-up resistance                                     | $R_{PULL}$ | P00 to P07,<br>P10 to P17,<br>P30 to P37,<br>P40 to P47,<br>P60, RST           | $V_i = 0.0\text{ V}$          | 25             | 50   | 100            | k $\Omega$    |                          |

(Continued)

# MB89601R Series

(Continued)

( $V_{CC} = +5.0\text{ V}$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter             | Symbol    | Pin                              | Condition                                     | Value |      |      | Unit          | Remarks        |
|-----------------------|-----------|----------------------------------|---|-------|------|------|---------------|----------------|
|                       |           |                                  |   | Min.  | Typ. | Max. |               |                |
| Power supply current* | $I_{CC}$  | $V_{CC}$                         | $F_C = 8\text{ MHz}$<br>Normal operating mode | —     | 9    | 15   | mA            |                |
|                       |           |                                  | $F_C = 8\text{ MHz}$                          | —     | 10   | 18   | mA            | MB89P601       |
|                       | $I_{CCS}$ |                                  | $F_C = 8\text{ MHz}$<br>Sleep mode            | —     | 3    | 4    | mA            | External clock |
|                       | $I_{CCH}$ |                                  | $T_A = +25^\circ\text{C}$<br>Stop mode        | —     | —    | 10   | $\mu\text{A}$ |                |
| Input capacitance     | $C_{IN}$  | Other than $V_{CC}$ and $V_{SS}$ | $f = 1\text{ MHz}$                            | —     | 10   | —    | pF            |                |

\* : The power supply current is measured at the external clock.

Note: A pull-up resistor for P00 to P07, P10 to P17, P40 to P47 and P60 is selectable on MB89601R/603 only.

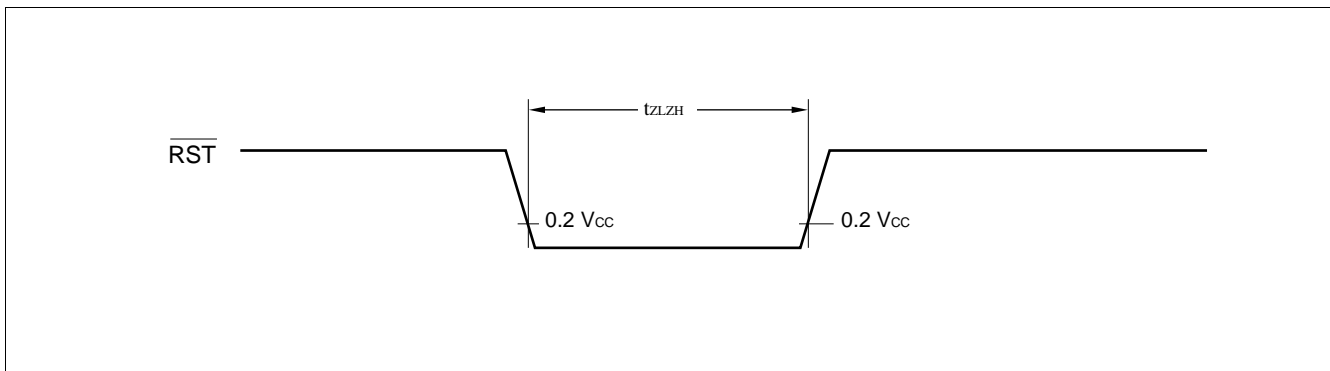
## 4. AC Characteristics

### (1) Reset Timing

( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                               | Symbol     | Condition | Value         |      | Unit | Remarks |
|---|------------|-----------|---------------|------|------|---------|
|   |            |           | Min.          | Max. |      |         |
| $\overline{\text{RST}}$ "L" pulse width | $t_{ZLZH}$ | —         | 16 $t_{XCYL}$ | —    | ns   |         |

Note:  $t_{XCYL}$  is the oscillation cycle ( $1/F_C$ ) to input to the X0 pin.



# MB89601R Series

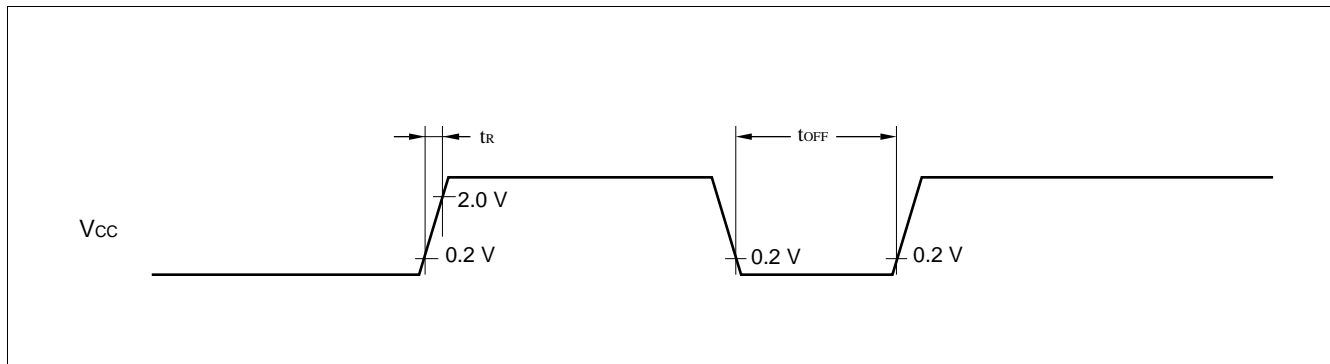
## (2) Power-on Reset

( $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                 | Symbol    | Condition | Value |      | Unit | Remarks                      |
|---------------------------|-----------|-----------|-------|------|------|------------------------------|
|                           |           |           | Min.  | Max. |      |                              |
| Power supply rising time  | $t_R$     | —         | —     | 50   | ms   | Power-on reset function only |
| Power supply cut-off time | $t_{OFF}$ |           | 1     | —    | ms   | Due to repeated operations   |

Note: Abrupt change in power supply voltage may cause a power-on reset.

If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

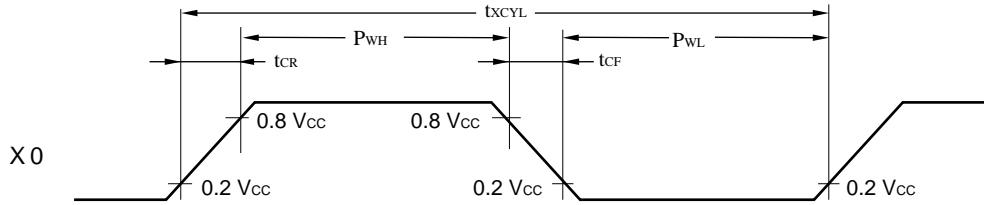


## (3) Clock Timing

( $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

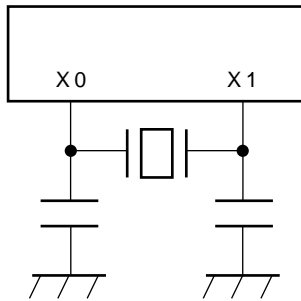
| Parameter                       | Symbol               | Pin    | Condition | Value |      | Unit | Remarks        |
|---------------------------------|----------------------|--------|-----------|-------|------|------|----------------|
|                                 |                      |        |           | Min.  | Max. |      |                |
| Clock frequency                 | $F_C$                | X0, X1 | —         | 1     | 8    | MHz  |                |
| Clock cycle time                | $t_{XYCL}$           | X0, X1 | —         | 125   | —    | ns   |                |
| Input clock pulse width         | $P_{WH}$<br>$P_{WL}$ | X0     | —         | 20    | —    | ns   | External clock |
| Input clock rising/falling time | $t_{CR}$<br>$t_{CF}$ | X0     | —         | —     | 10   | ns   | External clock |

## X0 and X1 Timing and Conditions

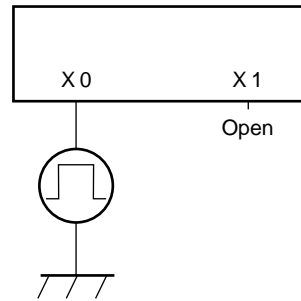


## Clock Conditions

When a crystal or ceramic resonator is used



When an external clock is used



## (4) Instruction Cycle

| Parameter                                  | Symbol            | Value (typical)  | Unit | Remarks   |
|--|-------------------|------------------|------|---|
| Instruction cycle (minimum execution time) | t <sub>inst</sub> | 4/F <sub>C</sub> | μs   | t <sub>inst</sub> = 0.5 μs when operating at F <sub>C</sub> = 8 MHz |

## (5) Serial I/O Timing

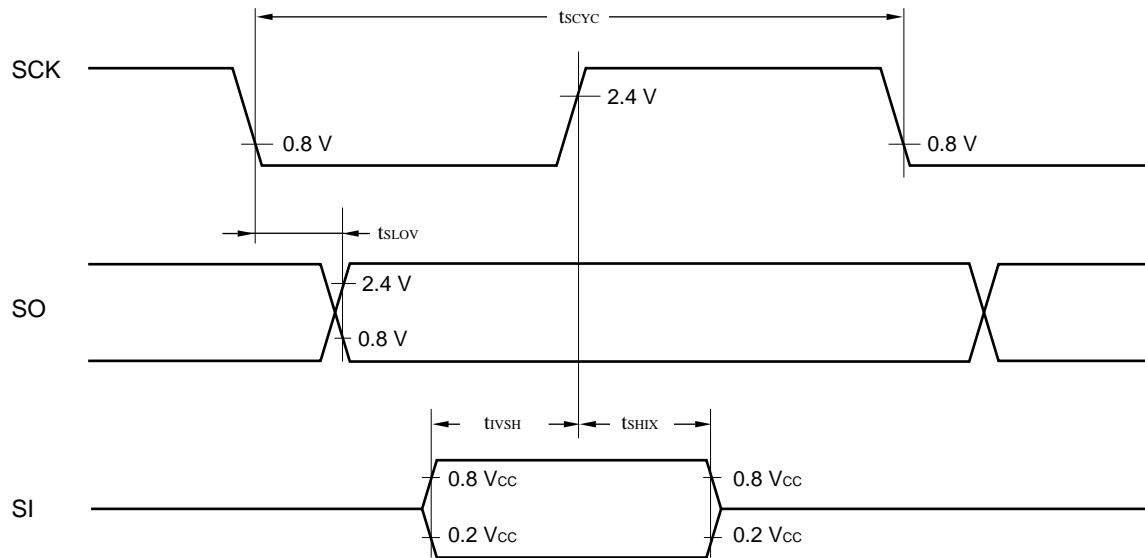
(V<sub>CC</sub> = +5.0 V ± 10%, V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40°C to +85°C)

| Parameter                    | Symbol            | Pin     | Condition                 | Value                   |      | Unit | Remarks |
|------------------------------|-------------------|---------|---------------------------|-------------------------|------|------|---------|
|                              |                   |         |                           | Min.                    | Max. |      |         |
| Serial clock cycle time      | t <sub>SCYC</sub> | SCK     | Internal shift clock mode | 2 t <sub>inst</sub> *   | —    | μs   |         |
| SCK ↓ → SO time              | t <sub>SLOV</sub> | SCK, SO |                           | -200                    | 200  | ns   |         |
| Valid SI → SCK ↑             | t <sub>IVSH</sub> | SI, SCK |                           | 1/2 t <sub>inst</sub> * | —    | μs   |         |
| SCK ↑ → valid SI hold time   | t <sub>SHIX</sub> | SCK, SI |                           | 1/2 t <sub>inst</sub> * | —    | μs   |         |
| Serial clock "H" pulse width | t <sub>SHSL</sub> | SCK     | External shift clock mode | 1 t <sub>inst</sub> *   | —    | μs   |         |
| Serial clock "L" pulse width | t <sub>LSLH</sub> | SCK     |                           | 1 t <sub>inst</sub> *   | —    | μs   |         |
| SCK ↓ → SO time              | t <sub>SLOV</sub> | SCK, SO |                           | 0                       | 200  | ns   |         |
| Valid SI → SCK ↑             | t <sub>IVSH</sub> | SI, SCK |                           | 1/2 t <sub>inst</sub> * | —    | μs   |         |
| SCK ↑ → valid SI hold time   | t <sub>SHIX</sub> | SCK, SI | 1/2 t <sub>inst</sub> *   | —                       | μs   |      |         |

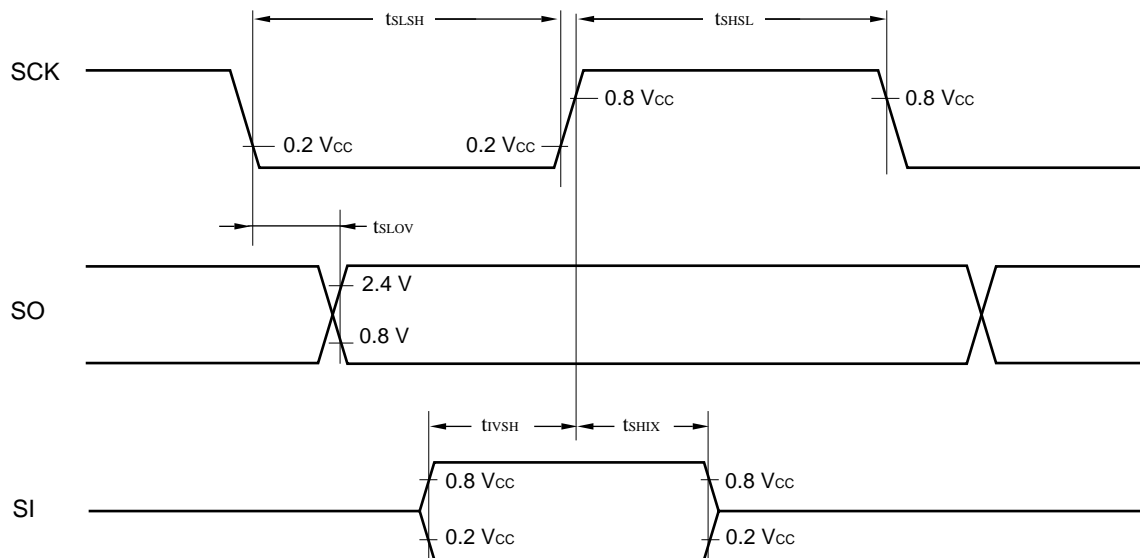
\* : For information on t<sub>inst</sub>, see "(4) Instruction Cycle."

# MB89601R Series

## Internal Shift Clock Mode



## External Shift Clock Mode

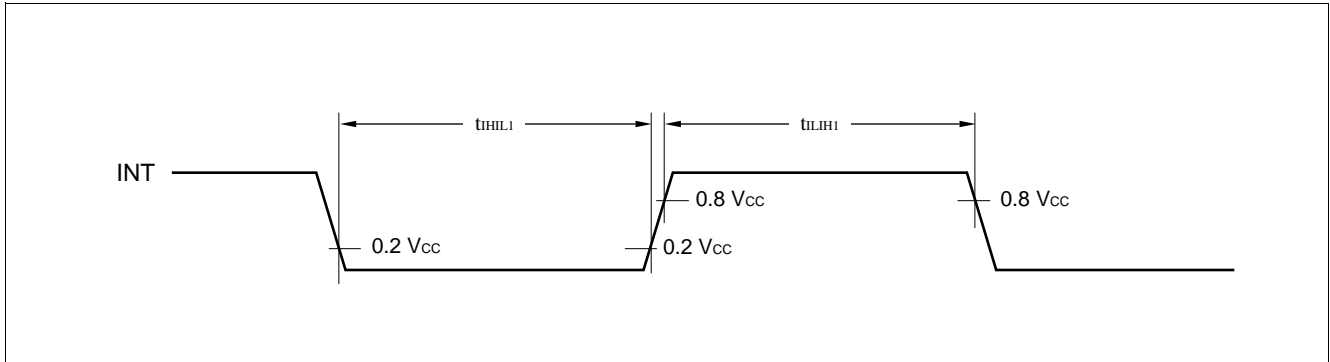


## (6) Peripheral Input Timing

( $V_{CC} = +5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Parameter                          | Symbol    | Pin | Condition | Value          |      | Unit          | Remarks |
|------------------------------------|-----------|-----|-----------|----------------|------|---------------|---------|
|                                    |           |     |           | Min.           | Max. |               |         |
| Peripheral input "H" pulse width 1 | $t_{LH1}$ | INT | —         | $2 t_{inst}^*$ | —    | $\mu\text{s}$ |         |
| Peripheral input "L" pulse width 1 | $t_{HL1}$ |     |           | $2 t_{inst}^*$ | —    | $\mu\text{s}$ |         |

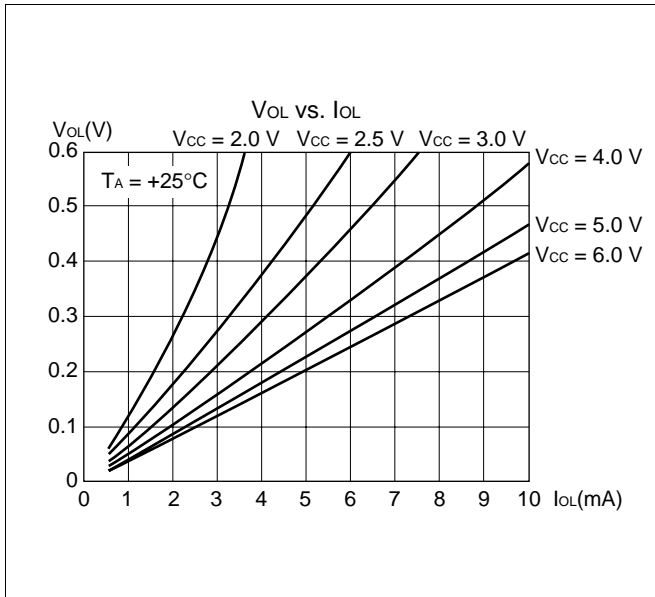
\* : For information on  $t_{inst}$ , see "(4) Instruction Cycle."



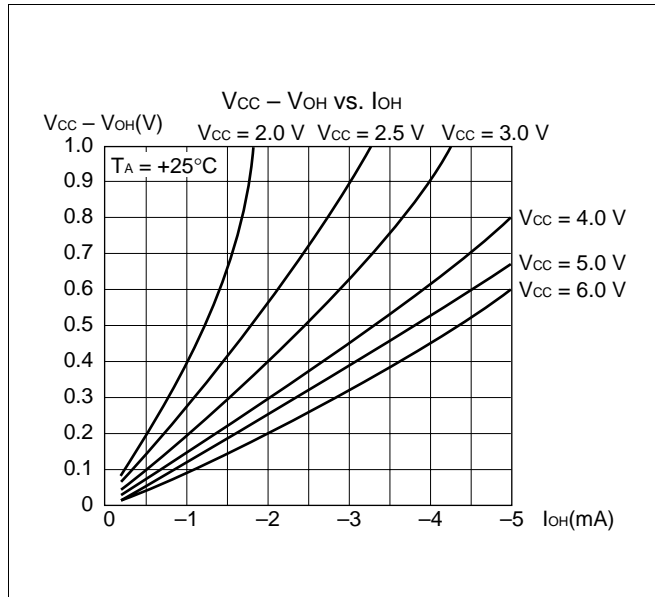
# MB89601R Series

## EXAMPLE CHARACTERISTICS

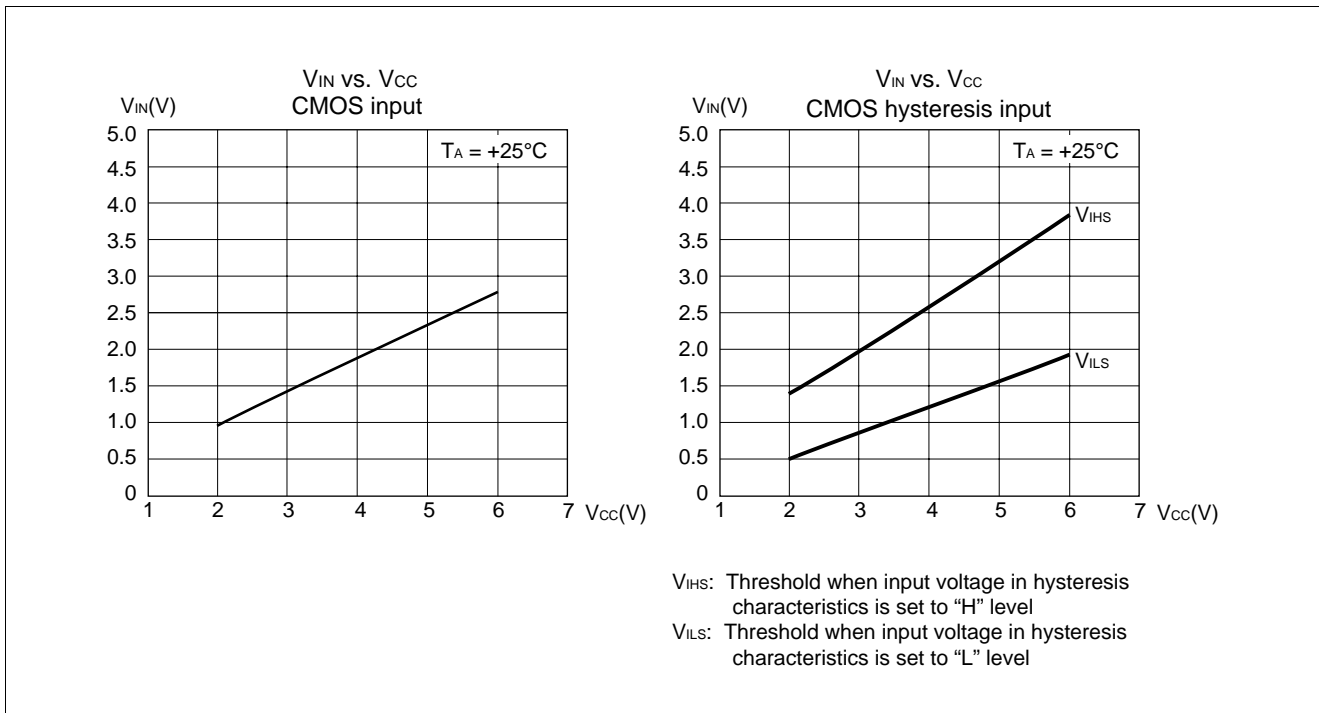
(1) "L" Level Output Voltage



(2) "H" Level Output Voltage

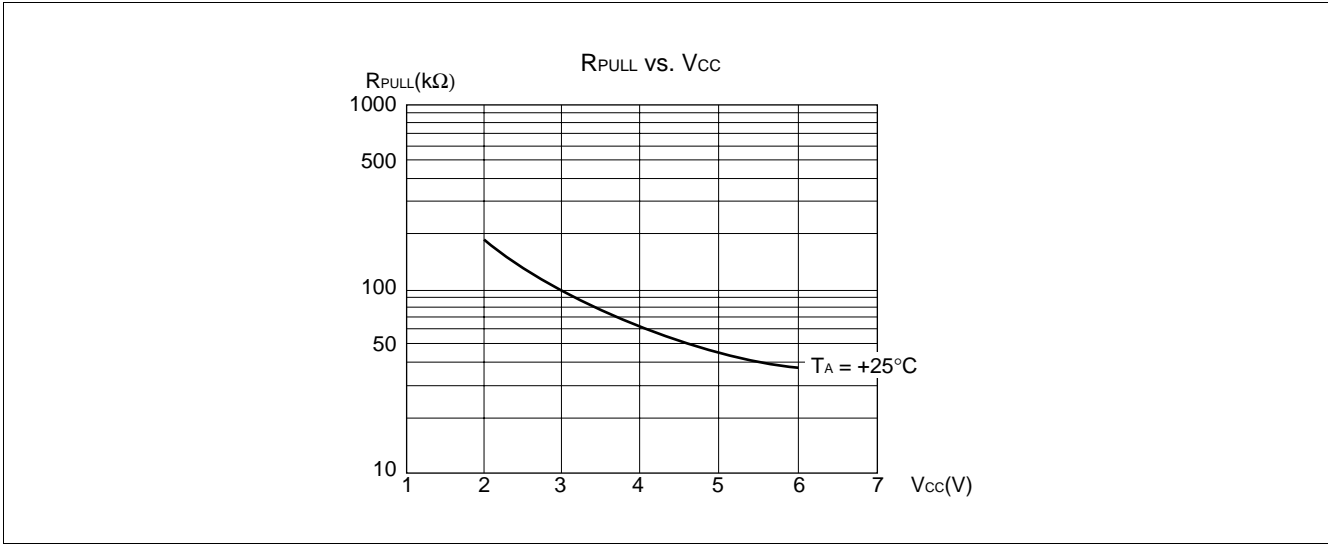


(3) "H" Level Input Voltage/"L" Level Input Voltage





## (4) Pull-up Resistance



# MB89601R Series

## ■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

**Table 1 Instruction Symbols**

| Symbol | Meaning   |
|--------|---|
| dir    | Direct address (8 bits)   |
| off    | Offset (8 bits)   |
| ext    | Extended address (16 bits)  |
| #vct   | Vector table number (3 bits)  |
| #d8    | Immediate data (8 bits)   |
| #d16   | Immediate data (16 bits)  |
| dir: b | Bit direct address (8:3 bits)   |
| rel    | Branch relative address (8 bits)  |
| @      | Register indirect (Example: @A, @IX, @EP)   |
| A      | Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)   |
| AH     | Upper 8 bits of accumulator A (8 bits)  |
| AL     | Lower 8 bits of accumulator A (8 bits)  |
| T      | Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)   |
| TH     | Upper 8 bits of temporary accumulator T (8 bits)  |
| TL     | Lower 8 bits of temporary accumulator T (8 bits)  |
| IX     | Index register IX (16 bits)   |
| EP     | Extra pointer EP (16 bits)  |
| PC     | Program counter PC (16 bits)  |
| SP     | Stack pointer SP (16 bits)  |
| PS     | Program status PS (16 bits)   |
| dr     | Accumulator A or index register IX (16 bits)  |
| CCR    | Condition code register CCR (8 bits)  |
| RP     | Register bank pointer RP (5 bits)   |
| Ri     | General-purpose register Ri (8 bits, i = 0 to 7)  |
| ×      | Indicates that the very × is the immediate data.<br>(Whether its length is 8 or 16 bits is determined by the instruction in use.)                       |
| (×)    | Indicates that the contents of × is the target of accessing.<br>(Whether its length is 8 or 16 bits is determined by the instruction in use.)           |
| ((×))  | The address indicated by the contents of × is the target of accessing.<br>(Whether its length is 8 or 16 bits is determined by the instruction in use.) |

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: The number of instructions

#: The number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- “-” indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH prior to the instruction executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

**Table 2 Transfer Instructions (48 instructions)**

| Mnemonic         | ~ | # | Operation                                     | TL | TH | AH | NZVC  | OP code  |
|------------------|---|---|---|----|----|----|-------|----------|
| MOV dir,A        | 3 | 2 | (dir) ← (A)                                   | -  | -  | -  | ----- | 45       |
| MOV @IX +off,A   | 4 | 2 | ((IX) +off) ← (A)                             | -  | -  | -  | ----- | 46       |
| MOV ext,A        | 4 | 3 | (ext) ← (A)                                   | -  | -  | -  | ----- | 61       |
| MOV @EP,A        | 3 | 1 | ((EP)) ← (A)                                  | -  | -  | -  | ----- | 47       |
| MOV Ri,A         | 3 | 1 | (Ri) ← (A)                                    | -  | -  | -  | ----- | 48 to 4F |
| MOV A,#d8        | 2 | 2 | (A) ← d8                                      | AL | -  | -  | ++--  | 04       |
| MOV A,dir        | 3 | 2 | (A) ← (dir)                                   | AL | -  | -  | ++--  | 05       |
| MOV A,@IX +off   | 4 | 2 | (A) ← ((IX) +off)                             | AL | -  | -  | ++--  | 06       |
| MOV A,ext        | 4 | 3 | (A) ← (ext)                                   | AL | -  | -  | ++--  | 60       |
| MOV A,@A         | 3 | 1 | (A) ← ((A))                                   | AL | -  | -  | ++--  | 92       |
| MOV A,@EP        | 3 | 1 | (A) ← ((EP))                                  | AL | -  | -  | ++--  | 07       |
| MOV A,Ri         | 3 | 1 | (A) ← (Ri)                                    | AL | -  | -  | ++--  | 08 to 0F |
| MOV dir,#d8      | 4 | 3 | (dir) ← d8                                    | -  | -  | -  | ----- | 85       |
| MOV @IX +off,#d8 | 5 | 3 | ((IX) +off) ← d8                              | -  | -  | -  | ----- | 86       |
| MOV @EP,#d8      | 4 | 2 | ((EP)) ← d8                                   | -  | -  | -  | ----- | 87       |
| MOV Ri,#d8       | 4 | 2 | (Ri) ← d8                                     | -  | -  | -  | ----- | 88 to 8F |
| MOVW dir,A       | 4 | 2 | (dir) ← (AH),(dir + 1) ← (AL)                 | -  | -  | -  | ----- | D5       |
| MOVW @IX +off,A  | 5 | 2 | ((IX) +off) ← (AH),<br>((IX) +off + 1) ← (AL) | -  | -  | -  | ----- | D6       |
| MOVW ext,A       | 5 | 3 | (ext) ← (AH), (ext + 1) ← (AL)                | -  | -  | -  | ----- | D4       |
| MOVW @EP,A       | 4 | 1 | ((EP)) ← (AH),(EP + 1) ← (AL)                 | -  | -  | -  | ----- | D7       |
| MOVW EP,A        | 2 | 1 | (EP) ← (A)                                    | -  | -  | -  | ----- | E3       |
| MOVW A,#d16      | 3 | 3 | (A) ← d16                                     | AL | AH | dH | ++--  | E4       |
| MOVW A,dir       | 4 | 2 | (AH) ← (dir), (AL) ← (dir + 1)                | AL | AH | dH | ++--  | C5       |
| MOVW A,@IX +off  | 5 | 2 | (AH) ← ((IX) +off),<br>(AL) ← ((IX) +off + 1) | AL | AH | dH | ++--  | C6       |
| MOVW A,ext       | 5 | 3 | (AH) ← (ext), (AL) ← (ext + 1)                | AL | AH | dH | ++--  | C4       |
| MOVW A,@A        | 4 | 1 | (AH) ← ((A)), (AL) ← ((A) + 1)                | AL | AH | dH | ++--  | 93       |
| MOVW A,@EP       | 4 | 1 | (AH) ← ((EP)), (AL) ← ((EP) + 1)              | AL | AH | dH | ++--  | C7       |
| MOVW A,EP        | 2 | 1 | (A) ← (EP)                                    | -  | -  | dH | ----- | F3       |
| MOVW EP,#d16     | 3 | 3 | (EP) ← d16                                    | -  | -  | -  | ----- | E7       |
| MOVW IX,A        | 2 | 1 | (IX) ← (A)                                    | -  | -  | -  | ----- | E2       |
| MOVW A,IX        | 2 | 1 | (A) ← (IX)                                    | -  | -  | dH | ----- | F2       |
| MOVW SP,A        | 2 | 1 | (SP) ← (A)                                    | -  | -  | -  | ----- | E1       |
| MOVW A,SP        | 2 | 1 | (A) ← (SP)                                    | -  | -  | dH | ----- | F1       |
| MOV @A,T         | 3 | 1 | ((A)) ← (T)                                   | -  | -  | -  | ----- | 82       |
| MOVW @A,T        | 4 | 1 | ((A)) ← (TH),(A) + 1 ← (TL)                   | -  | -  | -  | ----- | 83       |
| MOVW IX,#d16     | 3 | 3 | (IX) ← d16                                    | -  | -  | -  | ----- | E6       |
| MOVW A,PS        | 2 | 1 | (A) ← (PS)                                    | -  | -  | dH | ----- | 70       |
| MOVW PS,A        | 2 | 1 | (PS) ← (A)                                    | -  | -  | -  | ++++  | 71       |
| MOVW SP,#d16     | 3 | 3 | (SP) ← d16                                    | -  | -  | -  | ----- | E5       |
| SWAP             | 2 | 1 | (AH) ↔ (AL)                                   | -  | -  | AL | ----- | 10       |
| SETB dir: b      | 4 | 2 | (dir): b ← 1                                  | -  | -  | -  | ----- | A8 to AF |
| CLRB dir: b      | 4 | 2 | (dir): b ← 0                                  | -  | -  | -  | ----- | A0 to A7 |
| XCH A,T          | 2 | 1 | (AL) ↔ (TL)                                   | AL | -  | -  | ----- | 42       |
| XCHW A,T         | 3 | 1 | (A) ↔ (T)                                     | AL | AH | dH | ----- | 43       |
| XCHW A,EP        | 3 | 1 | (A) ↔ (EP)                                    | -  | -  | dH | ----- | F7       |
| XCHW A,IX        | 3 | 1 | (A) ↔ (IX)                                    | -  | -  | dH | ----- | F6       |
| XCHW A,SP        | 3 | 1 | (A) ↔ (SP)                                    | -  | -  | dH | ----- | F5       |
| MOVW A,PC        | 2 | 1 | (A) ← (PC)                                    | -  | -  | dH | ----- | F0       |

Note During byte transfer to A, T ← A is restricted to low bytes.

Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F<sup>2</sup>MC-8 family)

# MB89601R Series

**Table 3 Arithmetic Operation Instructions (62 instructions)**

| Mnemonic        | ~  | # | Operation  | TL | TH | AH | NZVC | OP code  |
|-----------------|----|---|--|----|----|----|------|----------|
| ADDC A,Ri       | 3  | 1 | $(A) \leftarrow (A) + (Ri) + C$                  | -  | -  | -  | ++++ | 28 to 2F |
| ADDC A,#d8      | 2  | 2 | $(A) \leftarrow (A) + d8 + C$                    | -  | -  | -  | ++++ | 24       |
| ADDC A,dir      | 3  | 2 | $(A) \leftarrow (A) + (dir) + C$                 | -  | -  | -  | ++++ | 25       |
| ADDC A,@IX +off | 4  | 2 | $(A) \leftarrow (A) + ((IX) + off) + C$          | -  | -  | -  | ++++ | 26       |
| ADDC A,@EP      | 3  | 1 | $(A) \leftarrow (A) + ((EP)) + C$                | -  | -  | -  | ++++ | 27       |
| ADDCW A         | 3  | 1 | $(A) \leftarrow (A) + (T) + C$                   | -  | -  | dH | ++++ | 23       |
| ADDC A          | 2  | 1 | $(AL) \leftarrow (AL) + (TL) + C$                | -  | -  | -  | ++++ | 22       |
| SUBC A,Ri       | 3  | 1 | $(A) \leftarrow (A) - (Ri) - C$                  | -  | -  | -  | ++++ | 38 to 3F |
| SUBC A,#d8      | 2  | 2 | $(A) \leftarrow (A) - d8 - C$                    | -  | -  | -  | ++++ | 34       |
| SUBC A,dir      | 3  | 2 | $(A) \leftarrow (A) - (dir) - C$                 | -  | -  | -  | ++++ | 35       |
| SUBC A,@IX +off | 4  | 2 | $(A) \leftarrow (A) - ((IX) + off) - C$          | -  | -  | -  | ++++ | 36       |
| SUBC A,@EP      | 3  | 1 | $(A) \leftarrow (A) - ((EP)) - C$                | -  | -  | -  | ++++ | 37       |
| SUBCW A         | 3  | 1 | $(A) \leftarrow (T) - (A) - C$                   | -  | -  | dH | ++++ | 33       |
| SUBC A          | 2  | 1 | $(AL) \leftarrow (TL) - (AL) - C$                | -  | -  | -  | ++++ | 32       |
| INC Ri          | 4  | 1 | $(Ri) \leftarrow (Ri) + 1$                       | -  | -  | -  | +++- | C8 to CF |
| INCW EP         | 3  | 1 | $(EP) \leftarrow (EP) + 1$                       | -  | -  | -  | ---- | C3       |
| INCW IX         | 3  | 1 | $(IX) \leftarrow (IX) + 1$                       | -  | -  | -  | ---- | C2       |
| INCW A          | 3  | 1 | $(A) \leftarrow (A) + 1$                         | -  | -  | dH | ++-- | C0       |
| DEC Ri          | 4  | 1 | $(Ri) \leftarrow (Ri) - 1$                       | -  | -  | -  | +++- | D8 to DF |
| DECW EP         | 3  | 1 | $(EP) \leftarrow (EP) - 1$                       | -  | -  | -  | ---- | D3       |
| DECW IX         | 3  | 1 | $(IX) \leftarrow (IX) - 1$                       | -  | -  | -  | ---- | D2       |
| DECW A          | 3  | 1 | $(A) \leftarrow (A) - 1$                         | -  | -  | dH | ++-- | D0       |
| MULU A          | 19 | 1 | $(A) \leftarrow (AL) \times (TL)$                | -  | -  | dH | ---- | 01       |
| DIVU A          | 21 | 1 | $(A) \leftarrow (T) / (AL), MOD \rightarrow (T)$ | dL | 00 | 00 | ---- | 11       |
| ANDW A          | 3  | 1 | $(A) \leftarrow (A) \wedge (T)$                  | -  | -  | dH | ++R- | 63       |
| ORW A           | 3  | 1 | $(A) \leftarrow (A) \vee (T)$                    | -  | -  | dH | ++R- | 73       |
| XORW A          | 3  | 1 | $(A) \leftarrow (A) \nabla (T)$                  | -  | -  | dH | ++R- | 53       |
| CMP A           | 2  | 1 | $(TL) - (AL)$                                    | -  | -  | -  | ++++ | 12       |
| CMPW A          | 3  | 1 | $(T) - (A)$                                      | -  | -  | -  | ++++ | 13       |
| RORC A          | 2  | 1 | $\rightarrow C \rightarrow A$                    | -  | -  | -  | ++-+ | 03       |
| ROLC A          | 2  | 1 | $\leftarrow C \leftarrow A$                      | -  | -  | -  | ++-+ | 02       |
| CMP A,#d8       | 2  | 2 | $(A) - d8$                                       | -  | -  | -  | ++++ | 14       |
| CMP A,dir       | 3  | 2 | $(A) - (dir)$                                    | -  | -  | -  | ++++ | 15       |
| CMP A,@EP       | 3  | 1 | $(A) - ((EP))$                                   | -  | -  | -  | ++++ | 17       |
| CMP A,@IX +off  | 4  | 2 | $(A) - ((IX) + off)$                             | -  | -  | -  | ++++ | 16       |
| CMP A,Ri        | 3  | 1 | $(A) - (Ri)$                                     | -  | -  | -  | ++++ | 18 to 1F |
| DAA             | 2  | 1 | Decimal adjust for addition                      | -  | -  | -  | ++++ | 84       |
| DAS             | 2  | 1 | Decimal adjust for subtraction                   | -  | -  | -  | ++++ | 94       |
| XOR A           | 2  | 1 | $(A) \leftarrow (AL) \nabla (TL)$                | -  | -  | -  | ++R- | 52       |
| XOR A,#d8       | 2  | 2 | $(A) \leftarrow (AL) \nabla d8$                  | -  | -  | -  | ++R- | 54       |
| XOR A,dir       | 3  | 2 | $(A) \leftarrow (AL) \nabla (dir)$               | -  | -  | -  | ++R- | 55       |
| XOR A,@EP       | 3  | 1 | $(A) \leftarrow (AL) \nabla ((EP))$              | -  | -  | -  | ++R- | 57       |
| XOR A,@IX +off  | 4  | 2 | $(A) \leftarrow (AL) \nabla ((IX) + off)$        | -  | -  | -  | ++R- | 56       |
| XOR A,Ri        | 3  | 1 | $(A) \leftarrow (AL) \nabla (Ri)$                | -  | -  | -  | ++R- | 58 to 5F |
| AND A           | 2  | 1 | $(A) \leftarrow (AL) \wedge (TL)$                | -  | -  | -  | ++R- | 62       |
| AND A,#d8       | 2  | 2 | $(A) \leftarrow (AL) \wedge d8$                  | -  | -  | -  | ++R- | 64       |
| AND A,dir       | 3  | 2 | $(A) \leftarrow (AL) \wedge (dir)$               | -  | -  | -  | ++R- | 65       |

(Continued)

(Continued)

| Mnemonic         | ~ | # | Operation  | TL | TH | AH | NZVC | OP code  |
|------------------|---|---|--|----|----|----|------|----------|
| AND A,@EP        | 3 | 1 | $(A) \leftarrow (AL) \wedge (EP)$                | -  | -  | -  | ++R- | 67       |
| AND A,@IX +off   | 4 | 2 | $(A) \leftarrow (AL) \wedge ((IX) + \text{off})$ | -  | -  | -  | ++R- | 66       |
| AND A,Ri         | 3 | 1 | $(A) \leftarrow (AL) \wedge (Ri)$                | -  | -  | -  | ++R- | 68 to 6F |
| OR A             | 2 | 1 | $(A) \leftarrow (AL) \vee (TL)$                  | -  | -  | -  | ++R- | 72       |
| OR A,#d8         | 2 | 2 | $(A) \leftarrow (AL) \vee d8$                    | -  | -  | -  | ++R- | 74       |
| OR A,dir         | 3 | 2 | $(A) \leftarrow (AL) \vee (\text{dir})$          | -  | -  | -  | ++R- | 75       |
| OR A,@EP         | 3 | 1 | $(A) \leftarrow (AL) \vee (EP)$                  | -  | -  | -  | ++R- | 77       |
| OR A,@IX +off    | 4 | 2 | $(A) \leftarrow (AL) \vee ((IX) + \text{off})$   | -  | -  | -  | ++R- | 76       |
| OR A,Ri          | 3 | 1 | $(A) \leftarrow (AL) \vee (Ri)$                  | -  | -  | -  | ++R- | 78 to 7F |
| CMP dir,#d8      | 5 | 3 | $(\text{dir}) - d8$                              | -  | -  | -  | ++++ | 95       |
| CMP @EP,#d8      | 4 | 2 | $(EP) - d8$                                      | -  | -  | -  | ++++ | 97       |
| CMP @IX +off,#d8 | 5 | 3 | $((IX) + \text{off}) - d8$                       | -  | -  | -  | ++++ | 96       |
| CMP Ri,#d8       | 4 | 2 | $(Ri) - d8$                                      | -  | -  | -  | ++++ | 98 to 9F |
| INCW SP          | 3 | 1 | $(SP) \leftarrow (SP) + 1$                       | -  | -  | -  | ---- | C1       |
| DECW SP          | 3 | 1 | $(SP) \leftarrow (SP) - 1$                       | -  | -  | -  | ---- | D1       |

**Table 4 Branch Instructions (17 instructions)**

| Mnemonic       | ~ | # | Operation  | TL | TH | AH | NZVC    | OP code  |
|----------------|---|---|--|----|----|----|---------|----------|
| BZ/BEQ rel     | 3 | 2 | If $Z = 1$ then $PC \leftarrow PC + \text{rel}$                | -  | -  | -  | ----    | FD       |
| BNZ/BNE rel    | 3 | 2 | If $Z = 0$ then $PC \leftarrow PC + \text{rel}$                | -  | -  | -  | ----    | FC       |
| BC/BLO rel     | 3 | 2 | If $C = 1$ then $PC \leftarrow PC + \text{rel}$                | -  | -  | -  | ----    | F9       |
| BNC/BHS rel    | 3 | 2 | If $C = 0$ then $PC \leftarrow PC + \text{rel}$                | -  | -  | -  | ----    | F8       |
| BN rel         | 3 | 2 | If $N = 1$ then $PC \leftarrow PC + \text{rel}$                | -  | -  | -  | ----    | FB       |
| BP rel         | 3 | 2 | If $N = 0$ then $PC \leftarrow PC + \text{rel}$                | -  | -  | -  | ----    | FA       |
| BLT rel        | 3 | 2 | If $V \vee N = 1$ then $PC \leftarrow PC + \text{rel}$         | -  | -  | -  | ----    | FF       |
| BGE rel        | 3 | 2 | If $V \vee N = 0$ then $PC \leftarrow PC + \text{rel}$         | -  | -  | -  | ----    | FE       |
| BBC dir: b,rel | 5 | 3 | If $(\text{dir: } b) = 0$ then $PC \leftarrow PC + \text{rel}$ | -  | -  | -  | -+---   | B0 to B7 |
| BBS dir: b,rel | 5 | 3 | If $(\text{dir: } b) = 1$ then $PC \leftarrow PC + \text{rel}$ | -  | -  | -  | -+---   | B8 to BF |
| JMP @A         | 2 | 1 | $(PC) \leftarrow (A)$  | -  | -  | -  | ----    | E0       |
| JMP ext        | 3 | 3 | $(PC) \leftarrow \text{ext}$                                   | -  | -  | -  | ----    | 21       |
| CALLV #vct     | 6 | 1 | Vector call  | -  | -  | -  | ----    | E8 to EF |
| CALL ext       | 6 | 3 | Subroutine call  | -  | -  | -  | ----    | 31       |
| XCHW A,PC      | 3 | 1 | $(PC) \leftarrow (A), (A) \leftarrow (PC) + 1$                 | -  | -  | dH | ----    | F4       |
| RET            | 4 | 1 | Return from subroutine   | -  | -  | -  | ----    | 20       |
| RETI           | 6 | 1 | Return from interrupt  | -  | -  | -  | Restore | 30       |

**Table 5 Other Instructions (9 instructions)**

| Mnemonic | ~ | # | Operation | TL | TH | AH | NZVC  | OP code |
|----------|---|---|-----------|----|----|----|-------|---------|
| PUSHW A  | 4 | 1 |           | -  | -  | -  | ----  | 40      |
| POPW A   | 4 | 1 |           | -  | -  | dH | ----  | 50      |
| PUSHW IX | 4 | 1 |           | -  | -  | -  | ----  | 41      |
| POPW IX  | 4 | 1 |           | -  | -  | -  | ----  | 51      |
| NOP      | 1 | 1 |           | -  | -  | -  | ----  | 00      |
| CLRC     | 1 | 1 |           | -  | -  | -  | ----R | 81      |
| SETC     | 1 | 1 |           | -  | -  | -  | ----S | 91      |
| CLRI     | 1 | 1 |           | -  | -  | -  | ----  | 80      |
| SETI     | 1 | 1 |           | -  | -  | -  | ----  | 90      |

# MB89601R Series

## INSTRUCTION MAP

| L | H              | 0              | 1               | 2               | 3              | 4              | 5              | 6              | 7             | 8                | 9                | A              | B                 | C               | D               | E               | F            |
|---|----------------|----------------|-----------------|-----------------|----------------|----------------|----------------|----------------|---------------|------------------|------------------|----------------|-------------------|-----------------|-----------------|-----------------|--------------|
| 0 | NOP            | SWAP           | RET             | RETI            | PUSHW<br>A     | PUSHW<br>IX    | POPW<br>A      | MOV<br>A,ext   | MOVW<br>A,PS  | CLR<br>I         | SETI             | CLRB<br>dir: 0 | BBC<br>dir: 0,rel | INCW<br>A       | DECW<br>A       | JMP<br>@A       | MOVW<br>A,PC |
| 1 | MULU<br>A      | DIVU<br>A      | JMP<br>addr16   | CALL<br>addr16  | PUSHW<br>IX    | PUSHW<br>IX    | POPW<br>PS,A   | MOV<br>ext,A   | MOVW<br>PS,A  | CLRC             | SETC             | CLRB<br>dir: 1 | BBC<br>dir: 1,rel | INCW<br>SP      | DECW<br>SP      | MOVW<br>SPA     | MOVW<br>A,SP |
| 2 | ROL<br>A       | CMP<br>A       | ADDC<br>A       | SUBC<br>A       | XCH<br>A,T     | XCH<br>A,T     | XOR<br>A       | AND<br>A       | OR<br>A       | MOV<br>@A,T      | MOV<br>A,@A      | CLRB<br>dir: 2 | BBC<br>dir: 2,rel | INCW<br>IX      | DECW<br>IX      | MOVW<br>IX,A    | MOVW<br>A,IX |
| 3 | ROR<br>A       | CMPW<br>A      | ADDCW<br>A      | SUBCW<br>A      | XCHW<br>A,T    | XCHW<br>A,T    | XORW<br>A      | ANDW<br>A      | ORW<br>A      | MOVW<br>@A,T     | MOVW<br>A,@A     | CLRB<br>dir: 3 | BBC<br>dir: 3,rel | INCW<br>EP      | DECW<br>EP      | MOVW<br>EPA     | MOVW<br>A,EP |
| 4 | MOV<br>A,#d8   | CMP<br>A,#d8   | ADDC<br>A,#d8   | SUBC<br>A,#d8   | XOR<br>A,#d8   | XOR<br>A,#d8   | XOR<br>A,#d8   | AND<br>A,#d8   | OR<br>A,#d8   | DAA              | DAS              | CLRB<br>dir: 4 | BBC<br>dir: 4,rel | MOVW<br>A,ext   | MOVW<br>ext,A   | MOVW<br>A,#d16  | XCHW<br>A,PC |
| 5 | MOV<br>A,dir   | CMP<br>A,dir   | ADDC<br>A,dir   | SUBC<br>A,dir   | XOR<br>A,dir   | XOR<br>A,dir   | XOR<br>A,dir   | AND<br>A,dir   | OR<br>A,dir   | MOV<br>dir,#d8   | CMP<br>dir,#d8   | CLRB<br>dir: 5 | BBC<br>dir: 5,rel | MOVW<br>A,dir   | MOVW<br>dir,A   | MOVW<br>SP#d16  | XCHW<br>A,SP |
| 6 | MOV<br>A,@IX+d | CMP<br>A,@IX+d | ADDC<br>A,@IX+d | SUBC<br>A,@IX+d | XOR<br>A,@IX+d | XOR<br>A,@IX+d | XOR<br>A,@IX+d | AND<br>A,@IX+d | OR<br>A,@IX+d | MOV<br>@IX+d,#d8 | CMP<br>@IX+d,#d8 | CLRB<br>dir: 6 | BBC<br>dir: 6,rel | MOVW<br>A,@IX+d | MOVW<br>@IX+d,A | MOVW<br>IX,#d16 | XCHW<br>A,IX |
| 7 | MOV<br>A,@EP   | CMP<br>A,@EP   | ADDC<br>A,@EP   | SUBC<br>A,@EP   | XOR<br>A,@EP   | XOR<br>A,@EP   | XOR<br>A,@EP   | AND<br>A,@EP   | OR<br>A,@EP   | MOV<br>@EP,#d8   | CMP<br>@EP,#d8   | CLRB<br>dir: 7 | BBC<br>dir: 7,rel | MOVW<br>A,@EP   | MOVW<br>@EP,A   | MOVW<br>EP#d16  | XCHW<br>A,EP |
| 8 | MOV<br>A,R0    | CMP<br>A,R0    | ADDC<br>A,R0    | SUBC<br>A,R0    | XOR<br>R0,A    | MOV<br>R0,A    | XOR<br>A,R0    | AND<br>A,R0    | OR<br>A,R0    | MOV<br>R0,#d8    | CMP<br>R0,#d8    | SETB<br>dir: 0 | BBS<br>dir: 0,rel | INC<br>R0       | DEC<br>R0       | CALLV<br>#0     | BNC<br>rel   |
| 9 | MOV<br>A,R1    | CMP<br>A,R1    | ADDC<br>A,R1    | SUBC<br>A,R1    | MOV<br>R1,A    | MOV<br>A,R1    | XOR<br>A,R1    | AND<br>A,R1    | OR<br>A,R1    | MOV<br>R1,#d8    | CMP<br>R1,#d8    | SETB<br>dir: 1 | BBS<br>dir: 1,rel | INC<br>R1       | DEC<br>R1       | CALLV<br>#1     | BC<br>rel    |
| A | MOV<br>A,R2    | CMP<br>A,R2    | ADDC<br>A,R2    | SUBC<br>A,R2    | MOV<br>R2,A    | MOV<br>A,R2    | XOR<br>A,R2    | AND<br>A,R2    | OR<br>A,R2    | MOV<br>R2,#d8    | CMP<br>R2,#d8    | SETB<br>dir: 2 | BBS<br>dir: 2,rel | INC<br>R2       | DEC<br>R2       | CALLV<br>#2     | BP<br>rel    |
| B | MOV<br>A,R3    | CMP<br>A,R3    | ADDC<br>A,R3    | SUBC<br>A,R3    | MOV<br>R3,A    | MOV<br>A,R3    | XOR<br>A,R3    | AND<br>A,R3    | OR<br>A,R3    | MOV<br>R3,#d8    | CMP<br>R3,#d8    | SETB<br>dir: 3 | BBS<br>dir: 3,rel | INC<br>R3       | DEC<br>R3       | CALLV<br>#3     | BN<br>rel    |
| C | MOV<br>A,R4    | CMP<br>A,R4    | ADDC<br>A,R4    | SUBC<br>A,R4    | MOV<br>R4,A    | MOV<br>A,R4    | XOR<br>A,R4    | AND<br>A,R4    | OR<br>A,R4    | MOV<br>R4,#d8    | CMP<br>R4,#d8    | SETB<br>dir: 4 | BBS<br>dir: 4,rel | INC<br>R4       | DEC<br>R4       | CALLV<br>#4     | BNZ<br>rel   |
| D | MOV<br>A,R5    | CMP<br>A,R5    | ADDC<br>A,R5    | SUBC<br>A,R5    | MOV<br>R5,A    | MOV<br>A,R5    | XOR<br>A,R5    | AND<br>A,R5    | OR<br>A,R5    | MOV<br>R5,#d8    | CMP<br>R5,#d8    | SETB<br>dir: 5 | BBS<br>dir: 5,rel | INC<br>R5       | DEC<br>R5       | CALLV<br>#5     | BZ<br>rel    |
| E | MOV<br>A,R6    | CMP<br>A,R6    | ADDC<br>A,R6    | SUBC<br>A,R6    | MOV<br>R6,A    | MOV<br>A,R6    | XOR<br>A,R6    | AND<br>A,R6    | OR<br>A,R6    | MOV<br>R6,#d8    | CMP<br>R6,#d8    | SETB<br>dir: 6 | BBS<br>dir: 6,rel | INC<br>R6       | DEC<br>R6       | CALLV<br>#6     | BGE<br>rel   |
| F | MOV<br>A,R7    | CMP<br>A,R7    | ADDC<br>A,R7    | SUBC<br>A,R7    | MOV<br>R7,A    | MOV<br>A,R7    | XOR<br>A,R7    | AND<br>A,R7    | OR<br>A,R7    | MOV<br>R7,#d8    | CMP<br>R7,#d8    | SETB<br>dir: 7 | BBS<br>dir: 7,rel | INC<br>R7       | DEC<br>R7       | CALLV<br>#7     | BLT<br>rel   |

## ■ MASK OPTIONS

| No. | Part number   | MB89601R<br>MB89603                                 | MB89P601   | MB89PV620                                    |
|-----|---|---|--|--|
|     | Specifying procedure  | Specify when ordering masking                       | Setting not possible                                 | Setting not possible                         |
| 1   | Pull-up resistors<br><ul style="list-style-type: none"> <li>┌ P00 to P07, P10 to P17,</li> <li>└ P40 to P47<sup>*2</sup>, P60<sup>*2</sup></li> </ul>   | Selectable by pin                                   | Fixed to without pull-up resistor                    | Fixed to without pull-up resistor            |
|     | P30 to P33 <sup>*1</sup>  | Selectable by pin<br>(Software pull-up resistor)    | Can be set per pin<br>(Software pull-up resistor)    |  |
|     | P33 to P37 <sup>*1</sup>  | Selectable by 4 pins<br>(Software pull-up resistor) | Can be set per 4 pins<br>(Software pull-up resistor) |  |
| 2   | Power-on reset selection<br><ul style="list-style-type: none"> <li>┌ With power-on reset</li> <li>└ Without power-on reset</li> </ul>   | Selectable  | Fixed to with power-on reset                         | Fixed to with power-on reset                 |
| 3   | Selection of the oscillation stabilization time<br><ul style="list-style-type: none"> <li>┌ Crystal oscillator: (<math>2^{18}/F_c</math>)</li> <li>└ Ceramic oscillator: (<math>2^{12}/F_c</math>)</li> </ul> | Selectable  | Fixed to crystal oscillator ( $2^{18}/F_c$ )         | Fixed to crystal oscillator ( $2^{18}/F_c$ ) |
| 4   | Reset pin output<br><ul style="list-style-type: none"> <li>┌ With reset output</li> <li>└ Without reset output</li> </ul>   | Selectable  | Fixed to with reset output                           | Fixed to with reset output                   |

\*1: A pull-up resistor for P30 to P37 is not set when ordering masking. It is set by software.

\*2: When a pull-up resistor for P40 to P47 and P60 is selected, the input signal exceeding  $V_{CC}$  voltage is not possible.

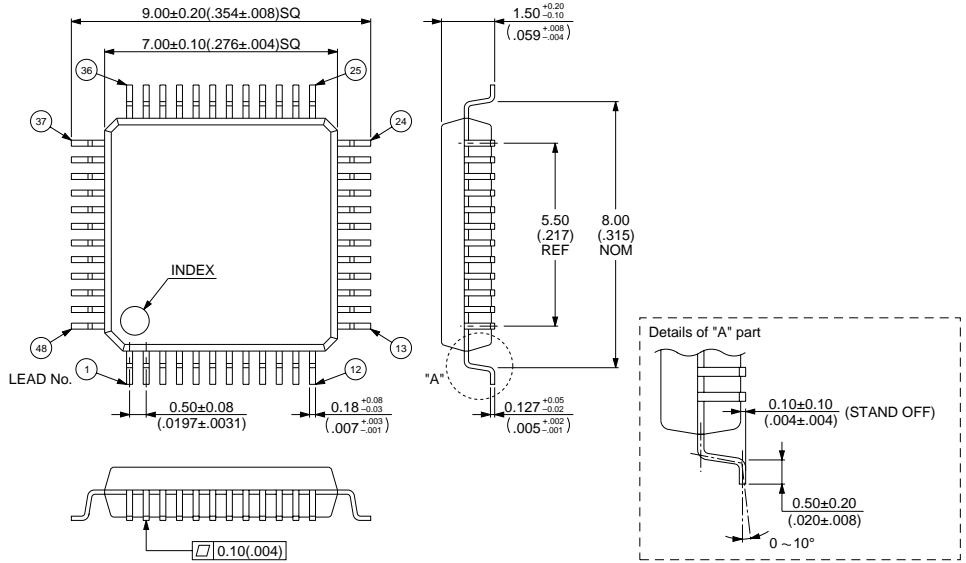
## ■ ORDERING INFORMATION

| Part number                              | Package                              | Remarks |
|--|--------------------------------------|---------|
| MB89601RPFV<br>MB89603PFV<br>MB89P601PFV | 48-pin Plastic SQFP<br>(FPT-48P-M05) |         |
| MB89PV620C-SH                            | 64-pin Ceramic MDIP<br>(MDP-64C-P02) |         |
| MB89PV620CF                              | 64-pin Ceramic MQFP<br>(MQP-64C-P01) |         |

# MB89601R Series

## PACKAGE DIMENSIONS

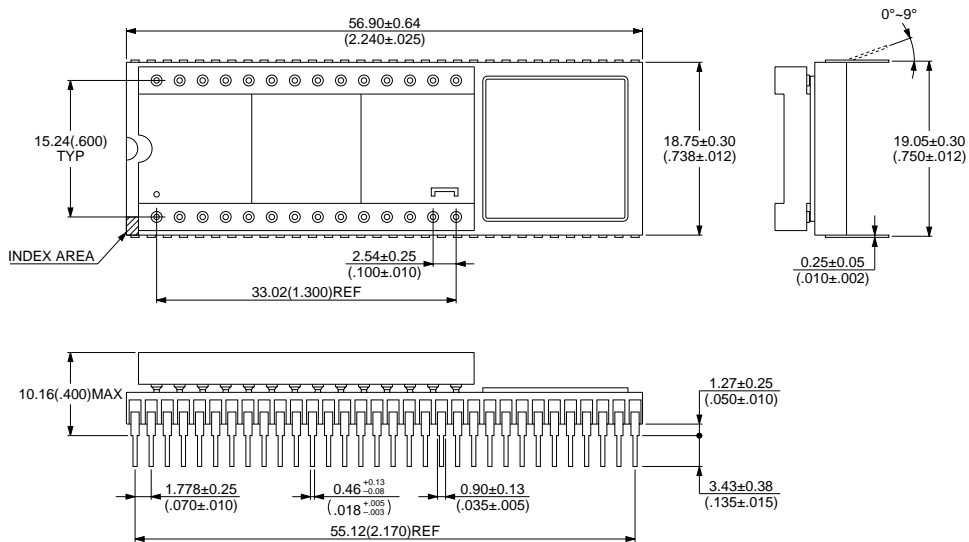
48 pin, Plastic LQFP  
(FPT-48P-M05)



© 1994 FUJITSU LIMITED F48013S-2C-4

Dimensions in mm (inches).

64-pin Ceramic MDIP  
(MDP-64C-P02)



© 1994 FUJITSU LIMITED M64002SC-14

Dimensions in mm (inches).





**MEMO**



**MEMO**

## FUJITSU LIMITED

*For further information please contact:*

### **Japan**

FUJITSU LIMITED  
Corporate Global Business Support Division  
Electronic Devices  
KAWASAKI PLANT, 4-1-1, Kamikodanaka,  
Nakahara-ku, Kawasaki-shi,  
Kanagawa 211-8588, Japan  
Tel: +81-44-754-3763  
Fax: +81-44-754-3329

<http://www.fujitsu.co.jp/>

### **North and South America**

FUJITSU MICROELECTRONICS, INC.  
3545 North First Street,  
San Jose, CA 95134-1804, USA  
Tel: +1-408-922-9000  
Fax: +1-408-922-9179

Customer Response Center  
*Mon. - Fri.: 7 am - 5 pm (PST)*  
Tel: +1-800-866-8608  
Fax: +1-408-922-9179

<http://www.fujitsumicro.com/>

### **Europe**

FUJITSU MICROELECTRONICS EUROPE GmbH  
Am Siebenstein 6-10,  
D-63303 Dreieich-Buchsschlag,  
Germany  
Tel: +49-6103-690-0  
Fax: +49-6103-690-122

<http://www.fujitsu-fme.com/>

### **Asia Pacific**

FUJITSU MICROELECTRONICS ASIA PTE LTD  
#05-08, 151 Lorong Chuan,  
New Tech Park,  
Singapore 556741  
Tel: +65-281-0770  
Fax: +65-281-0220

<http://www.fmap.com.sg/>

F9703

© FUJITSU LIMITED Printed in Japan

All Rights Reserved.

The contents of this document are subject to change without notice.

Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The contents of this document may not be reproduced or copied without the permission of FUJITSU LIMITED.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipments, industrial, communications, and measurement equipments, personal or household devices, etc.).  
**CAUTION:**

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.