Melexis
Microelectronic Integrated Systems

TH8080

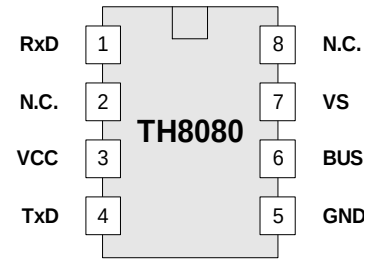
Single LIN Bus Transceiver

Features and Benefits

- Single wire LIN transceiver
- Compatible to LIN Protocol Specification, Rev. 1.1
- Compatible to ISO9141 functions
- Up to 20 kbps bus speed
- Low RFI due to slew rate control
- Fully integrated receiver filter
- Protection against load dump, jump start
- Bus terminals proof against short-circuits and transients in the automotive environment
- Very low (30 µA) typical power consumption in recessive state and therefore no sleep mode necessary
- Thermal overload and short circuit protection
- High impendance Bus pin in case of loss of ground and undervoltage condition
- 8-pin SOIC
- ±4kV ESD protection on Bus pin

Pin Diagram

SOIC8NB



Ordering Information

Part No.	***Temperature Range***	***Package***
TH8080 JDC	-40ºC...125ºC	SOIC8, 150mil

General Description

The TH8080 is a physical layer device for a single wire data link capable of operating in applications where high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and in the microprocessor which use the network. The TH8080 is designed in accordance to the physical layer definition of the LIN Protocol Specification , Rev. 1.1 . The IC furthermore can be used in ISO9141 systems.

Because of the very low current consumption of the TH8080 in the recessive state it's particularly suitable for ECU applications with hard standby current requirements , whereby no sleep/wake up control due to the microprocessor is necessary.

Functional Diagram

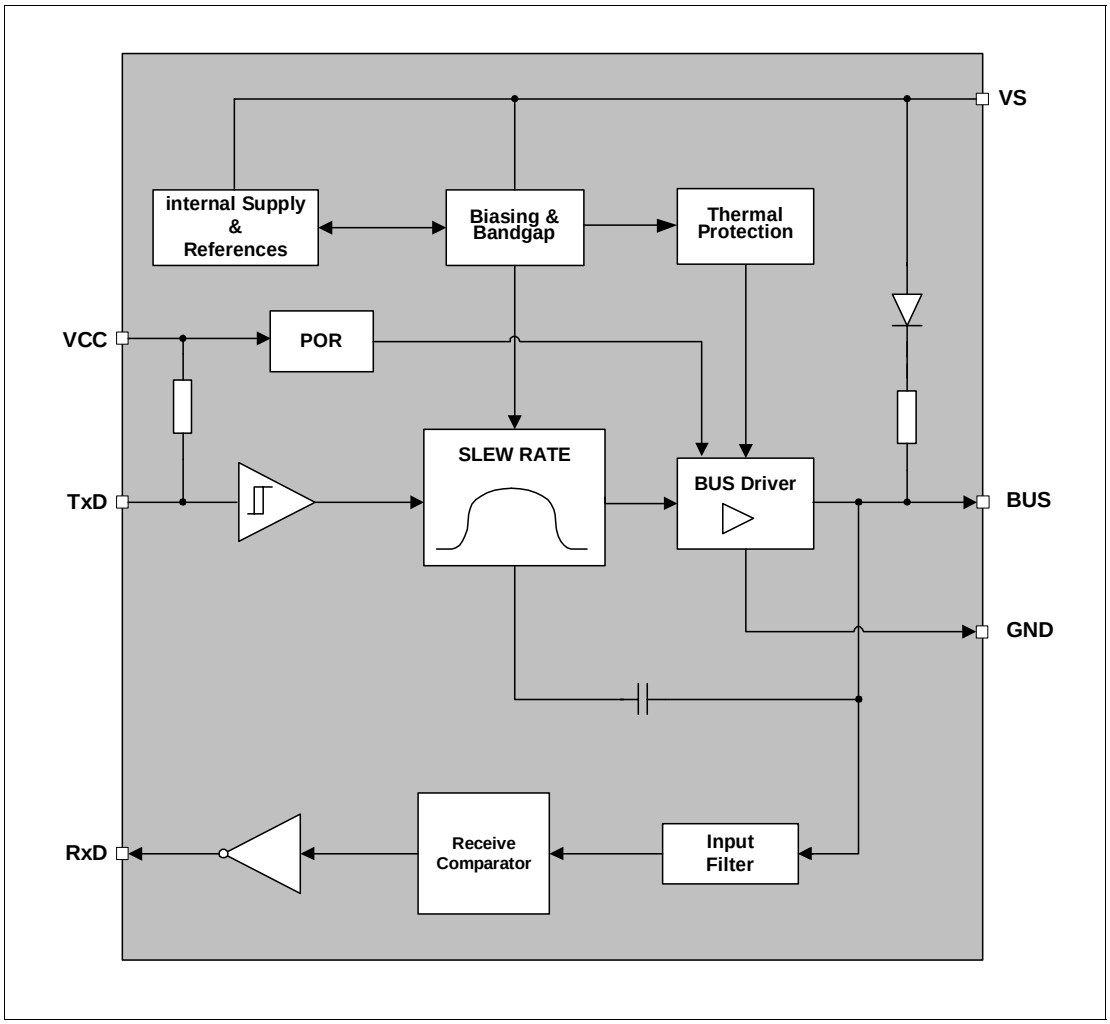


Figure 1 - Block Diagram

Application Circuit

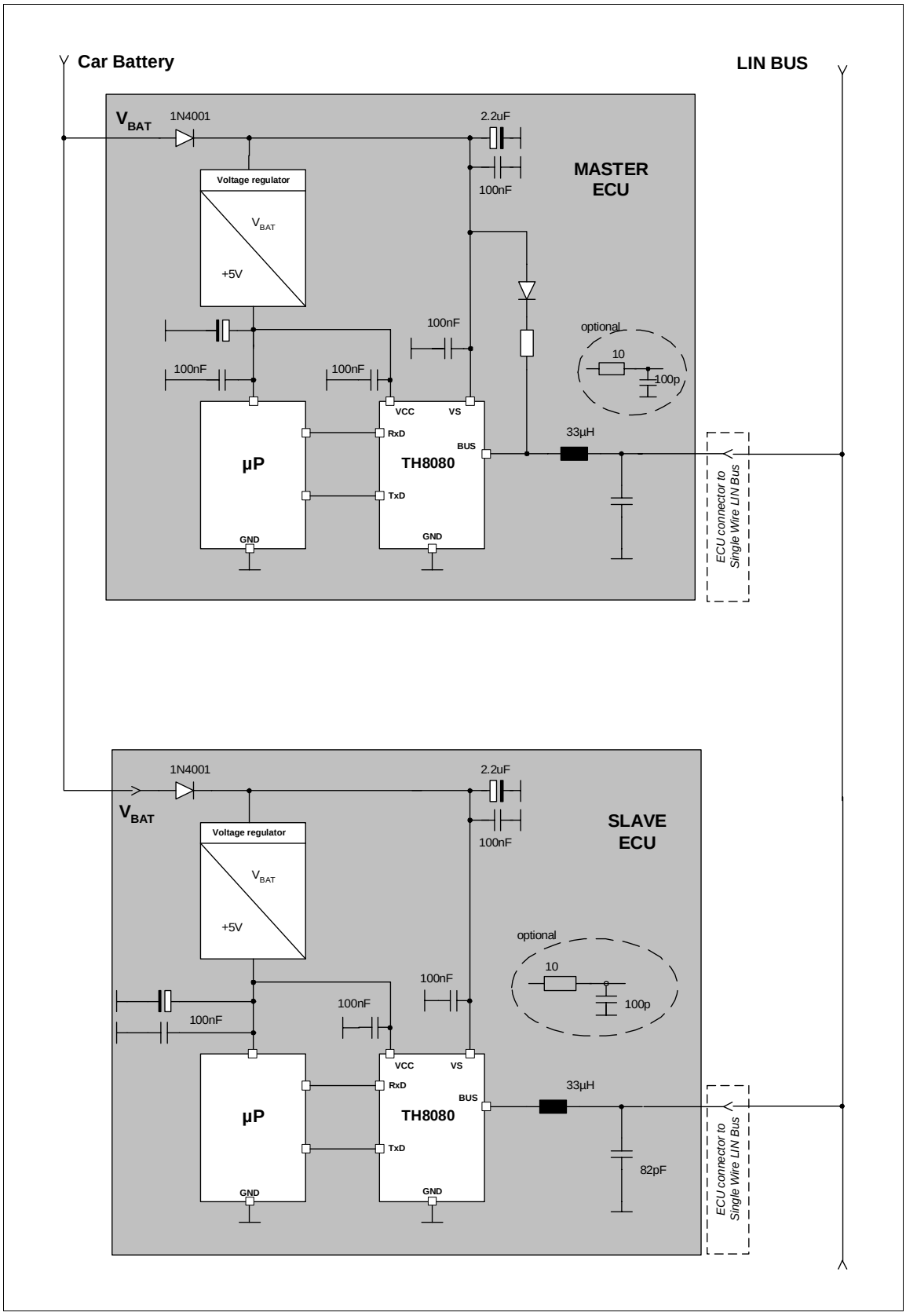


Figure 2 - Application Circuit

Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC. The absolute maximum ratings given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Reliable operation of the TH8080 is only specified within the limits shown in "Operating conditions".

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery voltage	V_S	6	20	V
Supply voltage	V_{CC}	4.5	5.5	V
Operating ambient temperature	T_A	-40	+125	°C
Junction temperature [1]	T_{Jc}		+150	°C

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Max.	Unit
Batterry Supply Voltage	V_S		-0.3	+27	V
Supply Voltage	V_{CC}		-0.3	+7	V
Short-term supply voltage	$V_{S.ld}$	Load dump; t<500ms		+40	V
Transient supply voltage	$V_{S.tr1}$	ISO 7637/1 pulse 1[1]	-150		V
Transient supply voltage	$V_{S.tr2}$	ISO 7637/1 pulses 2[1]		+100	V
Transient supply voltage	$V_{S.tr3}$	ISO 7637/1 pulses 3A, 3B	-150	+150	V
BUS voltage	V_{BUS}		-40	+40	V
Transient bus voltage	$V_{BUS.tr1}$	ISO 7637/1 pulse 1 [2]	-150		V
Transient bus voltage	$V_{BUS.tr2}$	ISO 7637/1 pulses 2 [2]		+100	V
Transient bus voltage	$V_{BUS.tr3}$	ISO 7637/1 pulses 3A, 3B [2]	-150	+150	V
DC voltage on pins TxD, RxD	V_{DC}		-0.3	+7	V
ESD capability of pin BUS	ESD_{BUSHB}	Human body model, equivalent to discharge 100pF with 1.5kΩ	-4	+4	kV
ESD capability of any other pins	ESD_{HB}	Human body model, equivalent to discharge 100pF with 1.5kΩ	-2	+2	kV
Maximum latch – up free current at any Pin	I_{LATCH}		-500	+500	mA
Maximum power dissipation	P_{tot}	At T_{amb} = +125 °C		197	mW
Thermal impedance	Θ_{JA}	in free air		152	K/W
Storage temperature	T_{stg}		-55	+150	°C
Junction temperature	T_{vj}		-40	+150	°C

[1] ISO 7637 test pulses are applied to VS via a reverse polarity diode and >1uF blocking capacitor .
[2] ISO 7637 test pulses are applied to BUS via a coupling capacitance of 1 nF.

Static Characteristics

(V_S = 6 to 20V, V_{CC}= 4.5 to 5.5V, T_A = -40 to +125°C, unless otherwise specified)
All voltages are referenced to ground (GND), positive currents are flow into the IC.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PIN VS,VCC						
Supply current, dominant	I_{Sd}	V_S = 16V,V_{CC} = 5.5V TxD=L		tbd	50	µA
Supply current, dominant	I_{CCd}	V_S = 16V,V_{CC} = 5.5V TxD=L		tbd	1	mA
Supply current, recessive	I_{Sr}	V_S = 16V,V_{CC} = 5.5V TxD open		8	20	µA
Supply current, recessive	I_{CCr}	V_S = 16V,V_{CC} = 5.5V TxD open		20	30	µA
PIN BUS / TRANSMITTER						
Bus output voltage, dominant	V_{ol_BUS}	TxD=L , I_{BUS} = 40mA			1.2	V
Bus output voltage, recessive	V_{oh_BUS}	V_S = 8...18V, TxD open	0.8* V_S			V
Bus short circuit current	I_{BUS_SHORT}	TxD=L , V_{BUS} > 2.5V	40		130	mA
Bus input current, recessive	I_{BUS_leakp}	TxD open ,V_{BUS} = 18V	-20		20	µA
Bus reverse polarity current, re-	I_{BUS_leakn}	TxD open ,V_{BUS} = -18V	-1		1	mA
Bus pull up resistor	R_{BUS_pu}		20	30	47	kΩ
PIN BUS / RECEIVER						
Bus input threshold, recessive to dominant	V_{ihBUS_rd}	TxD open , -18V<V_{BUS} < V_{ihBUS_rd}	0.4x V_S	0.45* V_S		V
Bus input threshold, dominant to recessive	V_{ihBUS_rd}	TxD open , V_{ihBUS_rd} <V_{BUS} < 18V		0.55* V_S	0.6*V_S	V
Bus input hysteresis	V_{BUS_hys}		20			mV
PIN TXD						
High level input voltage	V_{ih}	Rising edge			0.7* V_{CC}	V
Low level input voltage	V_{il}	Falling edge	0.3* V_{CC}			V
TxD pull up current, high level	I_{IH_TXD}	V_{TxD} = 4V	-125	-50	-25	µA
TxD pull up current, low level	I_{IH_TXD}	V_{TxD} = 1V	-500	-250	-100	µA
PIN RXD						
Low level output voltage	V_{ol_rxd}	I_{RxD} = 1.25mA			0.9	V
High level output voltage	V_{oh_rxd}	I_{RxD} = -250µA	V_{CC} -0.9			V
Thermal protection						
Thermal shutdown	T_{sd} [1]		150		180	°C
Hysteresis	T_{hys} [1]		5		25	°C

[1] Thresholds not tested in production, guaranteed by design, only switch on/off tested .

Dynamic Characteristics

All dynamic values of the table below refer to the test-schematic schown in Figure - Timing Diagram
($6V \leq V_S \leq 20V$, $-40°C \leq T_A \leq 125°C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Slew rate falling edge	t_{SRF}	80% < VBUS < 20% , minimum & maximum bus load	-2.5	-1.7	-1	V/µs
Slew rate rising edge	t_{SRR}	20% < VBUS < 80% , minimum bus load [1]	1	1.7	2.5	V/µs
Propagation delay transmitter (TxD->BUS)	t_{trans_pdf}	TxD high to low transition[2]			4	µs
Propagation delay transmitter (TxD->BUS)	t_{trans_pdr}	TxD low to high transition[2]			4	µs
Propagation delay transmitter symmetry	t_{trans_sym}	Calculate t_{trans_pdf} - t_{trans_pdr}	-2		2	µs
Propagation delay receiver (BUS->RxD)	t_{rec_pdf}	BUS recessive to dominant [2]			6	µs
Propagation delay receiver (BUS->RxD)	t_{rec_pdr}	BUS dominant to recessive[2]			6	µs
Propagation delay receiver symmetry	t_{rec_sym}	Calculate t_{trans_pdf} - t_{trans_pdr}	-2		2	µs
Receiver debounce time	t_{rec_deb}	BUS rising & falling edge[3]	1.2		3.1	µs

[1] Minimum slew rate of the rising edge is determined by the network time constant

[2] See timing diagram figure 3

[3] See timing diagram figure 4

Timing Diagrams

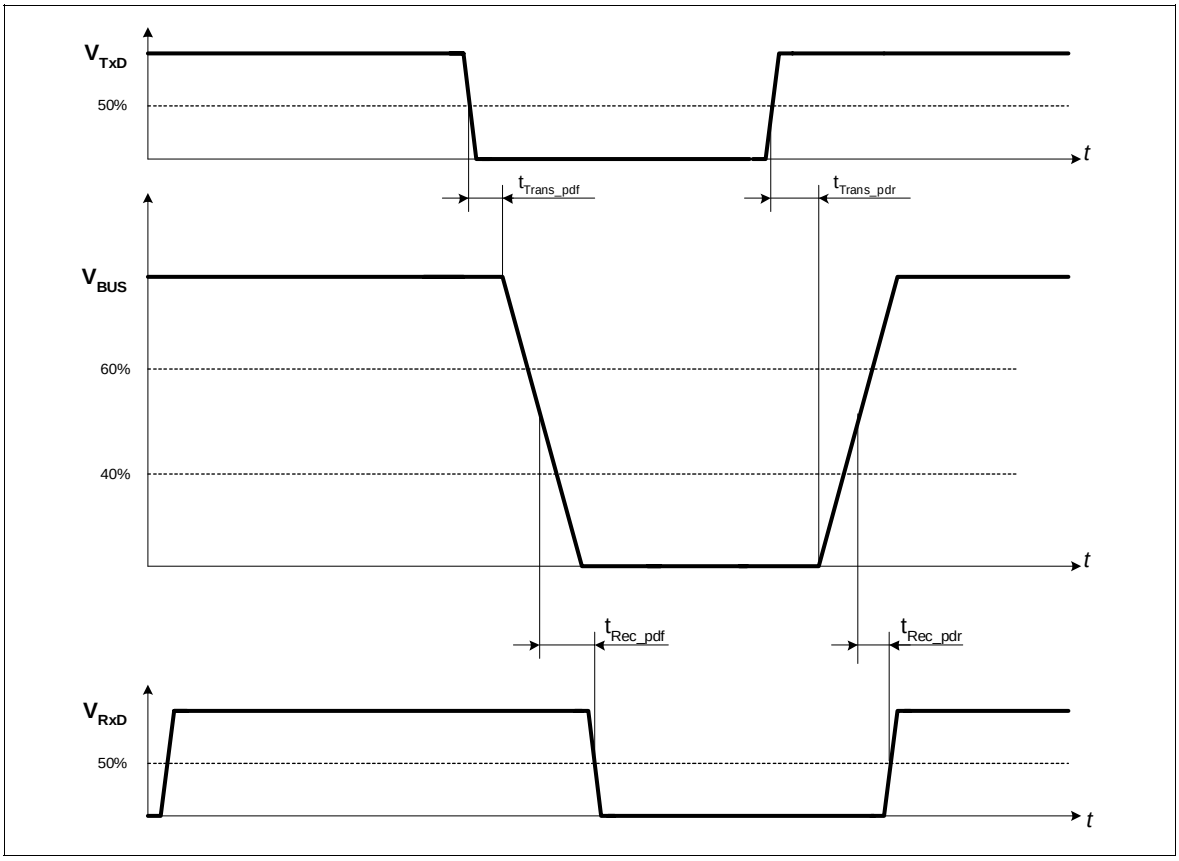


Figure 3 - Input/Output Timing

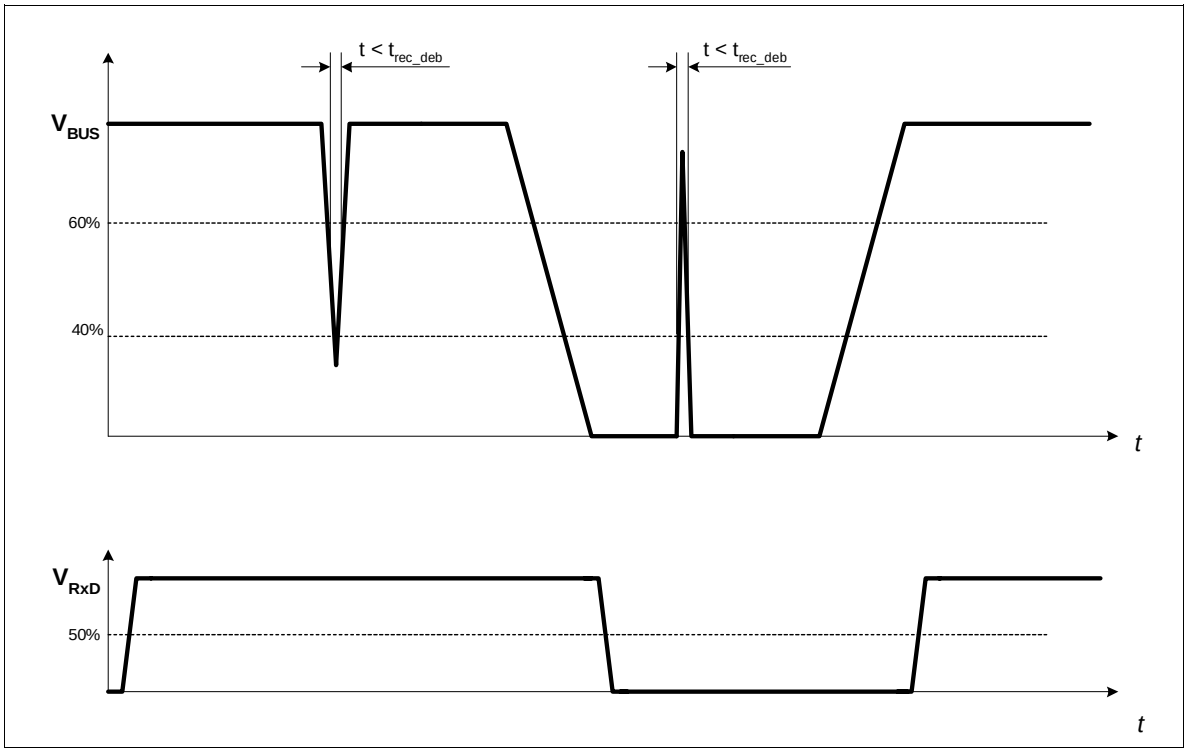


Figure 4 - Receiver Debouncing Filter

Test Circuit for Dynamic Characteristics

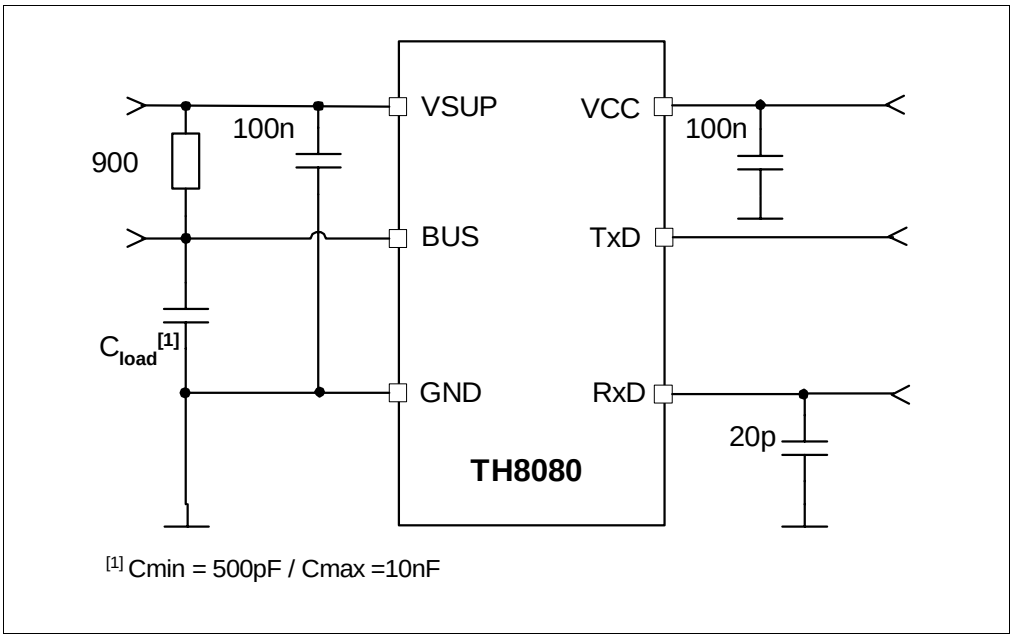


Figure 5 - Test Circuit for Dynamic Characteristics

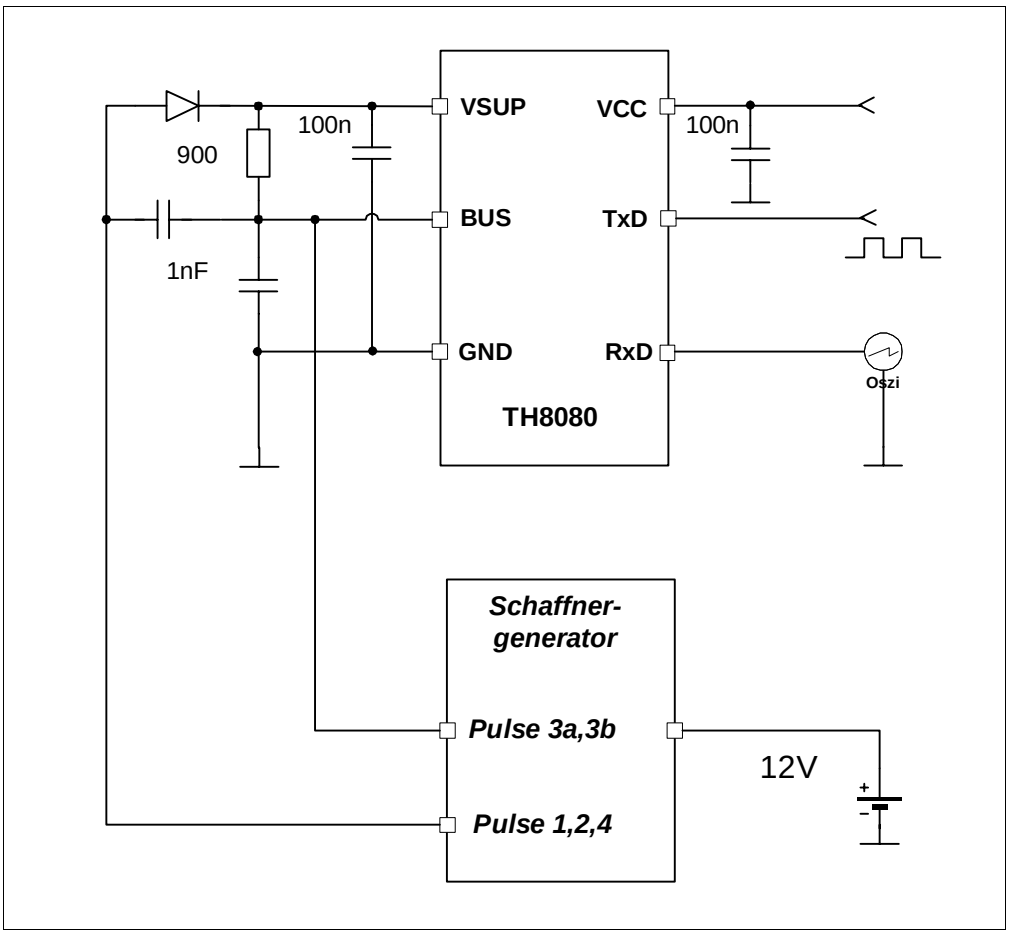
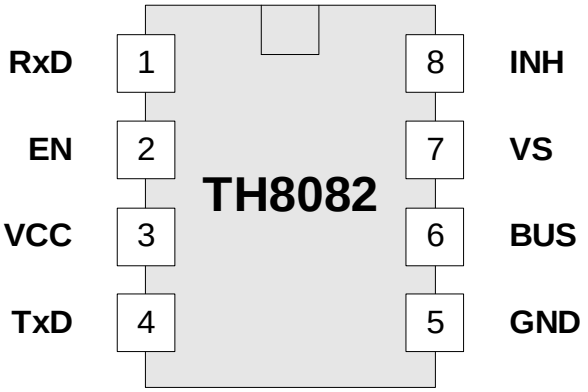


Figure 6 - Test Circuit for Automotive Transients

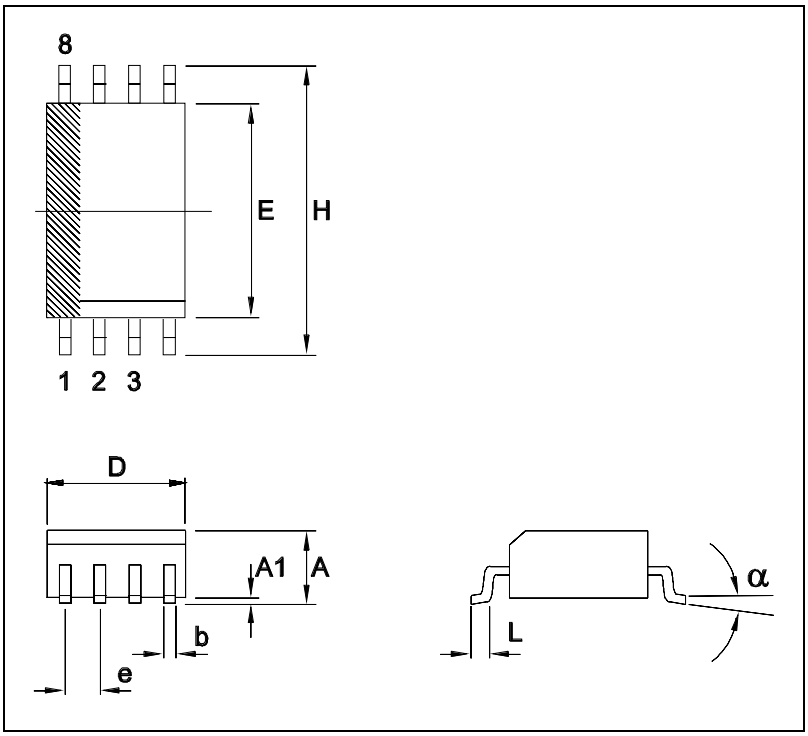
Pin Description



Pin	Name	I/O	Function
1	RXD	O	Receive data from BUS to core, LOW in dominant state
2	N.C.		
3	VCC		5V supply input
4	TXD	I	Transmit data from core to BUS, LOW in dominant state
5	GND		Ground
6	BUS	I/O	Single wire bus pin, LOW in dominant state
7	VS		Battery input voltage
8	N.C.		

Mechanical Specifications

SOIC8 Package Dimensions



Small Outline Integrated Circiut (SOIC), SOIC 8, 150 mil

All Dimension in mm, coplanarity < 0.1 mm									
	D	**E**	**H**	**A**	**A1**	**e**	**b**	**L**	**α**
min	4.8	3.80	10.00	5.80	0.10	1.27	0.33	0.40	0°
max	5.0	4.00	10.65	6.20	0.25		0.51	1.27	8°
All Dimension in inch, coplanarity < 0.004”									
min	0.189	0.150	0.228	0.053	0.004	0.050	0.013	0.016	0°
max	0.197	0.157	0.244	0.069	0.010		0.020	0.050	8°

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