TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

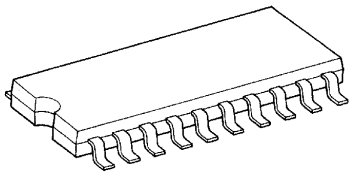
TC74LVX240F, TC74LVX240FW, TC74LVX240FT
TC74LVX244F, TC74LVX244FW, TC74LVX244FT

OCTAL BUS BUFFER
TC74LVX240 INVERTED, 3-STATE OUTPUTS
TC74LVX244 NON-INVERTED, 3-STATE OUTPUTS

The TC74LVX240 and 244 are high speed CMOS OCTAL BUS BUFFERs fabricated using silicon gate C^2MOS technology.
Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. These devices are suitable for low voltage and battery operated systems.
The TC74LVX240 is an inverting 3-state buffer while the TC74LVX244 is non-inverting. Both devices have two active-low output enables.
These devices are designed to be used in such applications as 3-state memory address drivers.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. These devices can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

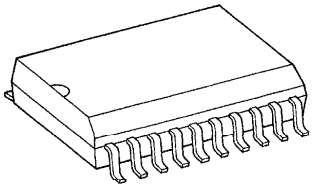
(Note) The JEDEC SOP (FW) is not available in Japan.

TC74LVX240F
TC74LVX244F



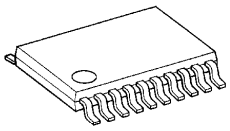
SOP20-P-300-1.27

TC74LVX240FW
TC74LVX244FW



SOL20-P-300-1.27

TC74LVX240FT
TC74LVX244FT



TSSOP20-P-0044-0.65

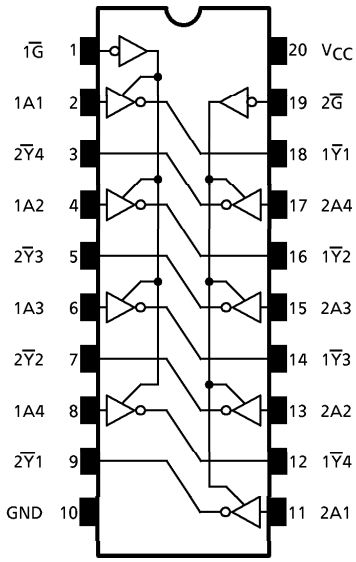
Weight
SOP20-P-300-1.27 : 0.22g (Typ.)
SOL20-P-300-1.27 : 0.46g (Typ.)
TSSOP20-P-0044-0.65 : 0.08g (Typ.)

FEATURES

- High speed : t_{pd} = 4.7ns (Typ.) (V_{CC} = 3.3V)
- Low power dissipation : I_{CC} = 4μA (Max.) (Ta = 25°C)
- Input voltage level : V_{IL} = 0.8V (Max.) (V_{CC} = 3V)
  V_{IH} = 2.0V (Min.) (V_{CC} = 3V)
- Power down protection is provided on all inputs.
- Balanced propagation delays : $t_{pLH} \simeq t_{pHL}$
- Low noise : V_{OLP} = 0.8V (Max.)
- Pin and function compatible with 74HC240 / 244

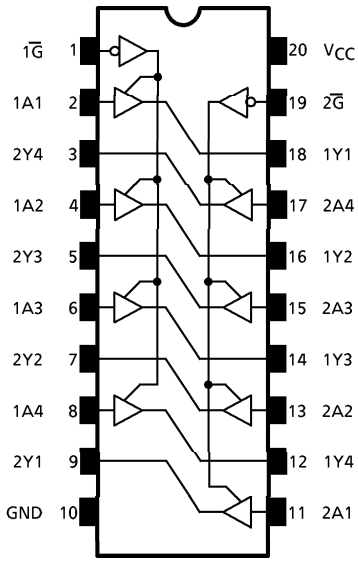
PIN ASSIGNMENT

TC74LVX240



(TOP VIEW)

TC74LVX244



(TOP VIEW)

TRUTH TABLE

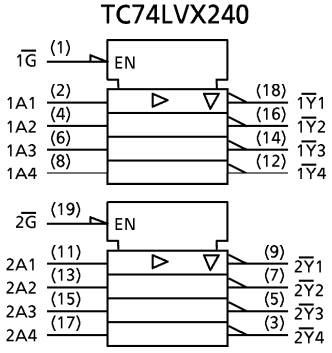
INPUTS		OUTPUTS	
$\overline{G}$	A_n	Y_n (244)	$\overline{Y}_n$ (240)
L	L	L	H
L	H	H	L
H	X	Z	Z

X : Don't Care

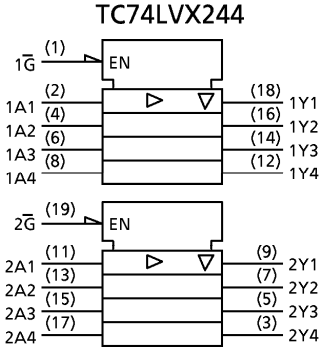
Z : High Inpedance

IEC LOGIC SYMBOL

TC74LVX240



TC74LVX244



961001EBA2'

MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYM-BOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
						MIN.	TYP.	MAX.	MIN.	MAX.	
Input Voltage	"H" Level	V_{IH}			2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					3.6	2.4	—	—	2.4	—	
	"L" Level	V_{IL}			2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output Voltage	"H" Level	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−50μA	2.0	1.9	2.0	—	1.9	—	V
				I_{OH}=−50μA	3.0	2.9	3.0	—	2.9	—	
				I_{OH}=−4mA	3.0	2.58	—	—	2.48	—	
	"L" Level	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=50μA	2.0	—	0.0	0.1	—	0.1	
				I_{OL}=50μA	3.0	—	0.0	0.1	—	0.1	
				I_{OL}=4mA	3.0	—	—	0.36	—	0.44	
3-State Output Off-State Current		I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		3.6	—	—	±0.25	—	±2.5	μA
Input Leakage Current		I_{IN}	V_{IN}=5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current		I_{CC}	V_{IN}=V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

AC characteristics (Input $t_r = t_f = 3ns$)

PARAMETER	SYM-BOL	TEST CONDITION	V_{CC} (V)	C_L (pF)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Propagation Delay Time (TC74LVX240)	t_{pLH} t_{pHL}		2.7	15	—	5.7	10.1	1.0	12.5	ns
				50	—	8.2	13.6	1.0	16.0	
			3.3 ± 0.3	15	—	4.3	6.2	1.0	7.5	
				50	—	6.8	9.7	1.0	11.0	
Propagation Delay Time (TC74LVX244)	t_{pLH} t_{pHL}		2.7	15	—	6.1	11.4	1.0	13.5	ns
				50	—	8.6	14.9	1.0	17.0	
			3.3 ± 0.3	15	—	4.7	7.1	1.0	8.5	
				50	—	7.2	10.6	1.0	12.0	
Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	2.7	15	—	7.1	13.8	1.0	16.5	ns
				50	—	9.6	17.3	1.0	20.0	
			3.3 ± 0.3	15	—	5.5	8.8	1.0	10.5	
				50	—	8.0	12.3	1.0	14.0	
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	2.7	50	—	11.6	16.0	1.0	19.0	ns
			3.3 ± 0.3	50	—	9.7	11.4	1.0	13.0	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Output Capacitance	C_{OUT}				—	6	—	—	—	pF
Power Dissipation Capacitance (Note 3)	C_{PD}	TC74LVX240			—	17	—	—	—	pF
		TC74LVX244			—	19	—	—	—	

(Note 1) Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

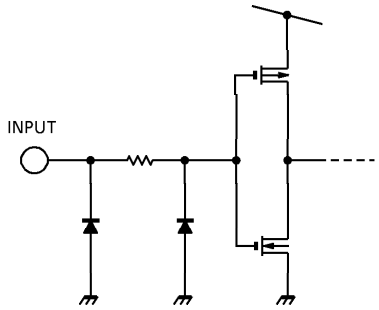
(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation :
$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per bit)

Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

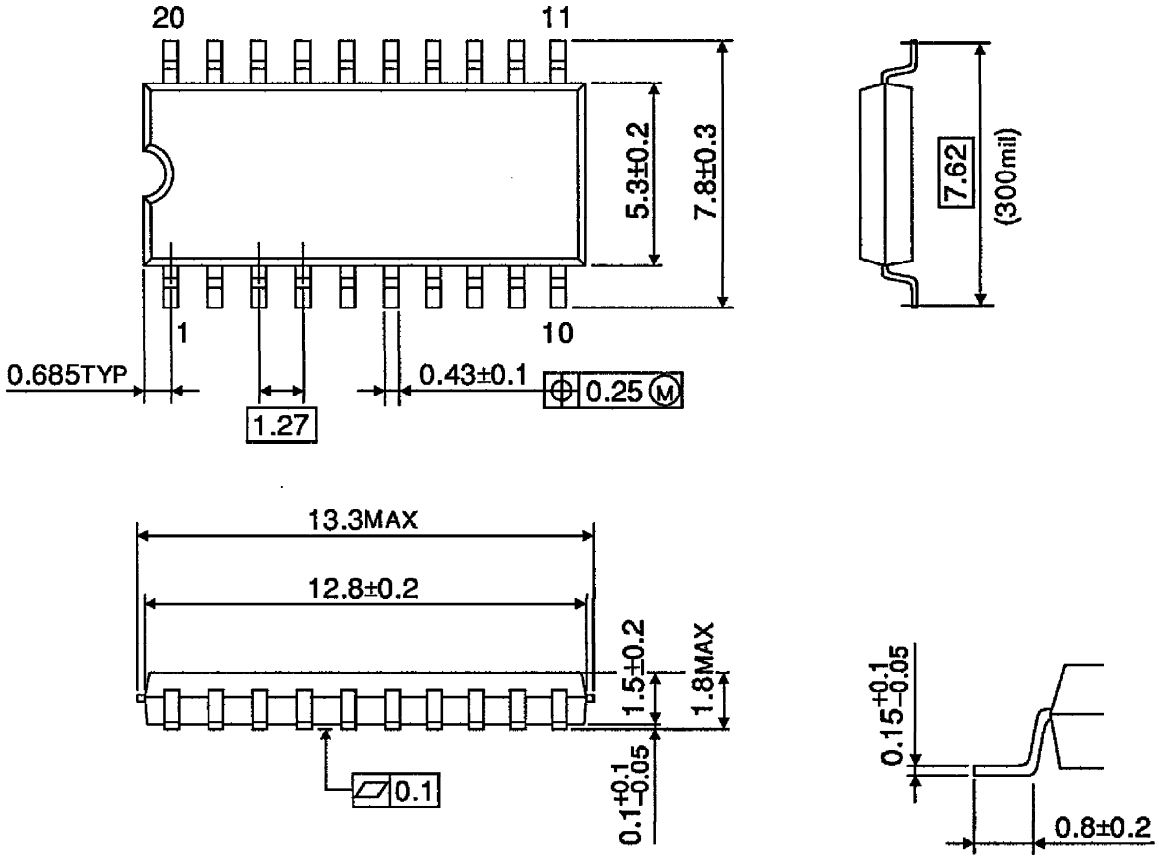
INPUT EQUIVALENT CIRCUIT



OUTLINE DRAWING

SOP20-P-300-1.27

Unit : mm

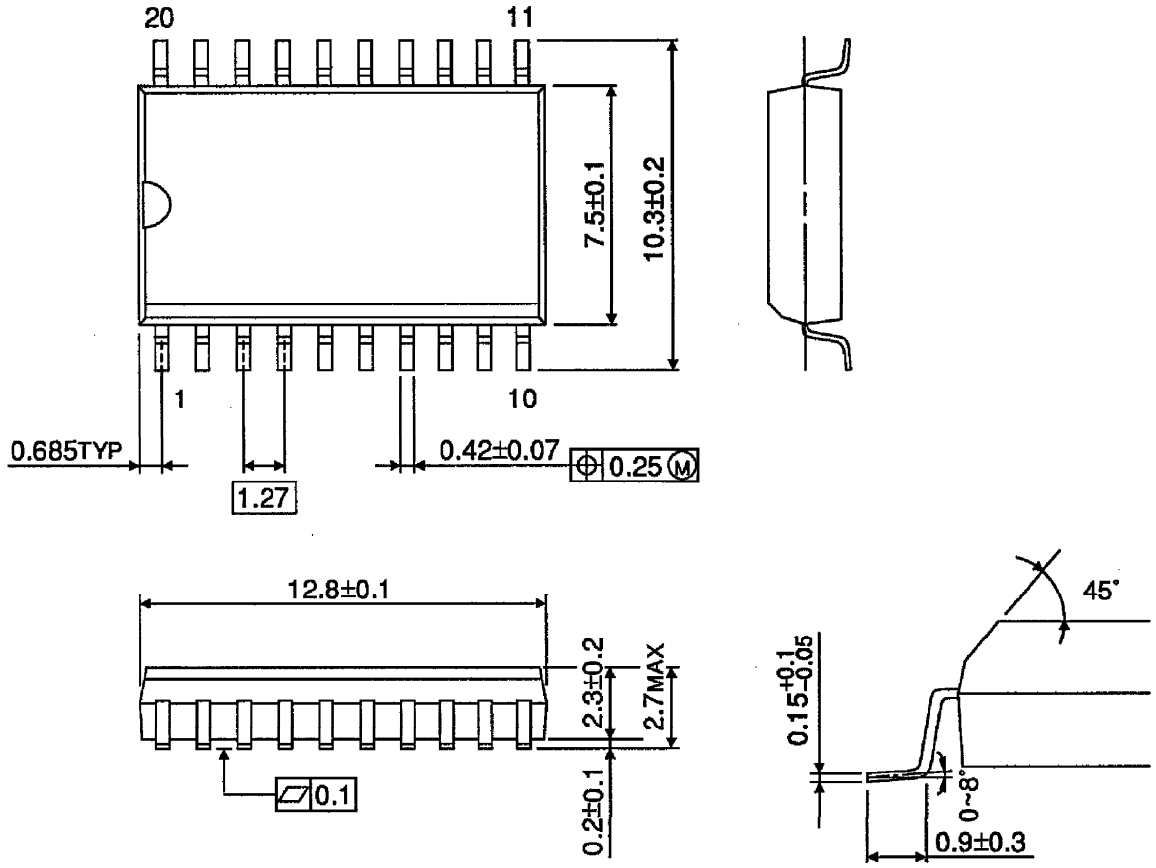


Weight : 0.22g (Typ.)

OUTLINE DRAWING

SOL20-P-300-1.27 Unit : mm

(Note) This package is not available in Japan.

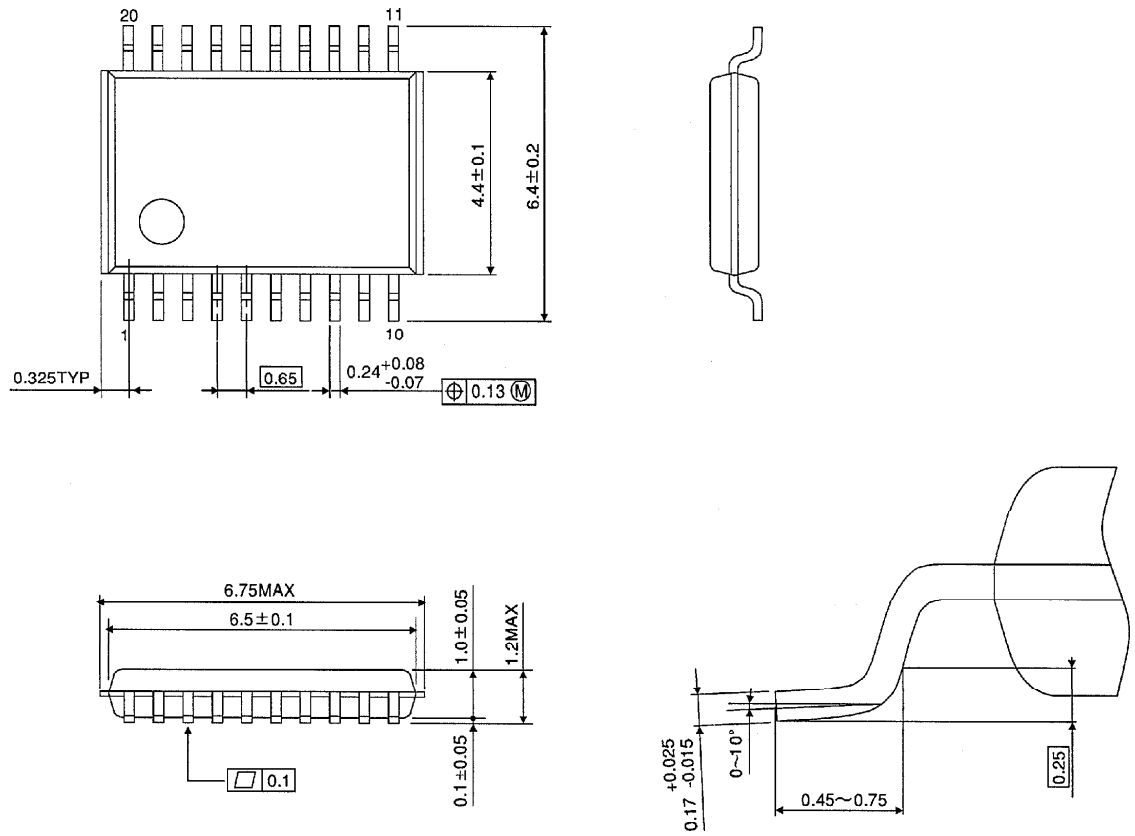


Weight : 0.46g (Typ.)

OUTLINE DRAWING

TSSOP20-P-0044-0.65

Unit : mm



Weight : 0.08g (Typ.)