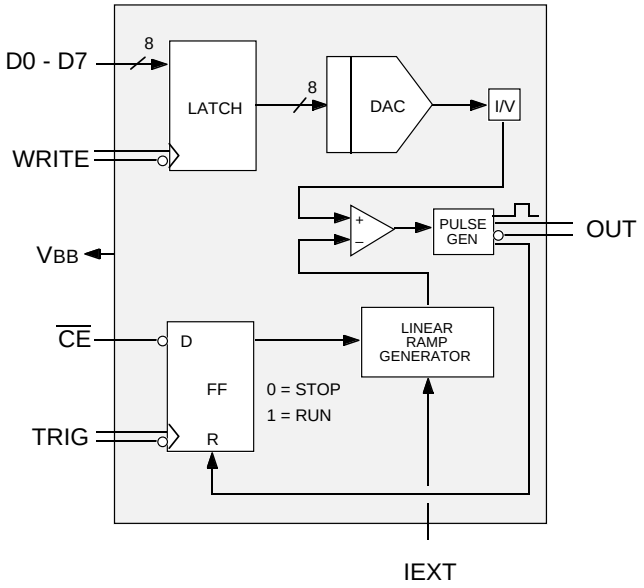
125MHz WRITE PROGRAMMABLE TIMING EDGE VERNIER

SY605

FEATURES

- **True 125MHz retrigger rate**
- **Pin-compatible with Bt605**
- **15ps delay resolution**
- **Less than ± 1 LSB timing accuracy**
- **Differential TRIGGER and delay WRITE inputs**
- **Delay spans from 4 to 40ns**
- **Compatible with 10KH ECL logic**
- **Lower power dissipation 350mW typical**
- **Available in 28-pin plastic (PLCC) or metal (MLCC) J-lead package**

BLOCK DIAGRAM



DESCRIPTION

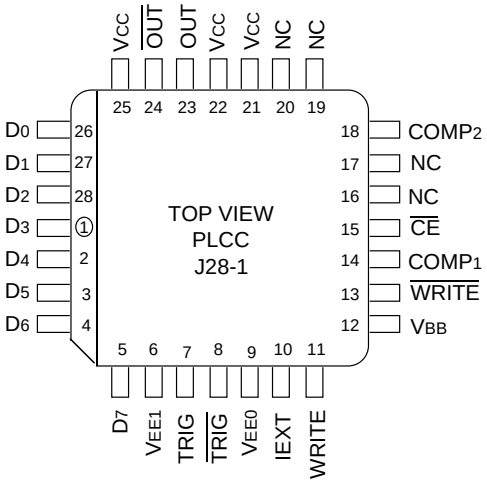
Micrel-Synergy's SY605 is an ECL-compatible timing vernier (delay generator) whose time delay is programmed via an 8-bit code which is loaded via an independent "WRITE" input. The SY605 is fabricated in Micrel-Synergy's proprietary ASSET™ bipolar process.

This device can be retriggered at speeds up to 125MHz, with a delay span as short as 4ns. At minimum span, the resolution is 4ns/255 = 15.7ps per step. The delay span is externally adjustable up to 40ns. The SY605 employs differential TRIGGER and WRITE inputs, and produces a differential OUTPUT pulse; all other control signals are single-ended ECL. Edge delay is specified by an 8-bit input which is loaded into the device with the WRITE signal. The output pulse width will typically be 3.5ns.

The SY605 is commonly used in Automatic Test Equipment to provide precise timing edge placement; it is also found in many instrumentation and communications applications.

Micrel-Synergy's circuit design techniques coupled with ASSET™ technology result in not only ultra-fast performance, but allow device operation at lower power dissipation than competing technologies. Outstanding reliability is achieved in volume production.

PIN CONFIGURATION



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PIN DESCRIPTION

D0 – D7
Data input pins (ECL compatible). On the falling edge of WRITE, D0 - D7 are latched into the DAC input register. D0 is the LSB. These inputs specify the amount of delay from the rising edge of TRIG to the output pulse.

WRITE, $\overline{\text{WRITE}}$
Differential write inputs (ECL compatible). These inputs control the parallel data input latch. When WRITE is a logical one, the data latch is transparent. Data is latched on the falling edge of WRITE. A single-ended write may be used by connecting $\overline{\text{WRITE}}$ to V_{BB}.

$\overline{\text{CE}}$
Chip enable input (ECL compatible). $\overline{\text{CE}}$ must be a logical zero on the rising edge of TRIG to enable the device to respond to the trigger. If $\overline{\text{CE}}$ is floating, the trigger will always be enabled.

TRIG, $\overline{\text{TRIG}}$
Differential trigger inputs (ECL compatible). The rising edge of TRIG is used to trigger the delay cycle if $\overline{\text{CE}}$ is a logical zero. If $\overline{\text{CE}}$ is a logical one, no operation occurs. It is recommended that triggering be performed with differential inputs.

OUT, $\overline{\text{OUT}}$
Differential outputs (ECL compatible).

IEXT
Current reference pin. The amount of current sourced into this pin determines the span of output delay. The voltage at IEXT is typically –1.25V.

COMP1, COMP2
Compensation pins. A 0.1µF ceramic capacitor must be connected between COMP1 and V_{EE0}, and COMP2 and V_{EE0} (see Figure 3).

V_{EE}
Device power. All V_{EE} pins must be connected.

V_{CC}
Device ground. All V_{CC} pins must be connected together.

V_{BB}
A –1.36V (typical) output.

FUNCTIONAL DESCRIPTION

The output pulse generation cycle begins with the arrival of TRIG shown in **Figure 1**. The DAC values are latched by the rising edge of WRITE. Then, when TRIG transitions to a high and $\overline{\text{CE}}$ is low the linear ramp is initiated.

When the ramp level reaches that of the DAC, the comparator initiates the pulse generator to produce an output pulse resets the ramp and the cycle is ready to begin again.

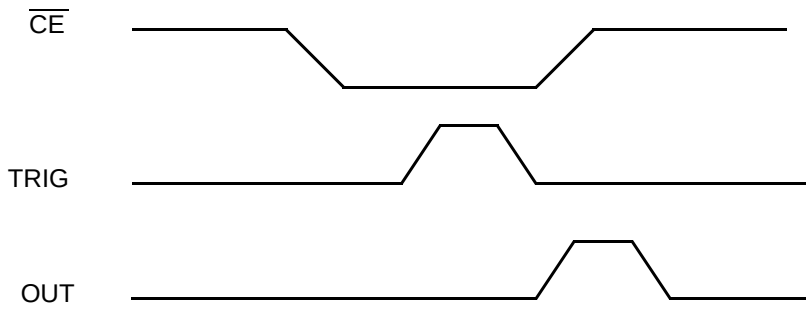


Figure 1.

ABSOLUTE MAXIMUM RATING[1]

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8 to 0	V
V_I	Input Voltage (V_{CC} = 0V)	0 to V_{EE}	V
I_{OUT}	Output Current — Continuous — Surge	 50 100	mA
T_A	Operating Temperature Range	0 to +85	°C
V_{EE}	Operating Range[2]	–5.7 to –4.2	V

NOTES:

1. Beyond which device life may be impaired.
2. Parametric values specified at 10E Series: –4.75V to –5.5V

DC CHARACTERISTICS

Symbol	Parameter	T_A = +0°C			T_A = +25°C			T_A = +70°C			Unit
		Min.	Typ.	Max.	MIn.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage (10K)	-1170	—	-840	-1130	—	-810	-1070	—	-735	mV
V_{IL}	Input LOW Voltage (10K)	-1950	—	-1480	-1950	—	-1480	-1950	—	-1450	mV
V_{OH}	Output HIGH Voltage (10K)	-1020	-975	-840	-980	-920	-810	-920	-850	-735	mV
V_{OL}	Output LOW Voltage (10K)	-1950	-1755	-1630	-1950	-1750	-1630	-1950	-1720	-1600	mV
I_{IH}	Input High Current (Vin = V_{IH} max)	—	100	150	—	100	150	—	100	150	µA
I_{IH}	TRIG, $\overline{TRIG}$	—	100	150	—	100	150	—	100	150	µA
I_{IL}	Input Low Current (Vin = V_{IL} min)	—	100	150	—	100	150	—	100	150	µA
I_{IL}	TRIG, $\overline{TRIG}$	—	100	150	—	100	150	—	100	150	µA
	Output Delay Spans										
D_L	Differential Linearity Error**	—	±0.84	±0.9	—	±0.84	±0.9	—	±0.84	±0.9	LSB
I_L	Integral Linearity Error**	—	±1.16	±1.25	—	±0.89	±1.0	—	±0.89	±1.0	
V_{BB}	V_{BB} Output Voltage	-1.44	—	-1.25	-1.44	-1.35	-1.25	-1.44	—	-1.25	V
I_{EXT}	I_{EXT} for Tspans										
	Tspan = 4ns	1.80	2.38	2.80	1.80	2.38	2.80	1.80	2.38	2.80	mA
	Tspan = 5ns	1.45	1.85	2.40	1.45	1.85	2.40	1.45	1.85	2.40	mA
	Tspan = 10ns	0.70	0.93	1.20	0.70	0.93	1.20	0.70	0.93	1.20	mA
	Tspan = 15ns	0.45	0.62	0.80	0.45	0.62	0.80	0.45	0.62	0.80	mA
	Tspan = 20ns	0.34	0.46	0.60	0.34	0.46	0.60	0.34	0.46	0.60	mA
	Tspan = 30ns	0.20	0.30	0.40	0.20	0.30	0.40	0.20	0.30	0.40	mA
	Tspan with I_{EXT} = 1.8 mA										
	(Tspan = Tmax - Tmin)	4.1	—	6.5	4.1	—	6.5	4.1	—	6.5	ns
Tmin	Minimum Delay Time*										
	Data = 00, Tspan = 5ns	—	2.8	3.8	—	2.8	3.8	—	2.8	3.8	ns
	Tspan = 10ns	—	3.4	4.9	—	3.4	4.9	—	3.4	4.9	ns
	Tspan = 15ns	—	4.0	6.0	—	4.0	6.0	—	4.0	6.0	ns
	Tspan = 20ns	—	4.6	7.1	—	4.6	7.1	—	4.6	7.1	ns
	Tspan = 25ns	—	5.2	8.2	—	5.2	8.2	—	5.2	8.2	ns
	Tspan = 30ns	—	5.8	9.3	—	5.8	9.3	—	5.8	9.3	ns
I_{EE}	V_{EE} Supply Current	—	—	100	—	70	100	—	—	100	mA

NOTE:

1. 10K series circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts.

AC CHARACTERISTICS

ECL input values are -0.9 to -1.7V, with input rise/fall times ≤ 2ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. OUT and $\overline{OUT}$ loading with 50Ω to -2.0V. Typical values are based on nominal temperature, i.e., and nominal voltage, i.e., - 5.2V.

Symbol	Parameter	T_A = +0°C			T_A = +25°C			T_A = +70°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{MAX}	Trigger Rate[1]	—	—	125	—	—	125	—	—	125	MHz
t_{WI}	Trigger Width High	2.0	1.0	—	2.0	1.0	—	2.0	1.0	—	ns
t_{WO}	Output Pulse Width High Time	2.5	3.5	4.5	2.5	3.5	4.5	2.5	3.5	4.5	ns
	Output Pulse Rise/Fall Time (20/80%)	—	550	750	—	550	750	—	550	750	ps
t_S	Output Pulse Spacing										
	Span = 4ns @ 1 LSB	8.0	—	—	8.0	—	—	8.0	—	—	ns
	Minimum Delay Time vs. Tspan										
	Δ T00 / ns (Tspan = 5 to 10ns)	—	125	220	—	125	220	—	125	220	ps/ns
	Output Delay										ns
1 LSB	Tspan (Tspan = Tmax - Tmin)	4.0	—	40	4.0	—	40	4.0	—	40	ns
1 LSB	Resolution (Tspan / 225)	15.7	—	157	15.7	—	157	15.7	—	157	ps
	Tempo (5ns Span)										
	Δ Tspan /°C	—	2	—	—	2	—	—	2	—	ps/°C
	Δ Tmin /°C	—	2	—	—	2	—	—	2	—	ps/°C
	Power Supply Rejection	—	60	—	—	60	—	—	60	—	ps/V
	(Data = 0-FF HEX, Tspan = 5ns)										
t_S	$\overline{CE}$ Setup Time	2.0	—	—	2.0	—	—	2.0	—	—	ns
t_H	$\overline{CE}$ Hold Time	1.5	—	—	1.5	—	—	1.5	—	—	ns
t_{WH}	WRITE Pulse Width High Time	2.0	—	—	2.0	—	—	2.0	—	—	ns
t_{DS}	D0 - D7 Setup Time	1.0	—	—	1.0	—	—	1.0	—	—	ns
t_{DH}	D0 - D7 Hold Time	1.5	—	—	1.5	—	—	1.5	—	—	ns

NOTE:

1. See chart below:

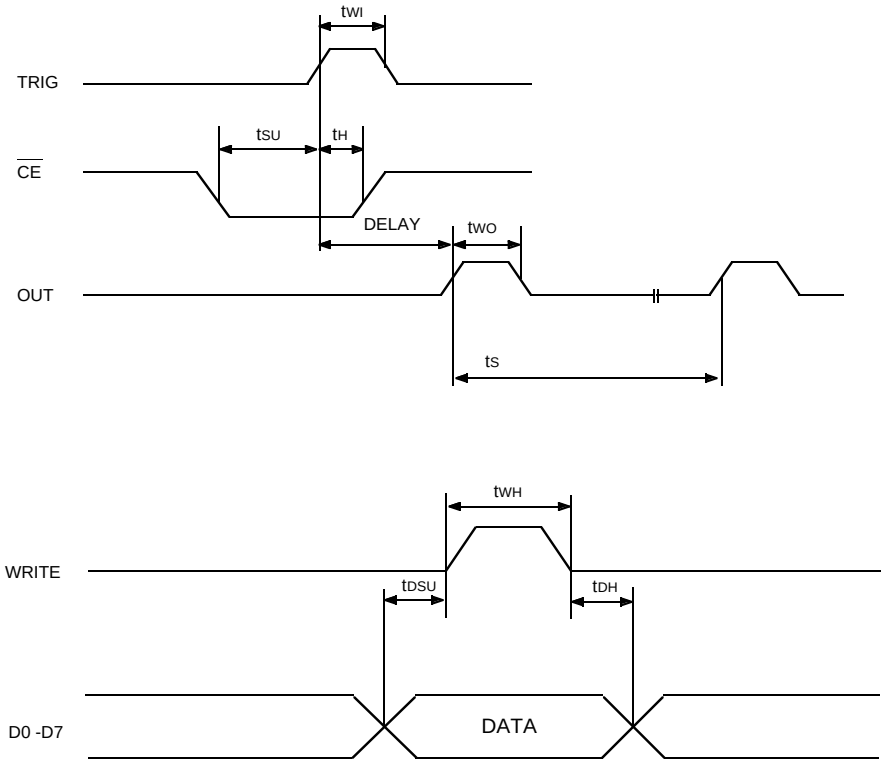
Maximum Tspan and Trigger Rates

Maximum Tspan (ns) Maintaining Linearity of ±1 LSB	Minimum Trigger Periods (ns)
4.0	8.0
5.1	10.0
5.8	11.1
6.75	12.5
8.1	14.3
9.9	16.6
12.0	20.0
15.5	25.0
22.0	33.3

The information in this table is guaranteed but not 100% production tested.

See **Figure 2** for a graphical representation.

TIMING DIAGRAMS



± 1 LSB
Span vs. Trigger Rates

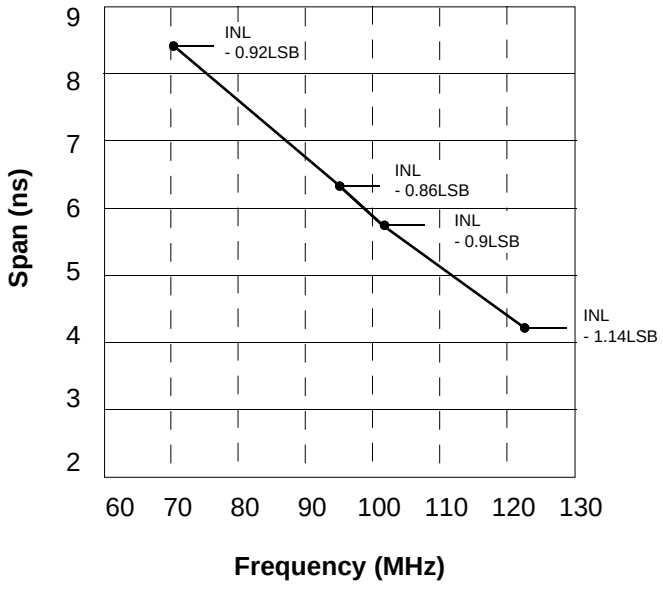
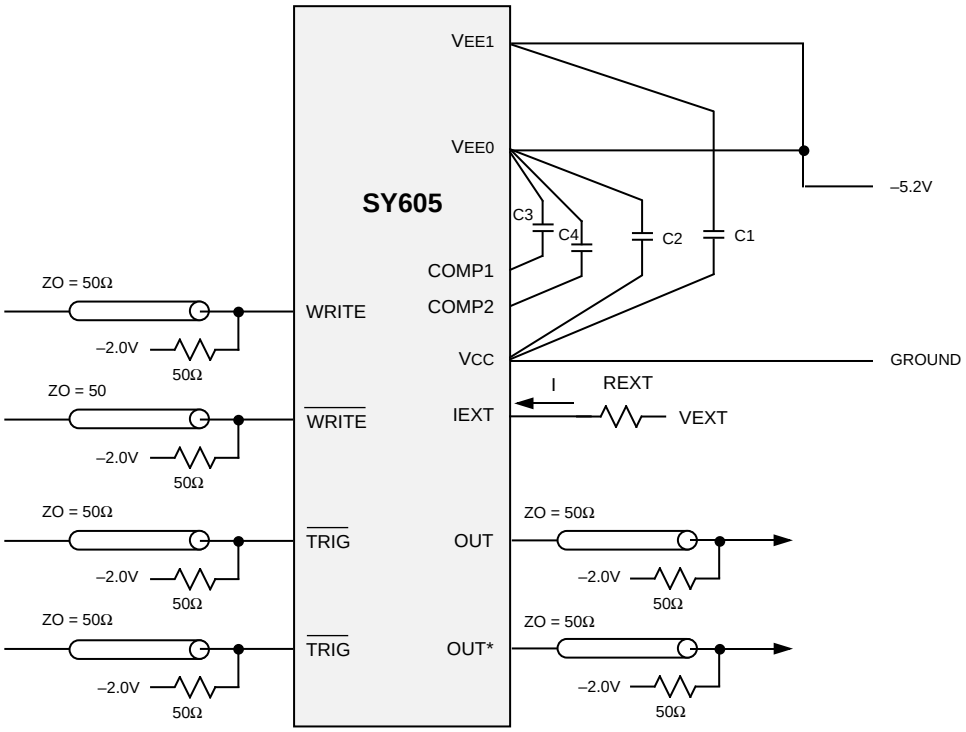


Figure 2.

APPLICATION DIAGRAM



REXT Calculation:

REXT = (VEXT + 1.25V)/IEXT

For Example:

If Tspan is around 15ns, then IEXT is around 0.6mA, (see DC Characteristic Table) and assume IEXT pin is tied to VCC with the resistor.

REXT = 0 + 1.25V/0.6mA

= 2.08K ohm

Location	Description	Vendor Part Number
C1–C4	0.1µF ceramic capacitor	Erie RPE112Z5U104M50V
REXT	1% metal film resistor (selected for proper Tspan)	CB301210 Dale CMF-55C

NOTE:

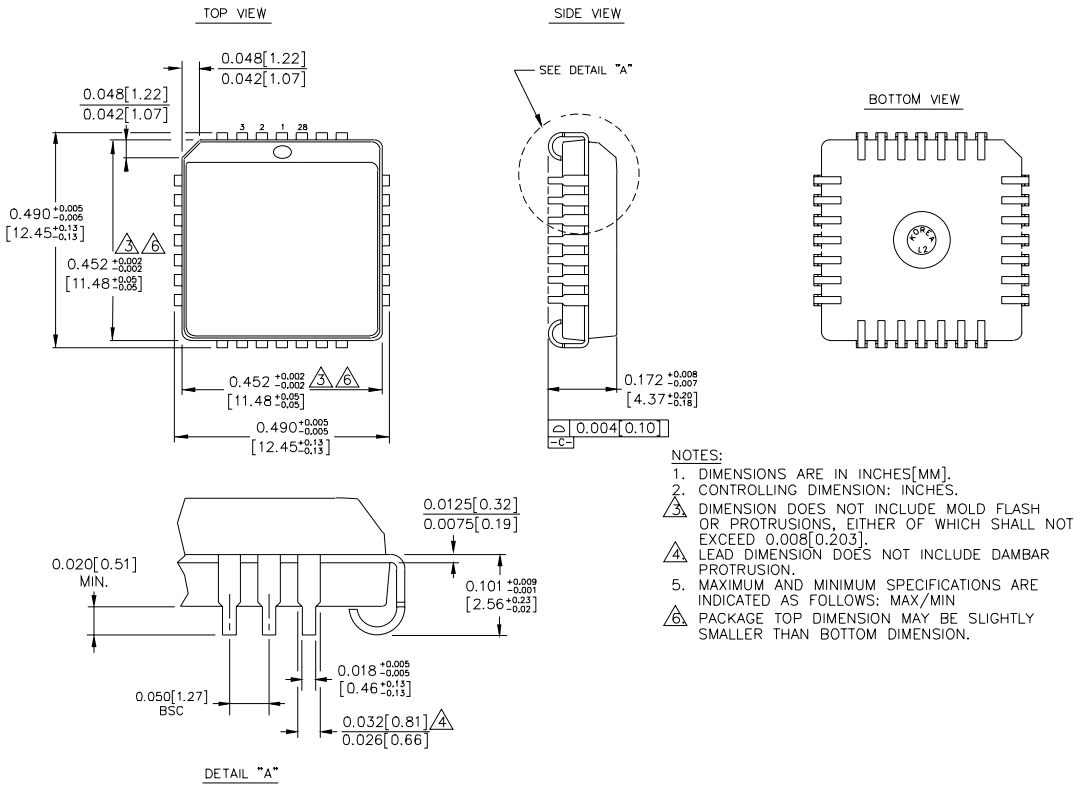
The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the SY605. All devices should be as close as possible to the SY605.

Figure 3. Typical Connection Diagram and Parts List.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY605JC	J28-1	Commercial
SY605JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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