FAIRCHILD

SEMICONDUCTOR®

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MSX532
532 Port Digital Crosspoint Switch with LVTTL I/O's

General Description

The MSX™ family of SRAM-based bit-oriented switching devices offer flow-through NRZ data rates of up to 150Mb/s and registered clock frequencies of up to 75MHz. The I/O buffers are individually configurable. The I/O buffers can be connected to each other through the switch matrix, which supports One-to-One and One-to-Many connections.

The proprietary RapidConfigure™ parallel interface allows fast configuration of both the I/O buffers and switch matrix. It also allows readback of the device for test and verification purposes. The MSX devices also support the industry standard JTAG (IEEE 1149.1) interface for boundary scan testing. The JTAG interface can also be used to download configuration data to the device. A functional block diagram of the MSX architecture is shown in Figure 1.

Features

■ SRAM-based, in-system programmable
■ Configurable I/O Ports
  • Individually programmable as input, output, bi-directional, or Bus Repeater™ mode
  • Control Signals per I/O port: 2 input enables, 2 output enables, 2 Global Clock inputs and Next Neighbor Clock option
  • Output data inversion: capable of inverting output signals in flow through mode
■ Non-blocking switch matrix
  • One-to-One and One-to-Many connections Double-buffered configuration RAM cells for simultaneous global updates
■ Registered and flow-through data modes
  • Up to 75 MHz clock frequency in registered mode
  • Up to 150 Mb/s in flow-through mode
■ 20 ns propagation delay in flow-through mode
■ 8 mA output current
■ Dedicated RapidConfigure parallel interface or JTAG serial interface available for configuration and readback of MSX devices
■ 3.3V operation, LVTTL I/O's (5V tolerant)
■ MSX532 is offered in a 792 TBGA package

Applications

• Telecom and datacom switching
• Video switches and servers
• Test equipment

Ordering Code:

Order Number	Package Number	Package Description
MSX532TB792	BGA792A	792-Ball Thermally-Enhanced Ball Grid Array (TBGA), JEDEC MO-149, 1.0mm pitch, 40mm Square

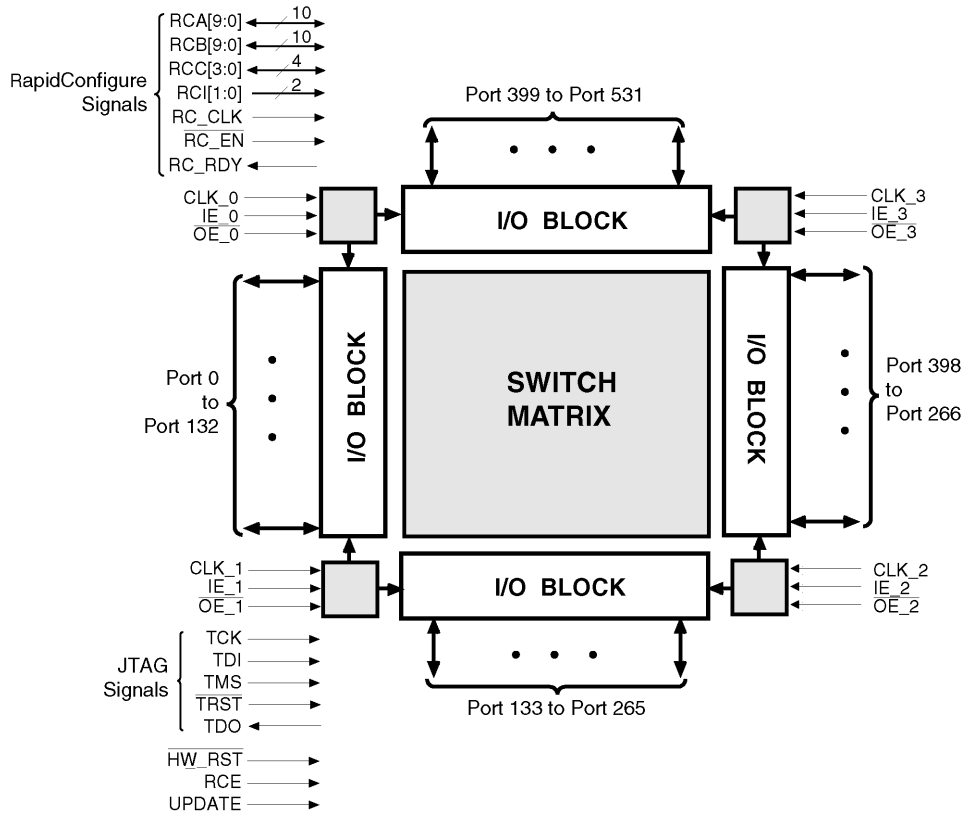MSX™, Bus Repeater™, and RapidConfigure™ are trademarks of Fairchild Semiconductor Corporation.

FIGURE 1. MSX532 Functional Block Diagram

Introduction

Switch Matrix

The MSX family are SRAM-based, bit-oriented switching devices. The main functional block of the device is a Switch Matrix as shown in Figure 1. The Switch Matrix is an x-y routing structure (or grid). Each horizontal signal trace is hardwired to a corresponding vertical signal trace as shown by the junction dots. An I/O Port pin connects to this horizontal-vertical trace pair through a programmable buffer. Signal paths through the Switch Matrix are well balanced, resulting in predictable and uniform pin-to-pin delays.

The two SRAM cells (shown in Figure 2) are arranged so that a double buffered scheme can be employed. The Active SRAM cells are responsible for establishing connections in the switch matrix by turning ON a pass transistor, while the Loading SRAM cell can be used to store a second configuration that can be transferred to the Active SRAM cell at any time. If the UPDATE signal is asserted HIGH, the contents of the Loading SRAM cell are transferred to the Active SRAM cell and the switch matrix connection is either made or broken.

The UPDATE signal can be used to control when the switch matrix is reconfigured. For instance, as long as the UPDATE signal is de-asserted (held LOW), the Loading SRAM cells for the entire switch matrix could be changed

without affecting the current configuration of the switch. When the UPDATE signal is asserted HIGH, the entire switch matrix would be reconfigured simultaneously. If the UPDATE signal is asserted continuously, all crosspoint programming commands (generated by JTAG or RapidConfigure programming cycles) will take effect immediately, since the Loading SRAM cell's contents will be transferred directly to the Active SRAM cell.
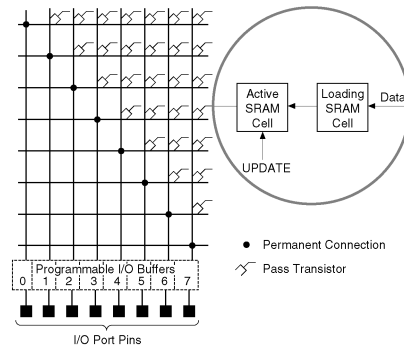

FIGURE 2. MSX Switch Matrix Diagram

Introduction (Continued)

Input and Output Buffers (I/O buffers)

Each signal in the switch matrix is connected to a programmable I/O buffer, which is independently configured through either the RapidConfigure or JTAG Interface. The I/O buffer attributes include its signal direction (input, output or bi-directional) and data flow mode (flow-through or registered). The signal can also be inverted at the output. Trickle current source (normally 15 μA) on the pin side and array side for each I/O Port and control pin is used to pull unused or non-driven circuits to a stable HIGH level. Figure 3 shows a basic block diagram of an I/O buffer with the sources for the three control signals (IE, OE and CLK). For any given port number, these three control signals can be selected from one of two sources. The control signals are explained in more detail in the following section.
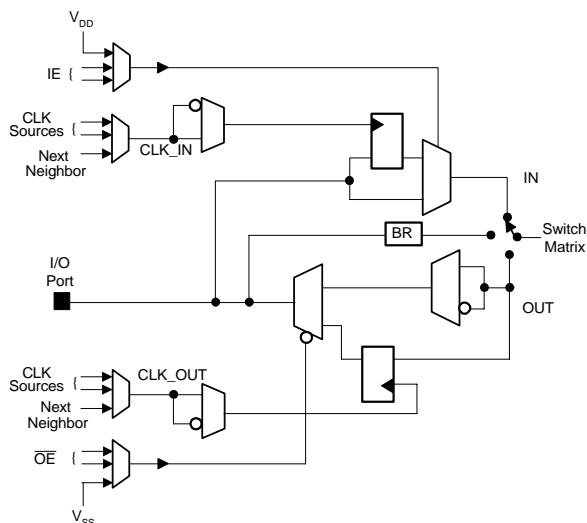

FIGURE 3. MSX I/O Buffer Block Diagram

I/O Port Function Mode

The following legend describes the various modes of the Input or Output Ports and the specification used by the Fairchild Development System Software for bitstream generation.

Legend:

Ax   = Switch Matrix Signal
Px   = I/O Port Signal
IE   = Input Enable
$\overline{\text{OE}}$ = Output Enable (Active LOW)
CLK = Clock

Next-Neighbor Clocking

Included among the clocking options in MSX532 is the ability to use an adjacent port as a clock source. This is referred to as a Next-Neighbor Clock. In the MSX532, Port 0 can be clocked by Port 1, which can be clocked by Port 2, which can be clocked by Port 3, etc. In turn, Port 531 can be clocked by Port 0. Since each I/O buffer can be programmed as an input or an output (among other options) there are four ways to utilize the next neighbor clock option.

Introduction (Continued)

Option 1: Registered Input with Next-Neighbor Clock as Input
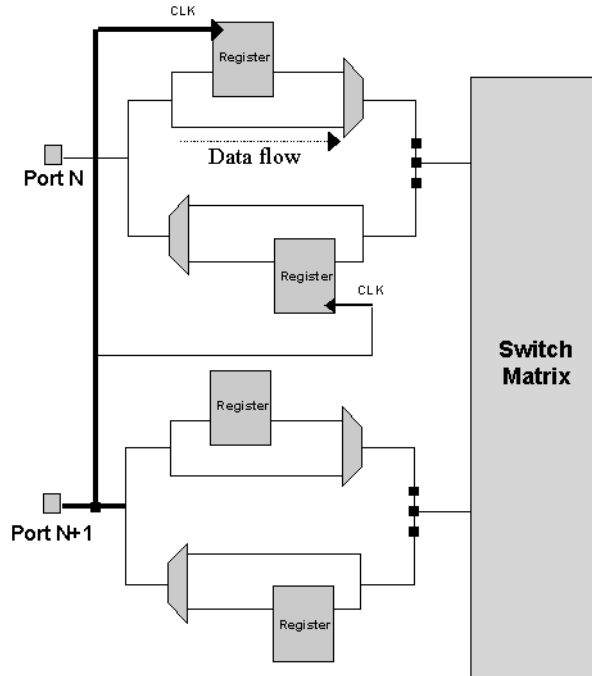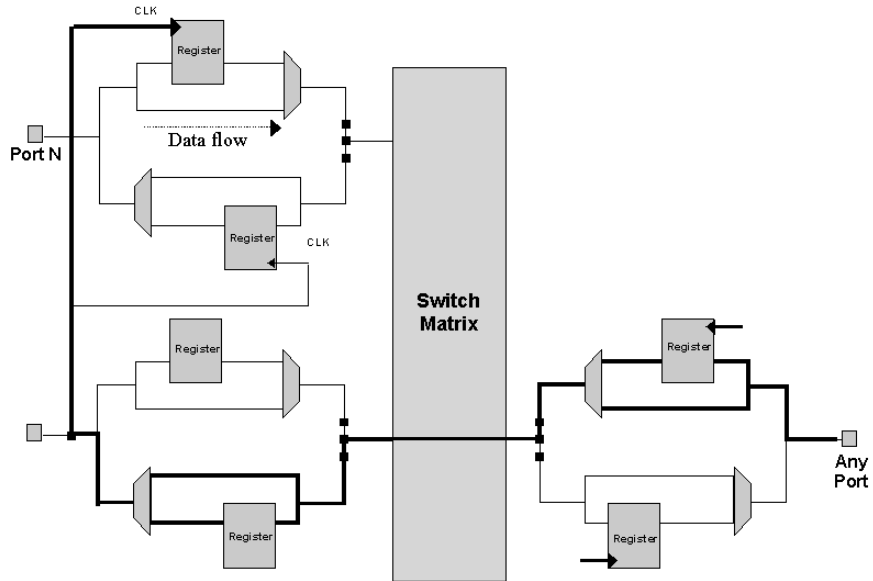

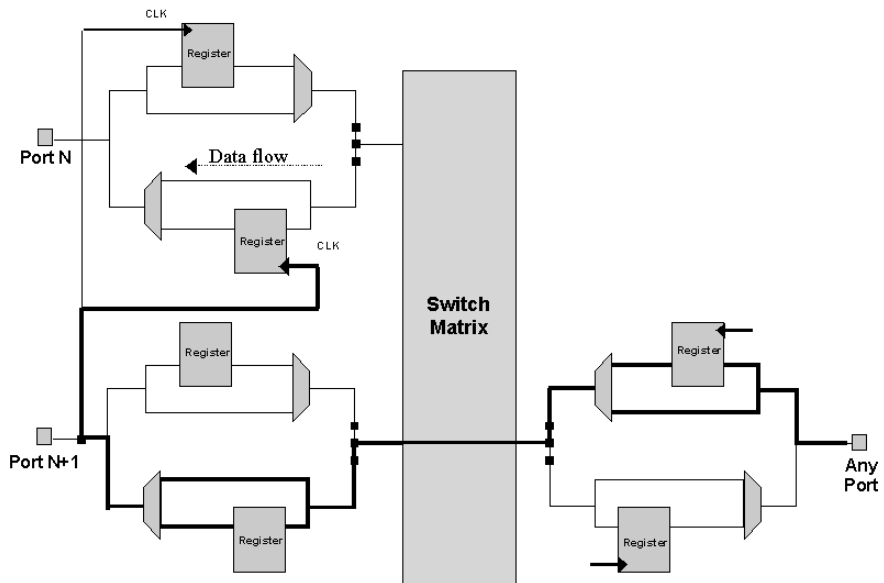**Option 2: Registered Output with Next-Neighbor Clock as Input**
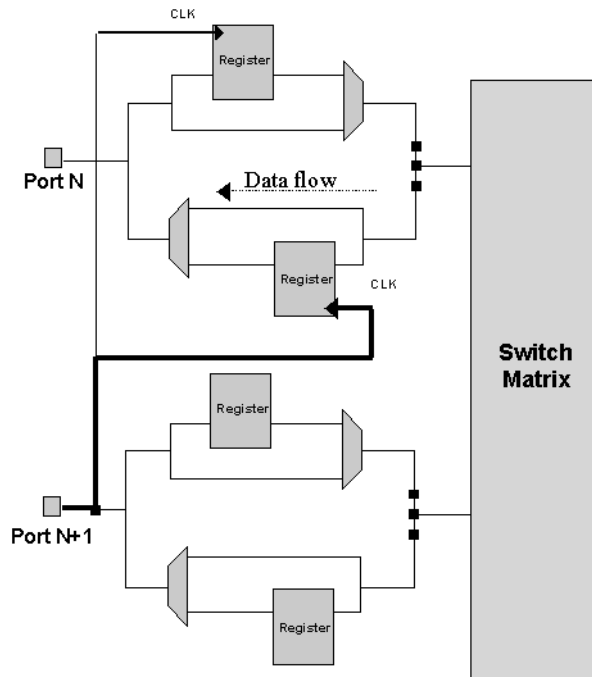
Introduction (Continued)

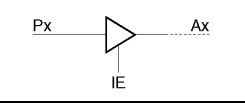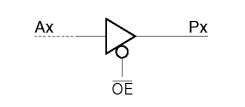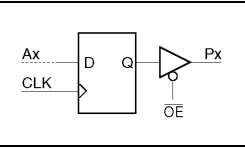**Option 3: Registered Input with Next-Neighbor Clock as Output**
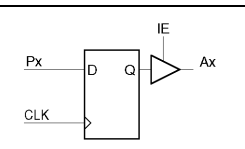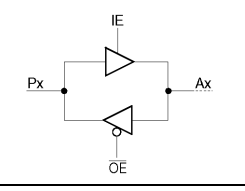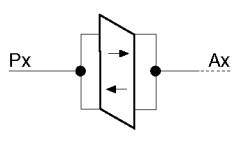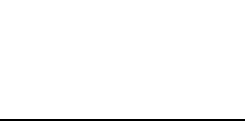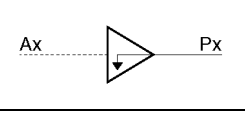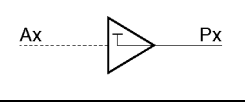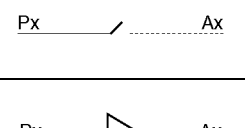
Option 4: Registered Output with Next-Neighbor Clock as Output

Introduction (Continued)

TABLE 1. Summary for Programmable I/O Attributes for MSX Devices

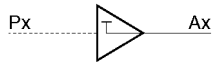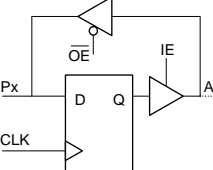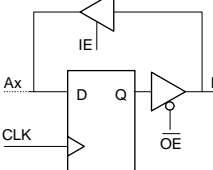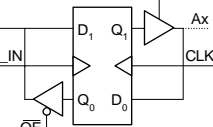| Symbol	I/O Port Function		Mnemonic
Px ▷ Ax IE	Input	The external signal is buffered from the Input Port pin to the corresponding Switch Matrix line.	IN
Ax ▷ Px $\overline{OE}$	Output	The internal signal is buffered from the corresponding Switch Matrix line to the Output Port pin. In this mode an optional output enable ($\overline{OE}$) can be selected. The default level is logic 0. The output data inversion mode is available to invert the output signal.	OP
IE Px → D Q → Ax CLK	Registered Input	The external signal at the I/O Port is registered into an edge-triggered register within the I/O Port. A clock source is required in this mode. An input enable (IE) is available but not required.	RI
Ax → D Q → Px CLK $\overline{OE}$	Registered Output	The internal signal on the Switch Matrix line is registered by an edge-triggered register within the I/O Port. A clock source is required in this mode. An output enable ($\overline{OE}$) is available but not required. The output data inversion mode is NOT available to invert the output signal.	RO
IE Px ▷ Ax ◁ $\overline{OE}$	Bidirectional Transceiver	In this mode, the I/O buffer acts as a bidirectional transceiver between the I/O Port pin and the corresponding Switch Matrix line. This mode requires an input enable (IE) and output enable ($\overline{OE}$). The output data inversion mode is available to invert the output signal.	BT
Px ◁▷ Ax	Bus Repeater	In the Bus Repeater mode, the I/O Port behaves as a wire (with a non-zero propagation delay). This unique feature patented by Fairchild incorporates as self-sensing circuit to determine signal direction and does not require a direction control signal. When multiple I/O Ports, configured as "Bus Repeater", are connected together through the Switch Matrix to form a single internal node, any (open collector or 3-STATABLE) LOW (logic "0") external signal appearing at any one of the I/O Ports gets repeated (or broadcast) to other I/O Ports. For more details, refer to the Technical Note: "The Bus Repeater Mode"	BR
Ax ▷ Px	Pin Side Force 0	In this output mode, the I/O Port pin is forced LOW (logic 0), regardless of the signal on the corresponding switch Matrix line. In this mode an optional output enable ($\overline{OE}$) can be selected.	F0
Ax ▷ Px	Pin Side Force 1	In this output mode, the I/O Port pin is forced HIGH (logic 1), regardless of the signal on the corresponding Switch Matrix line. In this mode an optional output enable ($\overline{OE}$) can be selected.	F1
Px / Ax	No Connect	In this mode, the I/O Port pin is isolated from the Switch Matrix. This is done by 3-STATING both the input and output part of the I/O buffer.	NC
Px ◁ Ax	Array Side Force 0	In this input mode, the Switch Matrix line is forced LOW (logic 0), regardless of the signal on the corresponding I/O Port. In this mode an optional input enable (IE) can be selected.	A0

Introduction (Continued)

Px ▷ Ax	Array Side Force 1	In this input mode, the Switch Matrix line is forced HIGH (logic 1), regardless of the signal on the corresponding I/O Port. In this mode an optional input enable (IE) can be selected.	A1
Px — D Q — Ax, OE, IE, CLK	Bidirectional Transceiver with Register Input	This mode combines Registered Input and buffered Output (OP). This mode requires a clock source (CLK), and input enable (IE) and output enable ($\overline{OE}$).	BT & RI
Ax — D Q — Px, IE, CLK, OE	Bidirectional Transceiver with Register Output	This mode combines Registered Output (RO) and buffered Input (IE). This mode requires a clock source (CLK), and input enable (IE) and output enable ($\overline{OE}$). The output data inversion mode is NOT available to invert the output signal.	BT & RO
Px — D_1 Q_1 — Ax, CLK_IN, CLK_OP, Q_0 D_0, IE, $\overline{OE}$	Bidirectional Transceiver with Register I/O	This mode combines Registered Input (RI) and Registered Output (RO). This mode requires a clock source (CLK), and input enable (IE) and output enable ($\overline{OE}$). The output data inversion mode is NOT available to invert the output signal.	BT, RI & RO

Introduction (Continued)

Control Signals

Every port on the MSX devices has two available global clock inputs, input enables, and output enables. However, not all ports have access to the same global control signals. There are four global clocks (CLK_0 through CLK_3),

four global input enables (IE_0 through IE_3), and four global output enables ($\overline{OE}$_0 through $\overline{OE}$_3). Each global control signal is available to half of the ports on the MSX device. Table 2 below shows the global control signals that are available to each port.

TABLE 2. MSX Global Control Signals

MSX340 Port Number	MSX532 Port Number	Input/Output Clock Source 1	Input Output Clock Source 2	Input Enable 1	Input Enable 2	Output Enable 1	Output Enable 2
Ports 0-84	Ports 0-132	CLK_0	CLK_1	IE_0	IE_1	OE_0	OE_1
Ports 85-169	Ports 133-265	CLK_1	CLK_2	IE_1	IE_2	OE_1	OE_2
Ports 170-254	Ports 266-398	CLK_2	CLK_3	IE_2	IE_3	OE_2	OE_3
Ports 255-339	Ports 399-531	CLK_3	CLK_0	IE_3	IE_0	OE_3	OE_0

RapidConfigure Interface

The MSX family of Digital Crosspoint Switches can be configured in either of two ways. Both the JTAG serial programming interface and the RapidConfigure (RC) parallel interface can assign crosspoint connections and configure I/O buffers, but JTAG is a serial input and is slower. JTAG runs reliably up to 8 MHz and requires over twenty cycles to program a single command. The RapidConfigure interface can run at up to 40 MHz and can send a new command on every clock cycle. Systems requiring frequent reconfiguration should be designed to use the RapidConfigure interface.

RapidConfigure is a 29 signal parallel interface that effectively flattens the serial JTAG bitstream. Rather than consecutively shifting in twenty or so bits of data to configure an I/O buffer or make a crosspoint connection, all of these bits are driven on the RC lines simultaneously and then latched in by the MSX device in a single cycle. Additionally, the MSX RapidConfigure interface has been enhanced to enable reading back of configuration data from the device.

RCA[9:0] = RapidConfigure Address A
RCB[9:0] = RapidConfigure Address B
RCC[3:0] = RapidConfigure Program Variable C
RCI[1:0] = RapidConfigure Instruction Bits
RC_CLK = RapidConfigure Clock
$\overline{RC\_EN}$ = RapidConfigure Cycle Enable
RC_RDY = Read out I/O buffer and connect/disconnect status

Signal Description

The RC interface supports four types of operations. Two are write operations to the MSX (I/O buffer configuration or crosspoint programming) and two are read operations (I/O buffer and crosspoint configuration read). The RC signals serve different purposes depending upon the type of operation being performed.

Most of the signals on the MSX device's RC interface are bi-directional. These signals receive data during write operations. During read operations these pins receive data during the first part of the cycle, and then drive the interface in the final part of the cycle. RCA[9:0], RCB[9:0], and RCC[0] are bi-directional pins. RCC[3:1], RC_CLK, $\overline{RC\_EN}$, and

RCI[1:0] are dedicated inputs. RC_RDY is a dedicated output.

The RC_CLK signal is the strobe that latches write data into the MSX device. It synchronizes the signals driven on to the RC interface and determines the rate at which commands can be loaded into the MSX device. The MSX device latches command data on the falling edge of RC_CLK when $\overline{RC\_EN}$ is asserted. RC Write operations can be repeated on consecutive clocks simply by keeping the $\overline{RC\_EN}$ signal asserted and providing new commands on the RCA, RCB, RCC, and RCI signals. RC Read operations require four AC clock cycles and cannot be performed on back-to-back clocks.

$\overline{RC\_EN}$ is an Active LOW signal that enables an RC operation. Back-to-back RC Write operations may be performed by keeping the $\overline{RC\_EN}$ signal asserted. During RC Read operations $\overline{RC\_EN}$ must remain asserted until the cycle is complete. Back-to-back RC Read operations can be executed simply by keeping $\overline{RC\_EN}$ asserted.

The MSX device asserts RC_RDY when it has entered the final stage of a read and data out is ready. RC_RDY is asserted on the falling edge of RC_CLK, and de-asserted on the next falling edge. The MSX device will be driving valid read data on the RC interface when RC_RDY is asserted HIGH.
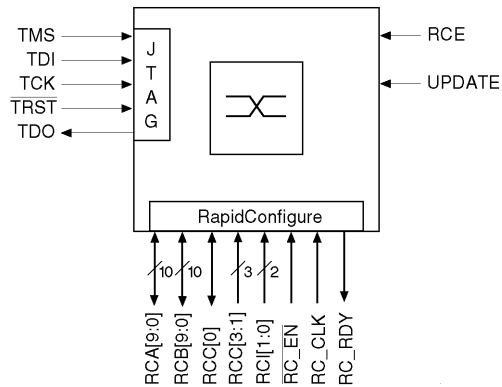

FIGURE 4. MSX Switch Configuration Signals

The RC interface specifies that the RCI signals be used to determine the type of operation being performed.

Introduction (Continued)

TABLE 3. RapidConfigure Input

RCI [1:0]	Description
00	Force Testing Command. Force commands can force a port to drive either a one or a zero to either the pad or crosspoint array. These commands are generally only used for diagnostic testing.
01	I/O Buffer Programming Command. These commands are used to configure a port as an input or output, registered or not, etc.
10	Crosspoint Array Programming Command. Crosspoint connections can be made or broken, or an individual port can be reset.
11	Read and Reset Commands. This setting is used to read back configuration data from an I/O buffer or crosspoint connection information. It can also be used to reset all of the I/O buffers and the crosspoint array.

Read and Reset Commands

When RCI[1:0] are equal to 11 a Read or Reset command is executed (see Table 4: Reset Commands).

Reset Commands
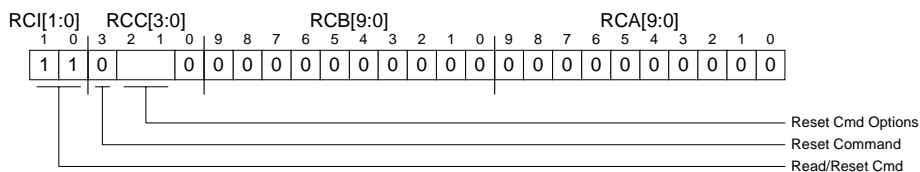
TABLE 4. Reset Commands (Continued)

RCC [2:1]	Description
00	Reserved. This is not a valid command.
01	Reserved. This is not a valid command.
10	Crosspoint Array Reset. This command will reset the entire crosspoint array, breaking any previously existing connections.
11	Crosspoint Array and I/O Buffer Reset. This command resets both the I/O buffers and the crosspoint array as described above.

RCC[0], RCB[9:0], and RCA[9:0] have no function during a reset command and must be written as zeroes.

Crosspoint Read Commands

A crosspoint read is used to check whether two ports are connected through the crosspoint array. The two ports are addressed using RCA[9:0] and RCB[9:0]

The MSX device uses RCC[0] to show whether the two ports are connected. It drives RCC[0] HIGH if the two ports are connected, and pulls RCC[0] LOW if the two ports are not connected.
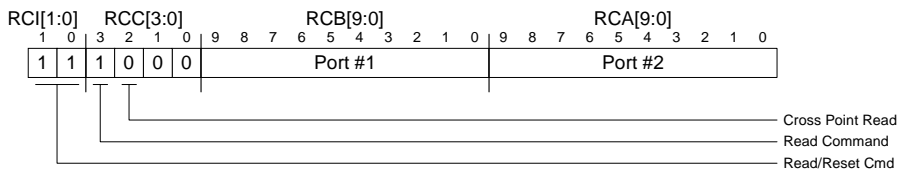
I/O Buffer Read Commands

I/O Buffer reads are more complicated (see Table 5: I/O Buffer read Commands). The port to be read is addressed

using RCA[9:0]. The MSX device uses RCA[9:0] and RCB[9:0] to return all of the configuration data for the particular I/O buffer.
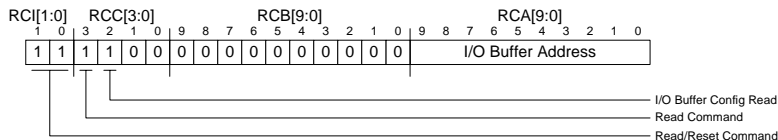
Introduction (Continued)

TABLE 5. I/O Buffer Read Commands

Signal	Description
RCA[0]	RCA[0] is set to one if the I/O buffer is an input. It is zero if the I/O buffer is not configured as an input. Note that an I/O buffer can be configured as an Input, Output, Input and Output (in bi-directional mode), or No Connect. All I/O buffers default to inputs at power-on reset or following a global I/O buffer Reset command, so RCA[0] will read as a one at reset. RCA[0] Function 0 I/O buffer not set to input 1 I/O buffer set to input (default)
RCA[1]	RCA[1] is set to a one if the I/O buffer is an output. It is zero if the I/O buffer is not configured as an output. If RCA[1:0] equal 00 the I/O buffer is configured as a No Connect. A No Connect means that the I/O pin of the MSX device is not connected to the crosspoint array. RCA[1] will read as a zero at reset. RCA[1] Function 0 I/O buffer not set to output (default) 1 I/O buffer set to output
RCA[2]	RCA[2] is set to a one if the I/O buffer is configured in Bus Repeater Mode. It is zero if the I/O buffer is not in Bus Repeater Mode. Bus Repeater Mode will be disabled by default at reset, so RCA[2] will read as a zero. RCA[2] Function 0 I/O buffer not set to Bus Repeater Mode (default) 1 I/O buffer set to Bus Repeater Mode
RCA[3]	RCA[3] is set to a one if the I/O buffer is configured as a registered input and is assigned to use its Input Clock 1. It is zero if the I/O buffer is not using Input Clock 1. Input Clock 1 for each I/O buffer will vary depending upon the quadrant of the device in which it resides. RCA[3] will read as a zero at reset. RCA[3] Function 0 I/O buffer not set to registered input mode (default) 1 I/O buffer set to registered input mode
RCA[4]	RCA[4] is set to a one if the I/O buffer is configured as a registered input and is assigned to use its Input Clock 2. It is zero if the I/O buffer is not using Input Clock 2. As with Input Clock 1, the source changes depending upon the quadrant of the device in which the I/O buffer resides. RCA[4] will read as a zero at reset. RCA[4] Function 0 I/O buffer not using Input Clock Source 2 in RI mode (default) 1 I/O buffer using Input Clock Source 2 in RI mode
RCA[5]	RCA[5] is set to a one if the I/O buffer is configured as a registered input and assigned to use Next Neighbor Clocking. It is zero if Next Neighbor Clocking is disabled. Next Neighbor Clocking allows the I/O buffer to be registered using the next higher numbered Port number signal as its input clock source. Port 100 on the MSX devices can use the signal from Port 101 for its input clock if this mode is enabled. Port 531's Next Neighbor is Port 0. Next Neighbor Clocking will be disabled by default at reset, so RCA[5] will read as a zero. RCA[5] Function 0 I/O buffer not using Next Neighbor Clock in RI mode (default) 1 I/O buffer using Next Neighbor Clock in RI mode
RCA[6]	RCA[6] is set to a one if the I/O buffer is configured as a registered output and is assigned to use its Output Clock 1. It is zero if the I/O buffer is not using Output Clock 1. As with Input Clock 1 and 2, the Output Clocks will vary depending upon the quadrant of the device in which the I/O buffer resides. In the case of the MSX devices, the Output Clock 1 and Input Clock 1 for each I/O buffer have the same source, and the Output Clock 2 and Input Clock 2 do as well. RCA[6] will read as a zero at reset. RCA[6] Function 0 I/O buffer not using Output Clock Source 1 in RO mode (default) 1 I/O buffer using Output Clock Source 1 in RO mode
RCA[7]	RCA[7] is set to a one if the I/O buffer is configured as a registered output and is assigned to use its Output Clock 2. It is zero if the I/O buffer is not using Output Clock 2. As with Output Clock 1, the source changes depending upon the quadrant of the device in which the I/O buffer resides. RCA[7] will read as a zero at reset. RCA[7] Function 0 I/O buffer not using Output Clock Source 2 in RO mode (default) 1 I/O buffer using Output Clock Source 2 in RO mode

I/O Buffer Read Commands (Continued)

Introduction (Continued)

Signal	Description
RCA[8]	RCA[8] is set to a one if the I/O buffer is configured as a registered output and is assigned to use Next Neighbor Clocking. It is zero if Next Neighbor Clocking is disabled. Next Neighbor Clocking allows the I/O buffer to be registered using the next higher numbered Port number signal as its output clock source. Port 100 on the MSX devices can use the signal from Port 101 for its output clock if this mode is enabled. Port 531's Next Neighbor is Port 0. Next Neighbor Clocking will be disabled by default at reset, so RCA[8] will read as a zero. RCA[8]　　Function 0　　I/O buffer not using Next Neighbor Clock in RO mode (default) 1　　I/O buffer using Next Neighbor Clock in RO mode
RCA[9]	RCA[9] is set to a one if the I/O buffer is assigned to use Input Enable 1. It is zero if the I/O buffer is not using Input Enable 1. All bi-directional I/O buffers must use one of the dedicated input enable pins (IE_0, IE_1, IE_2, or IE_3) to enable the I/O buffer to drive data into the crosspoint array. As with the dedicated clock pins, each I/O buffer can access two input enable signals, which will vary depending upon the quadrant of this chip in which the I/O buffer resides. RCA[9] will read as a zero at reset. RCA[9]　　Function 0　　I/O buffer not using Input Enable Source 1 (default) 1　　I/O buffer using Input Enable Source 1
RCB[0]	RCB[0] is set to a one if the I/O buffer is assigned to use Input Enable 2. It is zero if the I/O buffer is not using Input Enable 2. RCB[0] will read as a zero at reset. RCB[0]　　Function 0　　I/O buffer not using Input Enable Source 2 (default) 1　　I/O buffer using Input Enable Source 2
RCB[1]	RCB[1] is set to a one if the I/O buffer is assigned to use Output Enable 1. It is zero if the I/O buffer is not using Output Enable 1. All bi-directional I/O buffers must use one of the dedicated output enable pins ($\overline{OE}$_0, $\overline{OE}$_1, $\overline{OE}$_2, or $\overline{OE}$_3) to enable the I/O buffer to drive the pin of the device. As with the dedicated clock pins, each I/O buffer can access two output enable signals, which will vary depending upon the quadrant of the chip in which the I/O buffer resides. RCB[1] will read as a zero at reset. RCB[1]　　Function 0　　I/O buffer not using Output Enable Source 1 (default) 1　　I/O buffer using Output Enable Source 1
RCB[2]	RCB[2] is set to a one if the I/O buffer is assigned to use Output Enable 2. It is zero if the I/O buffer is not using Output Enable 2. RCB[2] will read as a zero at reset. RCB[2]　　Function 0　　I/O buffer not using Output Enable Source 2 (default) 1　　I/O buffer using Output Enable Source 2
RCB[6:3]	RCB[6:3] are reserved.
RCB[7]	RCB[7] is set to a one if the I/O buffer is configured as an inverted output. It is zero if the I/O buffer is not configured as an inverted output. The output of any I/O buffer may be inverted so long as it is not a registered output or running in Bus Repeater Mode. RCB[7] will read as a zero at reset. RCB[7]　　Function 0　　I/O buffer not configured as inverted output (default) 1　　I/O buffer configured as inverted output
RCB[8]	RCB[8] is set to a one if the I/O buffer is configured as a registered input and is using an inverted input clock source. It is zero if it is not using an inverted input clock. Inputs can use any of the three clock sources described above and may invert that clock if desired. RCB[8] will read as a zero at reset. RCB[8]　　Function 0　　I/O buffer not using inverted clock source in RI mode (default) 1　　I/O buffer using inverted clock source in RI mode
RCB[9]	RCB[9] is set to a one if the I/O buffer is configured as a registered output and is using an inverted output clock source. It is zero if it is not using an inverted output clock. Outputs can use any of the three clock sources described above and may invert that clock if desired. RCB[9] will read as a zero at reset. RCB[9]　　Function 0　　I/O buffer not using inverted clock source in RO mode (default) 1　　I/O buffer using inverted clock source in RO mode

Introduction (Continued)

Crosspoint Programming

Connections between ports through the crosspoint array can be quickly made or broken using the RC interface. The two ports to be connected or disconnected are addressed using RCA[9:0] and RCB[9:0]. RCC[1] controls whether a connection is made or broken. The two ports are connected when RCC[1] is set to zero, and disconnected when RCC[1] is set to one
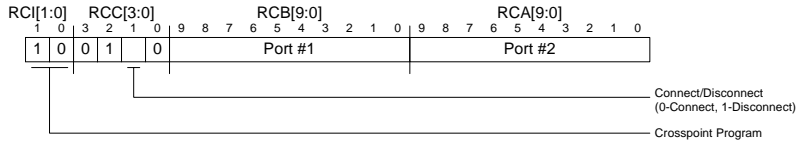
Unlike I/O buffer programming commands, which take effect immediately upon execution of the command, crosspoint connections will only be made if the UPDATE signal is asserted HIGH. The crosspoint programming command loads the Loading SRAM cell in the selected crosspoint array location with a one (in the case of a new connection) or a zero (to break an existing connection). If the UPDATE signal is asserted, the Loading SRAM cells contents are immediately transferred to the Active SRAM cell and the connection is made or broken. However, if the UPDATE signal is held LOW, the new connection will not be made.

The UPDATE signal can be used to control when the switch matrix connections are reconfigured.

I/O Buffer Configuration Programming

Each port can be fully configured in a single RapidConfigure cycle. The figure below shows how an I/O buffer is programmed using all of the signals on the RC interface. The following table shows how each control bits (RCC[3:0] and RCB[9:0]) are used. During an I/O buffer programming command the RCA[9:0] signals address the port to be programmed (see Table 6: I/O buffer Programming Commands)
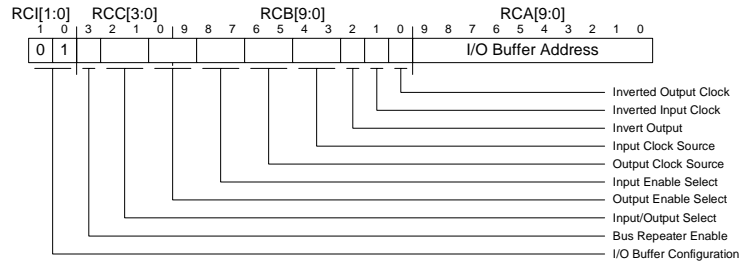
Introduction (Continued)

TABLE 6. I/O Buffer Programming Commands

Signal	Description
RCC[3]	Bus Repeater Enable. Setting this bit to a one enables the I/O buffer to operate in Bus Repeater Mode, a special bi-directional mode. When zero the I/O buffer will not operate in Bus Repeater Mode. When programming an I/O buffer to use Bus Repeater Mode, all of the other control bits must be set to zeroes. Attempting to combine other I/O buffer options with Bus Repeater Mode may lead to unpredictable results.
RCC[2:1]	Input/Output Select. These two bits are used to configure the I/O buffer as an input, output, input/output (bi-directional mode), or no connect. When operating in bi-directional mode it is critical that the port be assigned input and output enables so that it can be 3-STATED appropriately to avoid contention. RCC[2:1] Function 00 No Connect 01 Input 10 Output 11 Input / Output for Bi-Directional Mode
RCC[0] and RCB[9]	Output Enable Select. These two bits are used to select from the two available active LOW global output enables. The output will be allowed to drive when its assigned output enable is asserted. An output port will be 3-STATED when its assigned output enable is de-asserted. When both output enables are selected, the two available active LOW output enable signals are AND'ed together to form the port's combined output enable signal. RCC[0], RCB[9] Function 00 No Output Enable Selected 01 Output Enable 1 10 Output Enable 2 11 Both Output Enables
RCB[8:7]	Input Enable Select. These bits are used to assign a port one of the two available global input enable signals. An input port will drive into the crosspoint array when its assigned input enable is asserted. When both input enables are selected, the two available input enable signals are OR'ed together to form the port's combined input enable signal. RCB[8:7] Function 00 No Input Enable Selected 01 Input Enable 1 10 Input Enable 2 11 Both Input Enables
RCB[6:5]	Output Clock Source. These bits are used to select a clock source for a registered output port. Each I/O buffer can select from one of two global clock inputs, or can use Next Neighbor Clocking. Next Neighbor Clocking uses the signal on the next higher numbered port as a clock source. If no clock source is assigned to an output port, it will operate in flow-through mode. RCB[6:5] Function 00 No Output Clock Source Selected 01 Output Clock Source 1 10 Output Clock Source 2 11 Next Neighbor Output Clock Source
RCB[4:3]	Input Clock Source. These bits are used to select a clock source for a registered input port. Each I/O buffer can select from one of two global clock inputs, or can use Next Neighbor Clocking. Next Neighbor Clocking uses the signal on the next higher numbered port as a clock source. If no clock source is assigned to an input port, it will operate in flow-through mode. RCB[6:5] Function 00 No Input Clock Source Selected 01 Input Clock Source 1 10 Input Clock Source 2 11 Next Neighbor Input Clock Source
RCB[2]	Invert Output. If an output port is programmed with this bit set to a one, the output of the port will be inverted. If this bit is zero, the output will not be inverted. Outputs may not be inverted when operating in Bus Repeater Mode or in registered output mode.
RCB[1]	Inverted Input Clock. When this bit is set to a one, the registered input port's selected clock source will be inverted. When zero the input clock source will not be inverted.

Introduction (Continued)

Signal	Description
RCB[0]	Inverted Output Clock. When this bit is set to a one, the registered output port's selected clock source will be inverted. When zero the output clock source will not be inverted.

JTAG Interface

The dedicated JTAG TAP interface is designed in compliance with the IEEE-1149.1. The standard interface has five pins: Test Data Out (TDO), Test Mode Select (TMS), Test Data In (TDI), Test Reset (TRST), and Test Clock (TCK) which allow Boundary Scan Testing as well as device configuration and verification. Data on the TDI and TMS pins are clocked into the device on the rising edge of the TCK signal, while the valid data appears on the TDO pin after the falling edge of TCK. For more detailed information on JTAG programming, refer to the MSX Family Register Programming Manual.

I/O Buffer Programming

The JTAG I/O Buffer Data Register where data is held, is used to program the I/O buffer. This register is used with the JTAG interface only. The JTAG I/O buffer data register is 20 bits wide. Power on reset, RapidConfigure reset, Hardware reset, and JTAG reset programs all Ports as inputs. JTAG can be reset via the TRST pin or by clocking five consecutive ones to the TMS pin. The HW_RST (hardware reset) pin resets and breaks all connections in the Crosspoint Array to all no-connects, and the I/O buffers to inputs.

Table 7 lists the bits and their function in JTAG mode. These are internal bits as shifted into the I/O buffer data register for I/O buffer programming.

TABLE 7. I/O Buffer Programming Bit Functions

Bit Number	I/O Buffer Function	Description
0	Input (IN)	Input Pin Data to Drive Array
1	Output (OP)	Output Array Data to Pin
2	Bus Repeater (BR)	Low Array Signal, Drive Pin LOW Low Pin Signal, Drive Array LOW
3	Reg In Clock 1	Selects Reg. In I/O Buffer, Clock 1
4	Reg In Clock 2	Selects Reg. In I/O Buffer, Clock 2
5	Reg In Clock Neighbor	Selects Reg. In I/O Buffer, Neighbor
6	Reg Out Clock 1	Selects Reg. Out I/O Buffer, Clock 1
7	Reg Out Clock 1	Selects Reg. Out I/O Buffer, Clock 2
8	Reg Out Clock Neighbor	Selects Reg. Out I/O Buffer, Neighbor
9	Input Enable 1 (IE_1)	Select Input Enable 1 (Note 1)
10	Input Enable 2 (IE_2)	Select Input Enable 2 (Note 1)
11	Output Enable 1 (OE_1)	Select Output Enable 1 (Note 2)
12	Output Enable 2 (OE_2)	Select Output Enable 2 (Note 2)
13	Force 1	Force I/O Buffer Output Pin to a 1
14	Force 0	Force I/O Buffer Output Pin to a 0
15	Array 1	Force I/O Buffer Array to a 1
16	Array 0	Force I/O Buffer Array to a 0
17	Invert Output	Output data is inverted. This operation is invalid in Bus Repeater mode and Register Output mode
18	Invert Input Clock	Invert the Clock to the Input Register
19	Invert Output Clock	Invert the Clock to the Output Register

Note 1: If both IE_1 and IE_2 are selected, the two are assigned an OR function to form the IE. Either can be "1" to enable the input.

Note 2: If both OE_1 and OE_2 are selected, active LOW signals are assigned an AND function to form the resulting OE. Either can be "0" to enable the output.

Introduction (Continued)
JTAG Architecture and Shift Registers

Boundary Scan Register
(576 x 2 = 1152Bits)

JTAG Data Register - 1 Bit

IOB Data Register - 20 Bits

IOB Copy Register - 20 Bits

Device Identification Register - 32 Bits

TDI

MUX BUF TDO

Mode Control Register - 2 Bits

JTAG Address Register - 10 Bits

Bypass Register - 1 Bit

Instruction Register - 16 Bits

TMS

TCK

TAP
Controller

TRST
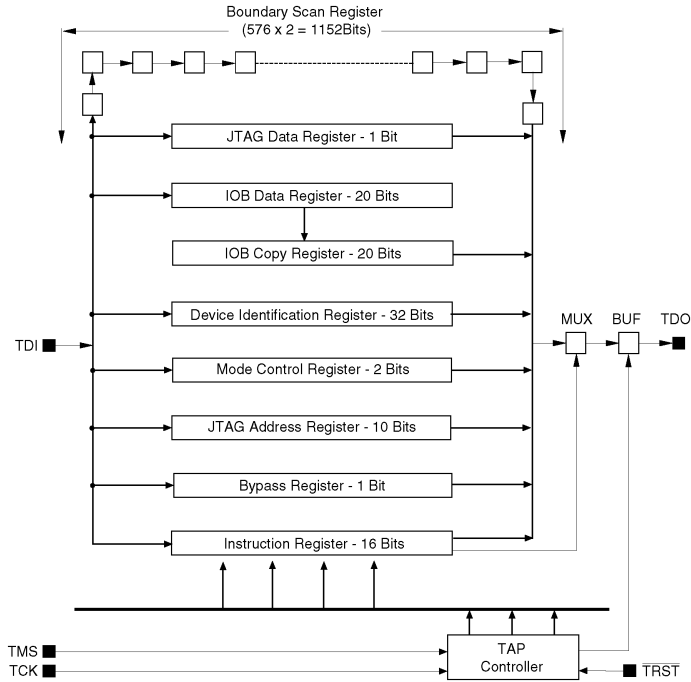
FIGURE 5. MSX JTAG Architecture

Test Logic
Reset

Run Test/
Idle

Select DR
Scan

Select IR
Scan

Capture
DR

Capture
IR

Shift DR

Shift IR

Exit 1 DR

Exit 1 IR

Pause DR

Pause IR

Exit 2 DR

Exit 2 IR

Update DR

Update IR
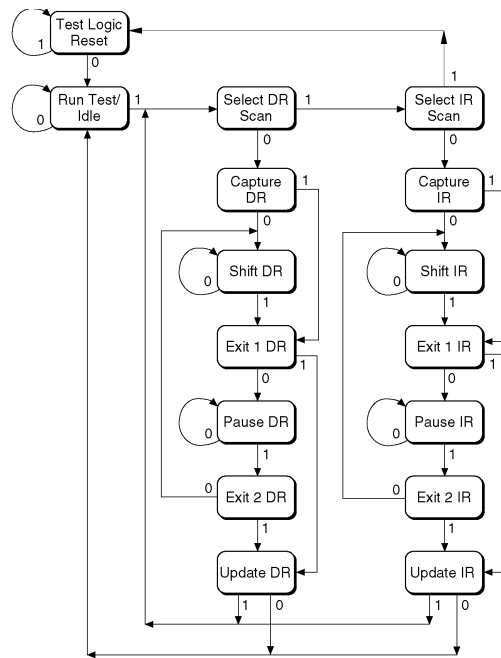
FIGURE 6. JTAG State Machine

Introduction (Continued)

TABLE 8. JTAG Input Format

	Instruction				Control		Address									
Bit Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	13	12	11	10	C1	C0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

TABLE 9. JTAG Instructions

15	14	13	12	Instruction	Description
1	1	1	1	Bypass	Places device in a mode to pass TDI data to TDO with one clock delay. Used for programming and testing devices through serial connected JTAG controls.
1	1	1	0	Control Bit	Sets and clears the control bit A0 (LSB)
1	1	0	1	IO Buffer and Crosspoint Array Reset, Device ID out	Resets I/O buffers for the Ports to Input and clear all Ports to Disconnect. The device ID is serialized out to TDO. The Instruction serialized out is the RESET Instruction during the Instruction phase. Update is forced to the crosspoint array
1	1	0	0	Device ID out	Serialize the device ID and revision history out to TDO. ID for the MSX is 0x0000A89F.
1	0	1	1	Set the JTAG Address Register	Set the 10-bit JTAG Address Register with the lower ten bits of the JTAG Instruction Register. The lower ten bits of the JTAG Address Register become the 'B' Address for Crosspoint Access.
1	0	1	0	Access the Crosspoint Array and Update Array	Read or Write the crosspoint addressed by the lower ten bits of the JTAG Instruction (A Address) and the JTAG Address Register or Address Counter (B Address). Read data is shifted out on TDO. C1 C0 = 0 0 Read Switch with A and B Address. Increment 'B' address with each ShiftDR. C1 C0 = 0 1 Connect switch at location Addressed with A and B. Increment 'B' address with each ShiftDR. Activate with UpdateDR. C1 C0 = 1 0 Disconnect switch at location Addressed with A and B. Increment 'B' address with each ShiftDR. Activate with UpdateDR. C1 C0 = 1 1 Force update of Switch Array Shadow register. Activate with UpdateDR.
1	0	0	1	Disconnect a Port in the Crosspoint Array	Disconnect all Ports from the Port Addressed by the lower ten bits of the JTAG Instruction. The addressed port is reset to disconnect. The programmed state of the I/O buffer is not changed.
1	0	0	0	Clear the Crosspoint Array	Clear the crosspoint array at no-connect. Leave the I/O buffers unchanged.
0	1	1	1	Shift the IO Buffer Data Register	Shift twenty bits of data into and out of the I/O buffer Data register. The data is used to program the I/O buffers. Parallel shift twenty bits into I/O buffer Copy Register.
0	1	1	0	Shift out the I/O buffer Copy Register	Shifts twenty bits of data out of the I/O buffer Copy Register. Data is either the I/O buffer Data register shifted in by instruction 0111 or the last JTAG I/O buffer Read Data.
0	1	0	1	Access an I/O buffer	Read or write the I/O buffer addressed with the lower ten bits of the JTAG Instruction. Read data is placed in the twenty-bit I/O buffer Copy Register. Write Data for the I/O buffer is from the I/O buffer Data Register. C1 C0 = 0 0 Read an I/O buffer date into the Copy Register. C1 C0 = 0 1 Write an I/O buffer with data in I/O buffer Data Register.
0	1	0	0		Not used.
0	0	1	1	Test mode only for programming device with RapidConfigure through JTAG	Fairchild only - internal test mode to test RapidConfigure through JTAG.
0	0	1	0	Crosspoint Array Write Testing, Write one location per ShiftDR	Instruction Address = Lower Limit = A, Address Register = Upper Limit = B. C1 = 1, C0 = 1 Connect all ports in address range C1 = 1, C0 = 0 Connect Pattern=A[1] XOR B[1] C1 = 0, C0 = 0 Connect Pattern=A[4] C1 = 0, C0 = 1 Connect Pattern = NOT (A[1] XOR B[1]). Compliment address limits, Address is complimented to test A-High Port to B-Low Port connections. Other three patterns test opposite. The number of cycles = (Sum of (X = 1), where X = Low Limit to X = High Limit) - 1
0	0	0	0	Sample/Preload EXTEST	External scan tests for interconnect testing.
0	0	0	1	Sample/Preload EXTEST	External scan tests for interconnect testing.

Introduction (Continued)

Device Reset Options

At power-on, all MSX532 I/O buffers are set as flow-through inputs (IN) with input enable ON, and the switch matrix set to all No Connects (NC).

The RapidConfigure reset, hardware reset, and JTAG reset functions will program the I/O buffers to flow-through input (IN) mode with input enable ON, and each Loading SRAM cell in the Switch Matrix is set to No Connect. An UPDATE

signal is required to complete the operation and set the Active SRAM cells to No Connect.

The JTAG interface can be reset via the $\overline{TRST}$ pin or by clocking five consecutive one to the TMS pin. The hardware reset pin can be done accomplished through the $\overline{HW\_RST}$ pin (Active LOW). RC reset can be accomplished by applying the RC Instruction 1101 to the RCI[3:0] pins.

Device Reset Options

Programming Interface	Reset Method	I/O Port	Switch Matrix	RCE Mode Control	JTAG TAP
Hardware Reset	Power-on Reset	IN	NC	1 (RC Enabled)	TLR (Note 3)
	$\overline{HW\_RST}$ (Low Pulse)	IN	NC (Note 4)	1 (RC Enabled)	TLR
JTAG Reset	1. Low Pulse on $\overline{TRST}$	Unchanged	Unchanged	Unchanged	TLR
	2. TMS High for 5 SCLK Cycles	Unchanged	Unchanged	Unchanged	TLR
	3. Device Reset (Instruction 1101)	IN	NC (Note 3)	1 (RC Enabled)	TLR
	4. Reset Crosspoint Array (Instruction 1101)	Unchanged	NC (Note 3)	Unchanged	Unchanged
RapidConfigure Reset	1. Device Reset (Instruction 1101)	IN	NC (Note 3)	1 (RC Enabled)	Unchanged
	2. Reset Crosspoint Array (Instruction 0010)	Unchanged	NC (Note 3)	Unchanged	Unchanged

Note 3: NC = No Connect. Each Loading SRAM cell in the Switch Matrix is updated to No Connect. An UPDATE signal is required to complete the operation and set the Active SRAM cells to No Connect.

Note 4: TLR = Test Logic Reset State.

Pin Description

Pin Name	Type	Description
P[531:000]	Bi-directional	Input/Output Signals.
$\overline{OE}$[3:0]	Input	Global Output Enables. Each output enable can control two of the four I/O banks.
		Signal MSX532 Connected I/O's
		$\overline{OE}$_0 P399-P531, P000-P132
		$\overline{OE}$_1 P000-P132, P133-P265
		$\overline{OE}$_2 P133-P265, P266-P398
		$\overline{OE}$_3 P266-P398, P399-P531
IE[3:0]	Input	Global Input Enables. Each input enable can control two of the four I/O banks.
		Signal MSX532 Connected I/O's
		IE_0 P399-P531, P000-P132
		IE_1 P000-P132, P133-P265
		IE_2 P133-P265, P266-P398
		IE_3 P266-P398, P399-P531
UPDATE	Input	Global Update
CLK[3:0]	Input	Global Clocks. Each clock can control two of the four I/O banks.
		Signal MSX532 Connected I/O's
		CLK_0 P399-P531, P000-P132
		CLK_1 P000-P132, P133-P265
		CLK_2 P133-P265, P266-P398
		CLK_3 P266-P398, P399-P531
$\overline{HW\_RST}$	Input	Hardware Reset.
RCE	Input	RapidConfigure Mode Select
		Programing mode is determined at power up or $\overline{HW\_RST}$
		0 = JTAG Mode (RapidConfigure Disabled)
		1 = RapidConfigure Mode (JTAG, I/O buffer, Crosspoint Programming Disabled)
		Note: Device can be reconfigured from JTAG to RC or from RC to JTAG in the JTAG mode without $\overline{HW\_RST}$ or power up. In RapidConfigure mode the programming of the I/O buffers and crosspoint array through JTAG is disabled, but the JTAG port can still be used for boundary scan testing.
RC Pins		
RC_CLK	Input	RapidConfigure Clock.
$\overline{RC\_EN}$	Input	RapidConfigure Cycle Enable.
RCA[9:0]	Bi-directional	RapidConfigure Address A.
RCB[9:0]	Bi-directional	RapidConfigure Address B.
RCC[0]	Bi-directional	RapidConfigure Program Variable C.
RCC[3:1]	Input	RapidConfigure Program Variable C.
RCI[1:0]	Input	RapidConfigure Instruction Bits.
RC_RDY	Output	Read Out I/O Buffer and Connect/Disconnect Status.
JTAG Pins		
TCK	Input	JTAG Test Clock.
TDI	Input	JTAG Test Data In.
TDI	Output	JTAG Test Data Out.
TMS	Input	JTAG Test Mode Select.
$\overline{TRST}$	Input	JTAG Test and JTAG Scan Reset.
Power and Ground Pins		
V_{DD}	Power	+3.3V power for the chip.
V_{SS}	Ground	Ground for the chip. Tie these pins to system ground.

Absolute Maximum Ratings(Note 5)

Supply Voltage V_{DD}	-0.3V to +3.6 V
Supply Voltage (Inputs) V_{IN}	
(Note 6)(Note 7)	-0.3V to +5.5V
Junction Temperature T_J	+150°C
Storage Temperature T_{STG}	-65°C to +150°C
Maximum Power Dissipation P_{MAX}	10.5W
Electrostatic Discharge ESD (Note 8)	1500V

Recommended Operating Conditions

Supply Voltage V_{DD}	+3.0V to +3.6V
Operating Temperature T_A	0°C to +70°C

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: A maximum undershoot of 2V for a maximum duration of 20 ns is acceptable. Overshoot to 5.5V is acceptable.

Note 7: All inputs are 5V tolerant with the V_{DD} pin at 3.3V.

Note 8: Measured using Human Body Model.

Pin Capacitance (Note 9)

Symbol	Parameter	Limits	Units
C_{CLK}	Input Capacitance	10.0	pF
C_{PORT}	I/O Signal Port Capacitance	8.0	pF

Note 9: Capacitance measured at 25°C. Sample tested only.

DC Electrical Characteristics (T_A = 0°C to 70°C, V_{DD} = 3.3V ±10%)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	HIGH Level Input	Ports are 5V Tolerant	2.1	5.25	V
V_{IL}	LOW Level Input	Ports are 5V Tolerant	-0.3	0.8	V
V_{OH}	HIGH Level Output	V_{DD} = Min V_{DD} = 3.00 I_{OH} = -4 mA	2.4	V_{DD} + 0.3	V
V_{OL}	LOW Level Output	V_{DD} = Min V_{DD} = 3.00 I_{OL} = 8 mA		0.4	V
I_{LIH}, I_{LIL}	Input Leakage for Non-programmable I/O pins	V_{DD} = Max $0.0 < I_n < V_{DD}$		+5.0 -600	µA
I_{LOZ}	3-STATE Leakage Output OFF State	V_{DD} = Max $0.0 < I_n < V_{DD}$		+5.0 -100	µA
I_{OSH}	Short Circuit Current, Out = HIGH	V_{DD} = Max V_0 = GND		-80.0	mA
I_{OSL}	Short Circuit Current, Out = LOW	V_{DD} = Max V_0 = V_{DD}		80.0	mA
Supply Current					
I_{DDQ}	Quiescent Supply Current	V_{DD} = Max		96.0	mA
Q_{DDD} (Note 10)	Dynamic Supply Current	V_{DD} = Max. No Load, One Input Cycling @ 50% Duty Cycle		0.375	mA/MHz

Note 10: See Power Consumption section for dynamic power consumption calculation.

AC Electrical Characteristics (T_A = 0°C to 70°C, V_{DD} = 3.3V ±10%)

Symbol	Parameter	Min	Max	Units
R_{DATA}	NRZ Data Rate		150	Mb/s
f_{RIO}	Registered Input/Output Clock Frequency		75.0	MHz
t_{W_RIO}	Registered Clock Pulse Width, HIGH or LOW	3.0		ns
t_{S_RI}	Registered Input Setup Time to Clock	5.0		ns
t_{S_RO}	Registered Output Setup Time to Clock	9.5		ns
t_{H_RI}	Registered Input Clock to Hold Data	0.0		ns
t_{H_RO}	Registered Output Clock to Hold Data	0.0		ns
t_{CO_RO}	Registered Output Clock to Data Out Valid		11.0	ns
t_{CO_RI}	Registered Input Clock to Data Out Valid		24.0	ns
t_{PHL}, t_{PLH}	One Way Signal Propagation Delay, Fanout = 1		20.0	ns
t_{MC} Delta	Additional Delay Per Output Multicast (MC) Mode		2.0	ns
t_{W+}	Input Flow-through Positive Pulse Width	6.0		
t_{W-}	Input Flow-through Negative Pulse Width	6.0		
t_{SK}	Skew		4.0	ns
t_{PZH_IT}, t_{PZL_IT}	Input Enable to Valid Data		20.0	ns
t_{PZH_OT}, t_{PZL_OT}	Output Enable to Valid Data		7.5	ns
t_{PZH_OT}, t_{PZL_OT}	Output Enable to High Z State		7.5	ns
t_{RC}	RapidConfigure Clock Period	20.0		ns
t_{W+_RC}, t_{W-_RC}	RapidConfigure Clock Pulse Width	8.0		ns
t_{S_RC}	RapidConfigure Address Setup to RC Clock	1.0		ns
t_{H_RC}	RapidConfigure Address Hold Time to RC Clock	4.0		ns
t_{P_RC}	Read Back Access Time		9.0	ns
t_{P_RD}	RC_RDY to Readback Data		4.0	ns
t_{P_UD}	Update of Crosspoint to Data Out		10.0	ns
f_{JTAG}	JTAG Clock Frequency (TCK)		8.0	MHz
t_{W_JTAG}	JTAG Clock Pulse Width (TCK) at 8 MHz Cycle	48.0	72.0	ns
t_{S_JTAG}	JTAG Setup Time	4.0		ns
t_{H_JTAG}	JTAG Hold Time	0.0		ns
t_{P_JTAG}	JTAG Clock to Output Data Valid (TDO)		10.0	ns

Refer to Figure 7 for AC test conditions.

Test Circuit and Timing Diagrams
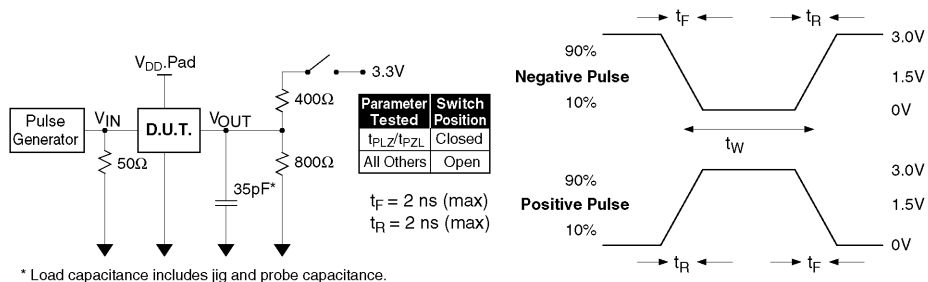
FIGURE 7. Test Circuit and Waveform Definition
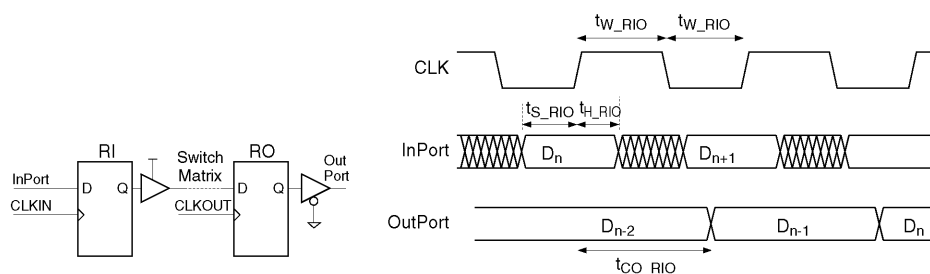
FIGURE 8. Registered Input and Registered Output Mode Timing (ICLK and OCLK Synchronized)
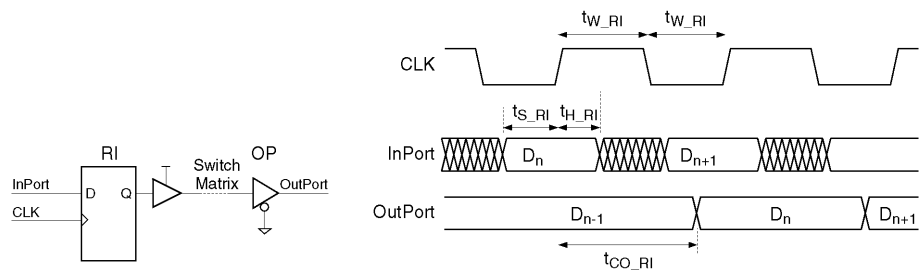
FIGURE 9. Registered Input Timing Mode
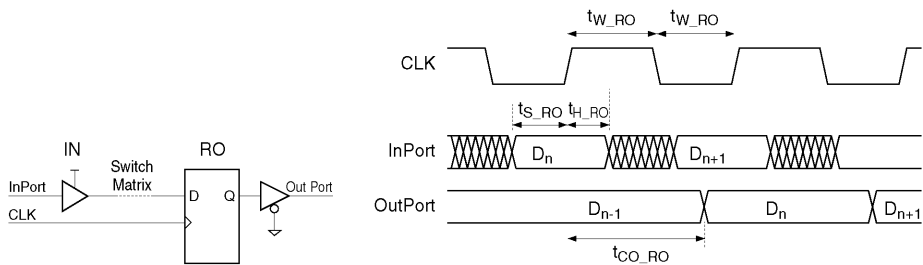
FIGURE 10. Registered Output Timing Mode

Test Circuit and Timing Diagrams (Continued)
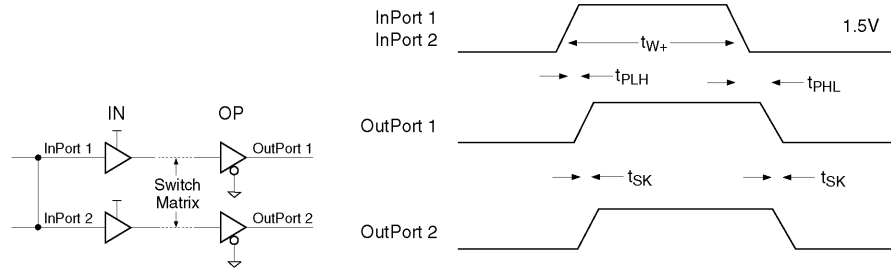
FIGURE 11. I/O Port Timing (Flow-through Mode)
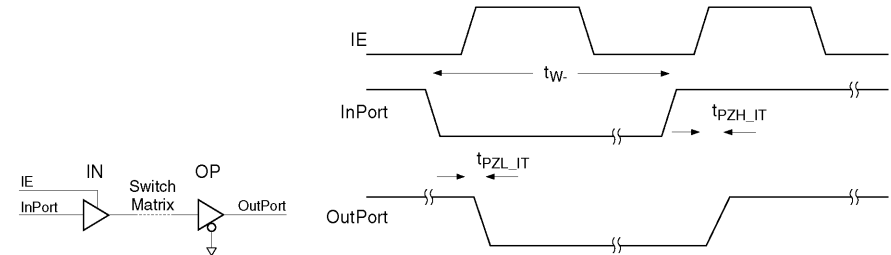
FIGURE 12. Input Enable Timing (Flow-through Mode)
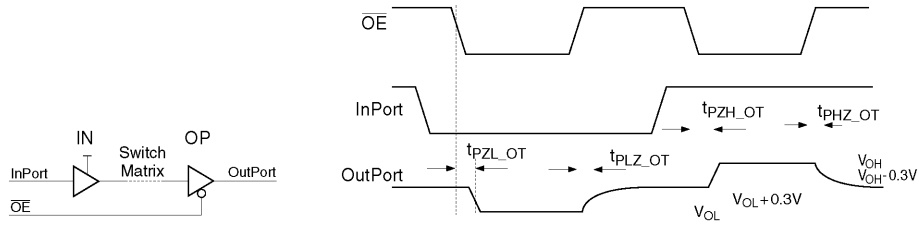
FIGURE 13. Output Enable Timing

FIGURE 14. JTAG Timing

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Test Circuit and Timing Diagrams (Continued)

RapidConfigure I/O Buffer or Crosspoint Write Cycle
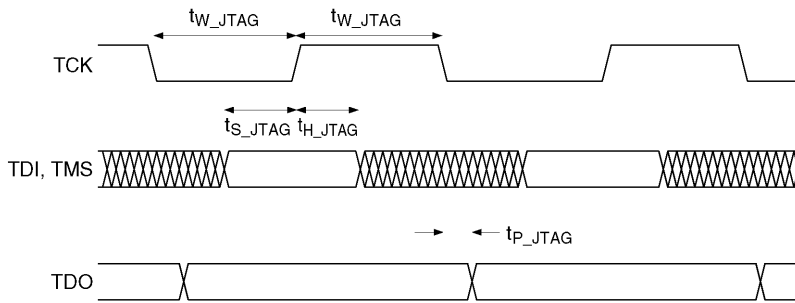
RapidConfigure I/O Buffer or Crosspoint Read Cycle
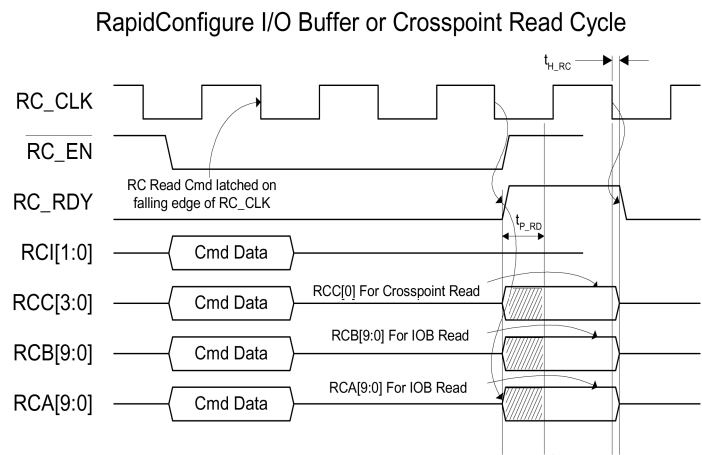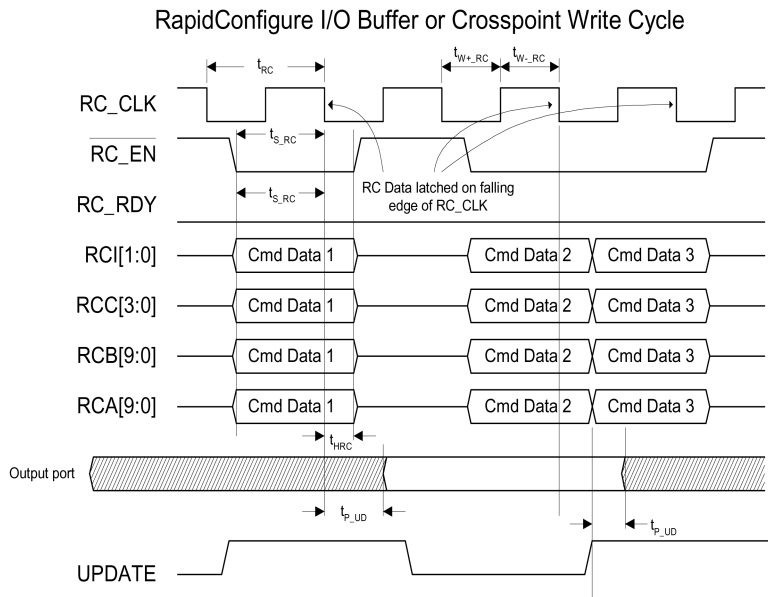
FIGURE 15. RapidConfigure I/O Buffer or Crosspoint Read and Write Cycles

Test Circuit and Timing Diagrams (Continued)
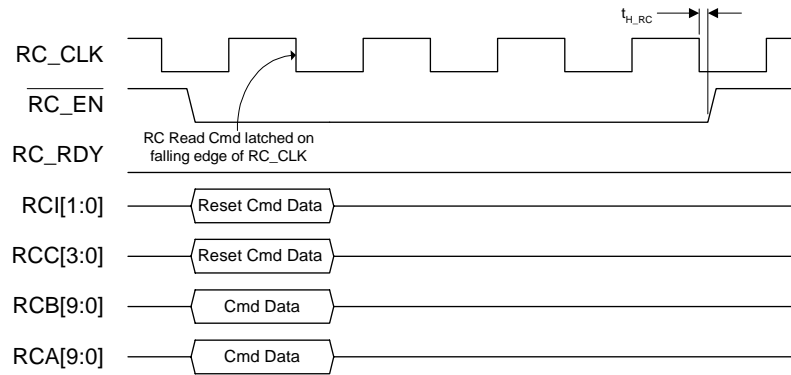
FIGURE 16. RapidConfigure Reset Command Cycle

Package and Pinout

MSX532 [792 TBGA Package] Pinout

MSX532
in 792 TBGA

Top View

MSX532

Package and Pinout (Continued)

TABLE 10. MSX532 Pinout By Ball Sequence

Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name
A1	V_{SS}	B1	V_{SS}	C1	V_{SS}	D1	V_{SS}	E1	RCA6	F1	RCB1
A2	V_{SS}	B2	V_{SS}	C2	V_{SS}	D2	RCA1	E2	RCA3	F2	RCA8
A3	V_{SS}	B3	V_{SS}	C3	V_{SS}	D3	V_{SS}	E3	RCA0	F3	RCA5
A4	V_{SS}	B4	CLK_0	C4	V_{SS}	D4	V_{SS}	E4	V_{SS}	F4	RCA4
A5	$\overline{TRST}$	B5	$\overline{HW\_RST}$	C5	IE_0	D5	V_{SS}	E5	V_{SS}	F5	RCA2
A6	P000	B6	P001	C6	TMS	D6	RC_RDY	E6	$\overline{OE\_0}$	F6	V_{DD}
A7	V_{SS}	B7	P002	C7	P003	D7	TCK	E7	TDO	F7	TDI
A8	P007	B8	P006	C8	P004	D8	P005	E8	V_{DD}	F8	V_{DD}
A9	P012	B9	P013	C9	P010	D9	P011	E9	P008	F9	P009
A10	P016	B10	P017	C10	P015	D10	P014	E10	V_{DD}	F10	V_{DD}
A11	V_{SS}	B11	P022	C11	P020	D11	P021	E11	P018	F11	P019
A12	P026	B12	P024	C12	P025	D12	P023	E12	V_{DD}	F12	V_{DD}
A13	P033	B13	P031	C13	P030	D13	P028	E13	P029	F13	P027
A14	P037	B14	P034	C14	P035	D14	P032	E14	V_{DD}	F14	V_{DD}
A15	V_{SS}	B15	P040	C15	P041	D15	P039	E15	P038	F15	P036
A16	P044	B16	P045	C16	P042	D16	P043	E16	V_{DD}	F16	V_{DD}
A17	P050	B17	P051	C17	P048	D17	P049	E17	P047	F17	P046
A18	P055	B18	P054	C18	P052	D18	P053	E18	V_{DD}	F18	V_{DD}
A19	V_{SS}	B19	P061	C19	P058	D19	P059	E19	P056	F19	P057
A20	P065	B20	P060	C20	P063	D20	P062	E20	V_{DD}	F20	V_{DD}
A21	V_{SS}	B21	P064	C21	P066	D21	P067	E21	P069	F21	P068
A22	P071	B22	P070	C22	P072	D22	P073	E22	V_{DD}	F22	V_{DD}
A23	P075	B23	P074	C23	P077	D23	P076	E23	P079	F23	P078
A24	P080	B24	P081	C24	P083	D24	P082	E24	V_{DD}	F24	V_{DD}
A25	V_{SS}	B25	P085	C25	P084	D25	P087	E25	P086	F25	P088
A26	P089	B26	P091	C26	P090	D26	P093	E26	V_{DD}	F26	V_{DD}
A27	P092	B27	P095	C27	P094	D27	P096	E27	P097	F27	P099
A28	P098	B28	P100	C28	P101	D28	P103	E28	V_{DD}	F28	V_{DD}
A29	V_{SS}	B29	P102	C29	P104	D29	P105	E29	P107	F29	P106
A30	P109	B30	P108	C30	P111	D30	P110	E30	V_{DD}	F30	V_{DD}
A31	P112	B31	P113	C31	P115	D31	P114	E31	P117	F31	P116
A32	P119	B32	P118	C32	P120	D32	P121	E32	V_{DD}	F32	V_{DD}
A33	V_{SS}	B33	P123	C33	P122	D33	P124	E33	P127	F33	P129
A34	P125	B34	P126	C34	P130	D34	P132	E34	P135	F34	V_{DD}
A35	V_{SS}	B35	P128	C35	P133	D35	V_{SS}	E35	V_{SS}	F35	P137
A36	V_{SS}	B36	P131	C36	V_{SS}	D36	V_{SS}	E36	V_{SS}	F36	P136
A37	V_{SS}	B37	V_{SS}	C37	V_{SS}	D37	V_{SS}	E37	P134	F37	CLK_1
A38	V_{SS}	B38	V_{SS}	C38	V_{SS}	D38	IE_1	E38	$\overline{OE\_1}$	F38	P139
A39	V_{SS}	B39	V_{SS}	C39	V_{SS}	D39	V_{SS}	E39	P142	F39	P145

Package and Pinout (Continued)

Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name
G1	V_{SS}	H1	RCB7	J1	V_{SS}	K1	RCE	L1	P526	M1	P521
G2	RCB3	H2	RCB6	J2	RCC2	K2	$\overline{RC\_EN}$	L2	P528	M2	P523
G3	RCB2	H3	RCB5	J3	RCC1	K3	RC_CLK	L3	P529	M3	P522
G4	RCB0	H4	RCB4	J4	RCC0	K4	RCI1	L4	P531	M4	P524
G5	RCA9	H5	V_{DD}	J5	RCB9	K5	RCI0	L5	P530	M5	P525
G6	RCA7	H6	V_{DD}	J6	RCB8	K6	RCC3	L6	UPDATE	M6	P527
G34	P138	H34	V_{DD}	J34	P150	K34	P157	L34	P163	M34	V_{DD}
G35	P141	H35	V_{DD}	J35	P152	K35	P156	L35	P162	M35	V_{DD}
G36	P140	H36	P147	J36	P153	K36	P159	L36	P165	M36	P168
G37	P143	H37	P149	J37	P155	K37	P158	L37	P164	M37	P169
G38	P144	H38	P148	J38	P154	K38	P160	L38	P167	M38	P171
G39	P146	H39	P151	J39	V_{SS}	K39	P161	L39	P166	M39	P170

Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name
N1	V_{SS}	P1	P512	R1	V_{SS}	T1	P502	U1	V_{SS}	V1	P495
N2	P517	P2	P513	R2	P506	T2	P504	U2	P499	V2	P494
N3	P516	P3	P515	R3	P509	T3	P505	U3	P498	V3	P496
N4	P519	P4	P514	R4	P508	T4	P507	U4	P501	V4	P497
N5	P518	P5	V_{DD}	R5	P511	T5	V_{DD}	U5	P500	V5	V_{DD}
N6	P520	P6	V_{DD}	R6	P510	T6	V_{DD}	U6	P503	V6	V_{DD}
N34	P172	P34	V_{DD}	R34	P180	T34	V_{DD}	U34	P190	V34	V_{DD}
N35	P173	P35	V_{DD}	R35	P183	T35	V_{DD}	U35	P192	V35	V_{DD}
N36	P175	P36	P177	R36	P182	T36	P186	U36	P193	V36	P197
N37	P174	P37	P179	R37	P184	T37	P189	U37	P195	V37	P196
N38	P176	P38	P178	R38	P185	T38	P188	U38	P194	V38	P199
N39	V_{SS}	P39	P181	R39	P187	T39	P191	U39	V_{SS}	V39	P198

Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name
W1	P488	Y1	P485	AA1	V_{SS}	AB1	P479	AC1	P475	AD1	P468
W2	P489	Y2	P484	AA2	P482	AB2	P476	AC2	P473	AD2	P466
W3	P491	Y3	P486	AA3	P478	AB3	P477	AC3	P472	AD3	P467
W4	P490	Y4	P487	AA4	P483	AB4	P474	AC4	P470	AD4	P465
W5	P492	Y5	V_{DD}	AA5	P481	AB5	V_{DD}	AC5	P471	AD5	V_{DD}
W6	P493	Y6	V_{DD}	AA6	P480	AB6	V_{DD}	AC6	P469	AD6	V_{DD}
W34	P200	Y34	V_{DD}	AA34	P213	AB34	V_{DD}	AC34	P223	AD34	V_{DD}
W35	P201	Y35	V_{DD}	AA35	P212	AB35	V_{DD}	AC35	P220	AD35	V_{DD}
W36	P203	Y36	P206	AA36	P210	AB36	P217	AC36	P221	AD36	P227
W37	P202	Y37	P207	AA37	P211	AB37	P216	AC37	P218	AD37	P225
W38	P205	Y38	P204	AA38	P209	AB38	P214	AC38	P219	AD38	P224
W39	V_{SS}	Y39	P208	AA39	V_{SS}	AB39	P215	AC39	V_{SS}	AD39	P222

Package and Pinout (Continued)

Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name
AE1	V_{SS}	AF1	P458	AG1	P450	AH1	P451	AJ	P443	AK1	P441
AE2	P464	AF2	P459	AG2	P454	AH2	P449	AJ2	P447	AK2	P440
AE3	P462	AF3	P457	AG3	P455	AH3	P448	AJ3	P444	AK3	P438
AE4	P463	AF4	P456	AG4	P452	AH4	P446	AJ4	P445	AK4	P439
AE5	P460	AF5	V_{DD}	AG5	P453	AH5	V_{DD}	AJ5	P442	AK5	V_{DD}
AE6	P461	AF6	V_{DD}	AG6	V_{SS}	AH6	V_{DD}	AJ6	V_{SS}	AK6	V_{DD}
AE34	P230	AF34	V_{DD}	AG34	P240	AH34	V_{DD}	AJ34	P249	AK34	V_{DD}
AE35	P231	AF35	V_{DD}	AG35	P238	AH35	V_{DD}	AJ35	P248	AK35	V_{DD}
AE36	P228	AF36	P234	AG36	P239	AH36	P245	AJ36	P246	AK36	P253
AE37	P229	AF37	P235	AG37	P236	AH37	P242	AJ37	P247	AK37	P252
AE38	P226	AF38	P233	AG38	P237	AH38	P243	AJ38	P244	AK38	P250
AE39	V_{SS}	AF39	P232	AG39	V_{SS}	AH39	P241	AJ39	V_{SS}	AK39	P251

Ball	Ball Name	Ball	Ball Name	Ball	Ball Name
AL1	P433	AM1	P432	AN1	V_{SS}
AL2	P436	AM2	P430	AN2	P429
AL3	P437	AM3	P431	AN3	P426
AL4	P434	AM4	P428	AN4	P427
AL5	P435	AM5	V_{DD}	AN5	P425
AL6	V_{SS}	AM6	V_{DD}	AN6	P423
AL34	P258	AM34	V_{DD}	AN34	P271
AL35	P259	AM35	V_{DD}	AN35	P268
AL36	P257	AM36	P262	AN36	P269
AL37	P256	AM37	P263	AN37	P267
AL38	P254	AM38	P260	AN38	P264
AL39	P255	AM39	P261	AN39	V_{SS}

Package and Pinout (Continued)

Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name
AP1	P424	AR1	V_{SS}	AT1	V_{SS}	AU1	V_{SS}	AV1	V_{SS}	AW1	V_{SS}
AP2	P422	AR2	P421	AT2	$\overline{OE}\_3$	AU2	V_{SS}	AV2	V_{SS}	AW2	V_{SS}
AP3	P420	AR3	P418	AT3	V_{SS}	AU3	V_{SS}	AV3	V_{SS}	AW3	V_{SS}
AP4	P419	AR4	V_{SS}	AT4	V_{SS}	AU4	V_{SS}	AV4	CLK_3	AW4	V_{SS}
AP5	V_{DD}	AR5	V_{SS}	AT5	V_{SS}	AU5	P417	AV5	P415	AW5	P410
AP6	V_{DD}	AR6	IE_3	AT6	P416	AU6	P414	AV6	P412	AW6	P407
AP7	P413	AR7	P411	AT7	P409	AU7	P408	AV7	P406	AW7	V_{SS}
AP8	P404	AR8	P405	AT8	P402	AU8	P403	AV8	P401	AW8	P400
AP9	P398	AR9	P399	AT9	P396	AU9	P397	AV9	P394	AW9	V_{SS}
AP10	V_{DD}	AR10	V_{DD}	AT10	P395	AU10	P393	AV10	P392	AW10	P390
AP11	P391	AR11	P389	AT11	P388	AU11	P386	AV11	V_{SS}	AW11	P387
AP12	V_{DD}	AR12	V_{DD}	AT12	P385	AU12	P384	AV12	P382	AW12	P383
AP13	P380	AR13	P381	AT13	P378	AU13	P379	AV13	P377	AW13	V_{SS}
AP14	V_{DD}	AR14	V_{DD}	AT14	P376	AU14	P374	AV14	P375	AW14	P372
AP15	P373	AR15	P370	AT15	P371	AU15	P369	AV15	P368	AW15	P366
AP16	V_{DD}	AR16	V_{DD}	AT16	P367	AU16	P364	AV16	P365	AW16	P362
AP17	P363	AR17	P361	AT17	P360	AU17	P358	AV17	P359	AW17	V_{SS}
AP18	V_{DD}	AR18	V_{DD}	AT18	P357	AU18	P356	AV18	P354	AW18	P355
AP19	P353	AR19	P352	AT19	P350	AU19	P351	AV19	P348	AW19	V_{SS}
AP20	V_{DD}	AR20	V_{DD}	AT20	P346	AU20	P347	AV20	P349	AW20	P345
AP21	P341	AR21	P340	AT21	P343	AU21	P342	AV21	P344	AW21	V_{SS}
AP22	V_{DD}	AR22	V_{DD}	AT22	P336	AU22	P337	AV22	P339	AW22	P338
AP23	P331	AR23	P330	AT23	P332	AU23	P333	AV23	P335	AW23	P334
AP24	V_{DD}	AR24	V_{DD}	AT24	P327	AU24	P326	AV24	P328	AW24	P329
AP25	P321	AR25	P323	AT25	P322	AU25	P325	AV25	P324	AW25	V_{SS}
AP26	V_{DD}	AR26	V_{DD}	AT26	P316	AU26	P319	AV26	P318	AW26	P320
AP27	P310	AR27	P312	AT27	P313	AU27	P315	AV27	P314	AW27	P317
AP28	V_{DD}	AR28	V_{DD}	AT28	P306	AU28	P309	AV28	P308	AW28	P311
AP29	P303	AR29	P302	AT29	P304	AU29	P305	AV29	P307	AW29	V_{SS}
AP30	P296	AR30	P297	AT30	P299	AU30	P298	AV30	P301	AW30	P300
AP31	P290	AR31	P293	AT31	P292	AU31	P295	AV31	P294	AW31	V_{SS}
AP32	V_{DD}	AR32	V_{DD}	AT32	P286	AU32	P289	AV32	P288	AW32	P291
AP33	IE_2	AR33	P283	AT33	P282	AU33	P285	AV33	P287	AW33	V_{SS}
AP34	V_{DD}	AR34	P279	AT34	P281	AU34	P280	AV34	$\overline{OE}\_2$	AW34	P284
AP35	V_{DD}	AR35	V_{SS}	AT35	V_{SS}	AU35	P276	AV35	P278	AW35	CLK_2
AP36	P274	AR36	V_{SS}	AT36	V_{SS}	AU36	V_{SS}	AV36	V_{SS}	AW36	V_{SS}
AP37	P272	AR37	P277	AT37	V_{SS}	AU37	V_{SS}	AV37	V_{SS}	AW37	V_{SS}
AP38	P270	AR38	P273	AT38	P275	AU38	V_{SS}	AV38	V_{SS}	AW38	V_{SS}
AP39	P265	AR39	P266	AT39	V_{SS}	AU39	V_{SS}	AV39	V_{SS}	AW39	V_{SS}

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Package and Pinout (Continued)

TABLE 11. MSX532 Pinout By Ball Name (alphabetically)

Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball
CLK_0	B4	P027	F13	P067	D21	P107	E29	P147	H36
CLK_1	F37	P028	D13	P068	F21	P108	B30	P148	H38
CLK_2	AW35	P029	E13	P069	E21	P109	A30	P149	H37
CLK_3	AV4	P030	C13	P070	B22	P110	D30	P150	J34
$\overline{\text{HW\_RST}}$	B5	P031	B13	P071	A22	P111	C30	P151	H39
IE_0	C5	P032	D14	P072	C22	P112	A31	P152	J35
IE_1	D38	P033	A13	P073	D22	P113	B31	P153	J36
IE_2	AP33	P034	B14	P074	B23	P114	D31	P154	J38
IE_3	AR6	P035	C14	P075	A23	P115	C31	P155	J37
$\overline{\text{OE}}$_0	E6	P036	F15	P076	D23	P116	F31	P156	K35
$\overline{\text{OE}}$_1	E38	P037	A14	P077	C23	P117	E31	P157	K34
$\overline{\text{OE}}$_2	AV34	P038	E15	P078	F23	P118	B32	P158	K37
$\overline{\text{OE}}$_3	AT2	P039	D15	P079	E23	P119	A32	P159	K36
P000	A6	P040	B15	P080	A24	P120	C32	P160	K38
P001	B6	P041	C15	P081	B24	P121	D32	P161	K39
P002	B7	P042	C16	P082	D24	P122	C33	P162	L35
P003	C7	P043	D16	P083	C24	P123	B33	P163	L34
P004	C8	P044	A16	P084	C25	P124	D33	P164	L37
P005	D8	P045	B16	P085	B25	P125	A34	P165	L36
P006	B8	P046	F17	P086	E25	P126	B34	P166	L39
P007	A8	P047	E17	P087	D25	P127	E33	P167	L38
P008	E9	P048	C17	P088	F25	P128	B35	P168	M36
P009	F9	P049	D17	P089	A26	P129	F33	P169	M37
P010	C9	P050	A17	P090	C26	P130	C34	P170	M39
P011	D9	P051	B17	P091	B26	P131	B36	P171	M38
P012	A9	P052	C18	P092	A27	P132	D34	P172	N34
P013	B9	P053	D18	P093	D26	P133	C35	P173	N35
P014	D10	P054	B18	P094	C27	P134	E37	P174	N37
P015	C10	P055	A18	P095	B27	P135	E34	P175	N36
P016	A10	P056	E19	P096	D27	P136	F36	P176	N38
P017	B10	P057	F19	P097	E27	P137	F35	P177	P36
P018	E11	P058	C19	P098	A28	P138	G34	P178	P38
P019	F11	P059	D19	P099	F27	P139	F38	P179	P37
P020	C11	P060	B20	P100	B28	P140	G36	P180	R34
P021	D11	P061	B19	P101	C28	P141	G35	P181	P39
P022	B11	P062	D20	P102	B29	P142	E39	P182	R36
P023	D12	P063	C20	P103	D28	P143	G37	P183	R35
P024	B12	P064	B21	P104	C29	P144	G38	P184	R37
P025	C12	P065	A20	P105	D29	P145	F39	P185	R38
P026	A12	P066	C21	P106	F29	P146	G39	P186	T36

Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball
P187	R39	P227	AD36	P267	AN37	P307	AV29	P347	AU20
P188	T38	P228	AE36	P268	AN35	P308	AV28	P348	AV19
P189	T37	P229	AE37	P269	AN36	P309	AU28	P349	AV20
P190	U34	P230	AE34	P270	AP38	P310	AP27	P350	AT19
P191	T39	P231	AE35	P271	AN34	P311	AW28	P351	AU19
P192	U35	P232	AF39	P272	AP37	P312	AR27	P352	AR19
P193	U36	P233	AF38	P273	AR38	P313	AT27	P353	AP19
P194	U38	P234	AF36	P274	AP36	P314	AV27	P354	AV18
P195	U37	P235	AF37	P275	AT38	P315	AU27	P355	AW18
P196	V37	P236	AG37	P276	AU35	P316	AT26	P356	AU18
P197	V36	P237	AG38	P277	AR37	P317	AW27	P357	AT18
P198	V39	P238	AG35	P278	AV35	P318	AV26	P358	AU17
P199	V38	P239	AG36	P279	AR34	P319	AU26	P359	AV17
P200	W34	P240	AG34	P280	AU34	P320	AW26	P360	AT17
P201	W35	P241	AH39	P281	AT34	P321	AP25	P361	AR17
P202	W37	P242	AH37	P282	AT33	P322	AT25	P362	AW16
P203	W36	P243	AH38	P283	AR33	P323	AR25	P363	AP17
P204	Y38	P244	AJ38	P284	AW34	P324	AV25	P364	AU16
P205	W38	P245	AH36	P285	AU33	P325	AU25	P365	AV16
P206	Y36	P246	AJ36	P286	AT32	P326	AU24	P366	AW15
P207	Y37	P247	AJ37	P287	AV33	P327	AT24	P367	AT16
P208	Y39	P248	AJ35	P288	AV32	P328	AV24	P368	AV15
P209	AA38	P249	AJ34	P289	AU32	P329	AW24	P369	AU15
P210	AA36	P250	AK38	P290	AP31	P330	AR23	P370	AR15
P211	AA37	P251	AK39	P291	AW32	P331	AP23	P371	AT15
P212	AA35	P252	AK37	P292	AT31	P332	AT23	P372	AW14
P213	AA34	P253	AK36	P293	AR31	P333	AU23	P373	AP15
P214	AB38	P254	AL38	P294	AV31	P334	AW23	P374	AU14
P215	AB39	P255	AL39	P295	AU31	P335	AV23	P375	AV14
P216	AB37	P256	AL37	P296	AP30	P336	AT22	P376	AT14
P217	AB36	P257	AL36	P297	AR30	P337	AU22	P377	AV13
P218	AC37	P258	AL34	P298	AU30	P338	AW22	P378	AT13
P219	AC38	P259	AL35	P299	AT30	P339	AV22	P379	AU13
P220	AC35	P260	AM38	P300	AW30	P340	AR21	P380	AP13
P221	AC36	P261	AM39	P301	AV30	P341	AP21	P381	AR13
P222	AD39	P262	AM36	P302	AR29	P342	AU21	P382	AV12
P223	AC34	P263	AM37	P303	AP29	P343	AT21	P383	AW12
P224	AD38	P264	AN38	P304	AT29	P344	AV21	P384	AU12
P225	AD37	P265	AP39	P305	AU29	P345	AW20	P385	AT12
P226	AE38	P266	AR39	P306	AT28	P346	AT20	P386	AU11

Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball
P387	AW11	P427	AN4	P467	AD3	P507	T4	RCB3	G2
P388	AT11	P428	AM4	P468	AD1	P508	R4	RCB4	H4
P389	AR11	P429	AN2	P469	AC6	P509	R3	RCB5	H3
P390	AW10	P430	AM2	P470	AC4	P510	R6	RCB6	H2
P391	AP11	P431	AM3	P471	AC5	P511	R5	RCB7	H1
P392	AV10	P432	AM1	P472	AC3	P512	P1	RCB8	J6
P393	AU10	P433	AL1	P473	AC2	P513	P2	RCB9	J5
P394	AV9	P434	AL4	P474	AB4	P514	P4	RCC0	J4
P395	AT10	P435	AL5	P475	AC1	P515	P3	RCC1	J3
P396	AT9	P436	AL2	P476	AB2	P516	N3	RCC2	J2
P397	AU9	P437	AL3	P477	AB3	P517	N2	RCC3	K6
P398	AP9	P438	AK3	P478	AA3	P518	N5	RCE	K1
P399	AR9	P439	AK4	P479	AB1	P519	N4	RCI0	K5
P400	AW8	P440	AK2	P480	AA6	P520	N6	RCI1	K4
P401	AV8	P441	AK1	P481	AA5	P521	M1	RC_RDY	D6
P402	AT8	P442	AJ5	P482	AA2	P522	M3	TCK	D7
P403	AU8	P443	AJ1	P483	AA4	P523	M2	TDI	F7
P404	AP8	P444	AJ3	P484	Y2	P524	M4	TDO	E7
P405	AR8	P445	AJ4	P485	Y1	P525	M5	TMS	C6
P406	AV7	P446	AH4	P486	Y3	P526	L1	$\overline{TRST}$	A5
P407	AW6	P447	AJ2	P487	Y4	P527	M6	UPDATE	L6
P408	AU7	P448	AH3	P488	W1	P528	L2	V_{DD}	E8
P409	AT7	P449	AH2	P489	W2	P529	L3	V_{DD}	E10
P410	AW5	P450	AG1	P490	W4	P530	L5	V_{DD}	E12
P411	AR7	P451	AH1	P491	W3	P531	L4	V_{DD}	E14
P412	AV6	P452	AG4	P492	W5	RC_CLK	K3	V_{DD}	E16
P413	AP7	P453	AG5	P493	W6	$\overline{RC\_EN}$	K2	V_{DD}	E18
P414	AU6	P454	AG2	P494	V2	RCA0	E3	V_{DD}	E20
P415	AV5	P455	AG3	P495	V1	RCA1	D2	V_{DD}	E22
P416	AT6	P456	AF4	P496	V3	RCA2	F5	V_{DD}	E24
P417	AU5	P457	AF3	P497	V4	RCA3	E2	V_{DD}	E26
P418	AR3	P458	AF1	P498	U3	RCA4	F4	V_{DD}	E28
P419	AP4	P459	AF2	P499	U2	RCA5	F3	V_{DD}	E30
P420	AP3	P460	AE5	P500	U5	RCA6	E1	V_{DD}	E32
P421	AR2	P461	AE6	P501	U4	RCA7	G6	V_{DD}	F6
P422	AP2	P462	AE3	P502	T1	RCA8	F2	V_{DD}	F8
P423	AN6	P463	AE4	P503	U6	RCA9	G5	V_{DD}	F10
P424	AP1	P464	AE2	P504	T2	RCB0	G4	V_{DD}	F12
P425	AN5	P465	AD4	P505	T3	RCB1	F1	V_{DD}	F14
P426	AN3	P466	AD2	P506	R2	RCB2	G3	V_{DD}	F16

Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball
V_{DD}	F18	V_{DD}	AF6	V_{DD}	AR32	V_{SS}	E4	V_{SS}	AU3
V_{DD}	F20	V_{DD}	AF34	V_{SS}	A1	V_{SS}	E5	V_{SS}	AU4
V_{DD}	F22	V_{DD}	AF35	V_{SS}	A2	V_{SS}	E35	V_{SS}	AU36
V_{DD}	F24	V_{DD}	AH5	V_{SS}	A3	V_{SS}	E36	V_{SS}	AU37
V_{DD}	F26	V_{DD}	AH6	V_{SS}	A4	V_{SS}	G1	V_{SS}	AU38
V_{DD}	F28	V_{DD}	AH34	V_{SS}	A7	V_{SS}	J1	V_{SS}	AU39
V_{DD}	F30	V_{DD}	AH35	V_{SS}	A11	V_{SS}	J39	V_{SS}	AV1
V_{DD}	F32	V_{DD}	AK5	V_{SS}	A15	V_{SS}	N1	V_{SS}	AV2
V_{DD}	F34	V_{DD}	AK6	V_{SS}	A19	V_{SS}	N39	V_{SS}	AV3
V_{DD}	H5	V_{DD}	AK34	V_{SS}	A21	V_{SS}	R1	V_{SS}	AV11
V_{DD}	H6	V_{DD}	AK35	V_{SS}	A25	V_{SS}	U1	V_{SS}	AV36
V_{DD}	H34	V_{DD}	AM5	V_{SS}	A29	V_{SS}	U39	V_{SS}	AV37
V_{DD}	H35	V_{DD}	AM6	V_{SS}	A33	V_{SS}	W39	V_{SS}	AV38
V_{DD}	M34	V_{DD}	AM34	V_{SS}	A35	V_{SS}	AA1	V_{SS}	AV39
V_{DD}	M35	V_{DD}	AM35	V_{SS}	A36	V_{SS}	AA39	V_{SS}	AW1
V_{DD}	P5	V_{DD}	AP5	V_{SS}	A37	V_{SS}	AC39	V_{SS}	AW2
V_{DD}	P6	V_{DD}	AP6	V_{SS}	A38	V_{SS}	AE1	V_{SS}	AW3
V_{DD}	P34	V_{DD}	AP10	V_{SS}	A39	V_{SS}	AE39	V_{SS}	AW4
V_{DD}	P35	V_{DD}	AP12	V_{SS}	B1	V_{SS}	AG6	V_{SS}	AW7
V_{DD}	T5	V_{DD}	AP14	V_{SS}	B2	V_{SS}	AG39	V_{SS}	AW9
V_{DD}	T6	V_{DD}	AP16	V_{SS}	B3	V_{SS}	AJ6	V_{SS}	AW13
V_{DD}	T34	V_{DD}	AP18	V_{SS}	B37	V_{SS}	AJ39	V_{SS}	AW17
V_{DD}	T35	V_{DD}	AP20	V_{SS}	B38	V_{SS}	AL6	V_{SS}	AW19
V_{DD}	V5	V_{DD}	AP22	V_{SS}	B39	V_{SS}	AN1	V_{SS}	AW21
V_{DD}	V6	V_{DD}	AP24	V_{SS}	C1	V_{SS}	AN39	V_{SS}	AW25
V_{DD}	V34	V_{DD}	AP26	V_{SS}	C2	V_{SS}	AR1	V_{SS}	AW29
V_{DD}	V35	V_{DD}	AP28	V_{SS}	C3	V_{SS}	AR4	V_{SS}	AW31
V_{DD}	Y5	V_{DD}	AP32	V_{SS}	C4	V_{SS}	AR5	V_{SS}	AW33
V_{DD}	Y6	V_{DD}	AP34	V_{SS}	C36	V_{SS}	AR35	V_{SS}	AW36
V_{DD}	Y34	V_{DD}	AP35	V_{SS}	C37	V_{SS}	AR36	V_{SS}	AW37
V_{DD}	Y35	V_{DD}	AR10	V_{SS}	C38	V_{SS}	AT1	V_{SS}	AW38
V_{DD}	AB5	V_{DD}	AR12	V_{SS}	C39	V_{SS}	AT3	V_{SS}	AW39
V_{DD}	AB6	V_{DD}	AR14	V_{SS}	D1	V_{SS}	AT4		
V_{DD}	AB34	V_{DD}	AR16	V_{SS}	D3	V_{SS}	AT5		
V_{DD}	AB35	V_{DD}	AR18	V_{SS}	D4	V_{SS}	AT35		
V_{DD}	AD5	V_{DD}	AR20	V_{SS}	D5	V_{SS}	AT36		
V_{DD}	AD6	V_{DD}	AR22	V_{SS}	D35	V_{SS}	AT37		
V_{DD}	AD34	V_{DD}	AR24	V_{SS}	D36	V_{SS}	AT39		
V_{DD}	AD35	V_{DD}	AR26	V_{SS}	D37	V_{SS}	AU1		
V_{DD}	AF5	V_{DD}	AR28	V_{SS}	D39	V_{SS}	AU2		

Package Thermal Characteristics

TABLE 12. Package Thermal Characteristics

Package	Pin Count	θ_{JC} (°C/W)	θ_{JA} (°C/W) Still Air	θ_{JA} (°C/W) 200 lfpm	θ_{JA} (°C/W) 300 lfpm	θ_{JA} (°C/W) 500 lfpm
TBGA	792	0.4	7.58	6.00	5.66	5.26

Thermal performance values are based on simulation data

Power Consumption

There are three components to consider when calculating power for the MSX Family of devices:

1. Steady State Component:
   This element equals 252 mW.
2. Connection Component:
   This element equals 0.006 mW x Mb/s x connections.
3. Output Drive Component:
   This element equals 0.013 mW x number of outputs x Mb/s x capacitive load (pF).

   Power Consumption = **Steady State Component** + **Connection Component** + **Output Drive Component.**

   = 252 mW + (0.006 x Mb/s x #connections) + (0.013 x Mb/s x #outputs x Cload)

   The following examples shows the total power consumption as determined by the above formula:

   Example 1

   Using the MSX532 with 10 Mb/s into a 10pF load with 266 inputs connected to 266 outputs:

   Power Consumption = 252 mW + (0.006 x 10 x 266) + (0.013 x 266 x 10 x 10)

   = 252 mW + 16 mW + 346 mW = 0.614 Watts

   Example 2

   Using the MSX532 with 150 Mb/s into a 10pF load with 266 inputs connected to 266 outputs:

   Power Consumption = 252 mW + (0.006 x 150 x 266) + (0.013 x 266 x 150 x 10)

   = 252 mW + 239.4 mW + 5187 mW = 5.68 Watts

Glossary

Array Side: The signal and connections between the Crosspoint Array and the I/O Buffer.

Bus Repeater: A circuit operation of the I/O Buffer that enables the MSX device to pass data in both directions on an I/O device pin. The I/O Buffer is placed in a disabled output state to the pin and to the Crosspoint array. A forced LOW on either side of the I/O Buffer will be transmitted to the other side of the I/O Buffer and held until the forced LOW is changed to a force HIGH. At the change of the forcing input, the I/O Buffer will force the other side to a following high state and drive a high level out for a period of time. After the period of time, the I/O Buffer will return to the disabled state.

Bypass: A JTAG instruction that connects the previous chip to the next chip through a one bit data register to speed up programming of other chips in a JTAG chain of devices.

Clock: Four device corner inputs used to gate data into registers in the I/O Buffer. The Corner inputs serve two sides of the MSX. This provides two choices for each I/O Buffer register in and register out. The neighbor input can also be used as register clock and the clocks can be inverted.

Control Register: A programmable register used to control various functions in programming and other circuit settings. All Bits programmed in the JTAG Mode.

RapidConfigure Enable bit can be set with a high level on the RCE pin during a reset of the circuits.

Crosspoint: A single cell containing two N Channel transistors and two RAM bits. The RAM bits are connected in a master-slave configuration to provide an update for programming and changing program information all at once. Each cell contains both an X and Y reset to remove all ports connected to an addressed port in a single program cycle.

Crosspoint Array: An array of Crosspoint used to connect any port to any other port or any combination of other ports. The array has all redundant cell removed; there is a single Crosspoint cell for each port to port connection. The reduced cell count is folded to provide a square array. The array has a diagonal line where the cells are rotated.

Data Bit Lines: A pair of signal lines used to write into and read out of Crosspoint Cells. The lines are pre-charged before a read and one is pulled LOW for a write.

Device ID: A 32-bit register in the MSX device with a wired identification. The ID consists of a given number for the device and a revision history field. The identification is shifted out during JTAG reset and the DEVICE ID instruction in JTAG mode. The ID for the MSX devices is 0x0000A89F.

Glossary (Continued)

Extest: A JTAG instruction that samples I/O pin states and loads new I/O buffer states for testing device pin connections. The MSX devices use a special test mode in Extext to observe the buffer data on the pin side and the array side. A bit in the Control Register controls this mode.

I/O Buffer: The circuit that controls the driving of its associated pin and its port into and out of the Crosspoint Array. The buffer contains all the circuits to make it independent of the other I/O Buffers. Each Buffer contains registers for input and output, driving circuits for input and output, sense for Crosspoint Array input, and RAM bits to hold programmed data controlling the function of the buffer.

Input or Output Path: The signal flow from pin to array and array to pin. Each path has a register with selectable clocks, drivers for the loaded outputs with selectable enables, and sense circuits to detect changes on either side of the I/O Buffer.

JTAG: The Joint Test Action group is a committee to standardize scan testing of devices. The JTAG interface is referred to as IEEE 1149.1. This is a five bit serial programming and testing method.

JTAG Sequence: The ordering of all the pins in a serial chain for driving and sensing signals on pins during Extest and Sample/Preload. All pins except power and ground and the five JTAG pins are in the serial string.

Next Neighbor: Input can be selected as the clock for the I/O buffer registers for data and clock pairing. The next higher port is the selected neighbor except for Port 531, which uses Port 0.

Pin Side Driver: The I/O Buffer circuit that drives the device pin associated with that buffer.

Port: A name followed by a number to identify a pin on the device. Ports are numbered from 531 to 0 on the MSX device. In shifting sequence, Port P000 is shifted in first and shifted out first.

RapidConfigure: A parallel programming method for the MSX devices. The RC mode uses 29 dedicated pins to program the Crosspoint Array and the I/O Buffers. The 29 pins consist of an enable, a strobe, two instruction bits, four variable bits, and two ten-bit address fields.

RCE: A control pin of the MSX device that is sampled during reset to determine if the device becomes active in the JTAG or the RapidConfigure mode. This pin places the Control Register bit in the state to allow RC operations or not based on the voltage level of the RCE pin. The JTAG mode is always enabled and can set or clear the RC bit in the Control Register.

Trickle Current: A very low current (~15 microamperes) used to pull unused or non-driven circuits to a stable HIGH level. Prevents signals from drifting between CMOS thresholds and drawing currents from the power supply. In the case of Bus Repeater, the small trickle current provides a known high level on the pin and array side inputs.

Physical Dimensions inches (millimeters) unless otherwise noted
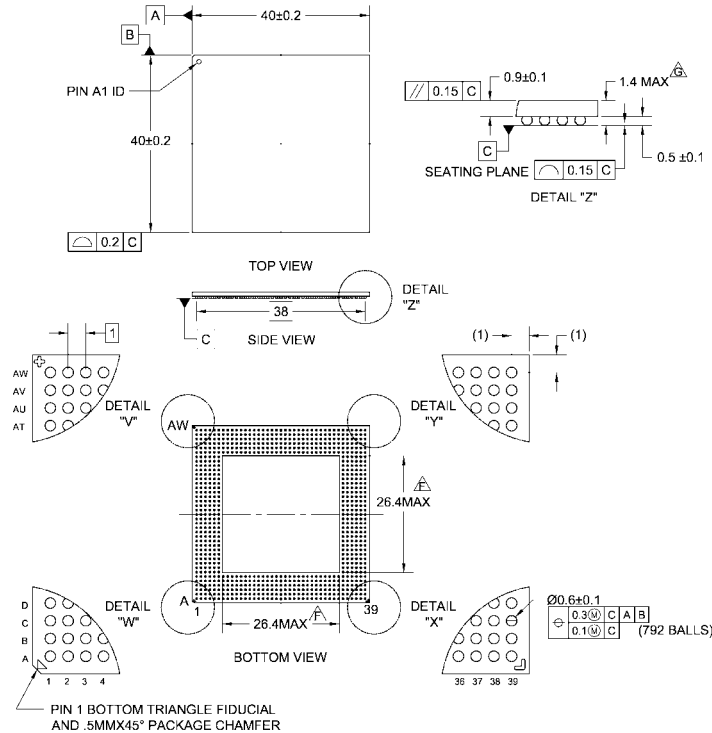
NOTES:
A) ALL DIMENSIONS IN MILLIMETERS.
B) CONFORMS TO JEDEC MO-149. Varaition (AN-1X)
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
D) ROW NAMING ORDER; A B C D E F G H J K L M N P R T U V W Y
   AA AB AC AD AE AF AG AH AJ AK AL AM AN AP AR AT AU AV AW
E) COLUMN NAMING ORDER; 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
   18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
F) ENCAPSULATION SIZE WILL VARY WITH CAVITY SIZE.
G) MAX STAND OFF FROM PCB AFTER MOUNTING.

BGA792ArevA

**792-Ball Thermally-Enhanced Ball Grid Array (TBGA), JEDEC MO-149, 1.0mm pitch, 40mm Square
Package Number BGA792A**

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