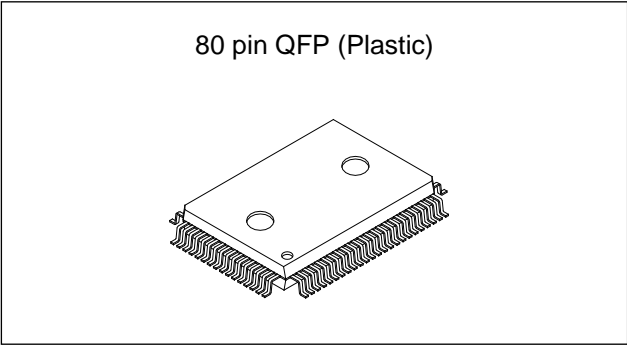


**CD-G Decoder**

**Description**

The CXD1807Q has functions to decode CD-G commands written in the CD subcode and write them into the DRAM to display them. It also has a built-in RGB 4-bit D/A converter. By adding 256K bits of DRAM and a video encoder, a CD graphics system can be configured.



**Functions**

- Real-time correction of subcode errors
- Powerful protection circuit for subcode synchronization
- RAM for color look-up table
- Compatible with both NTSC and PAL
- 4-bit DAC for RGB
- 80-pin QFP

**Applications**

CD-G decoder

**Structure**

Silicon gate CMOS IC

**Absolute Maximum Ratings** (Ta = 25°C)

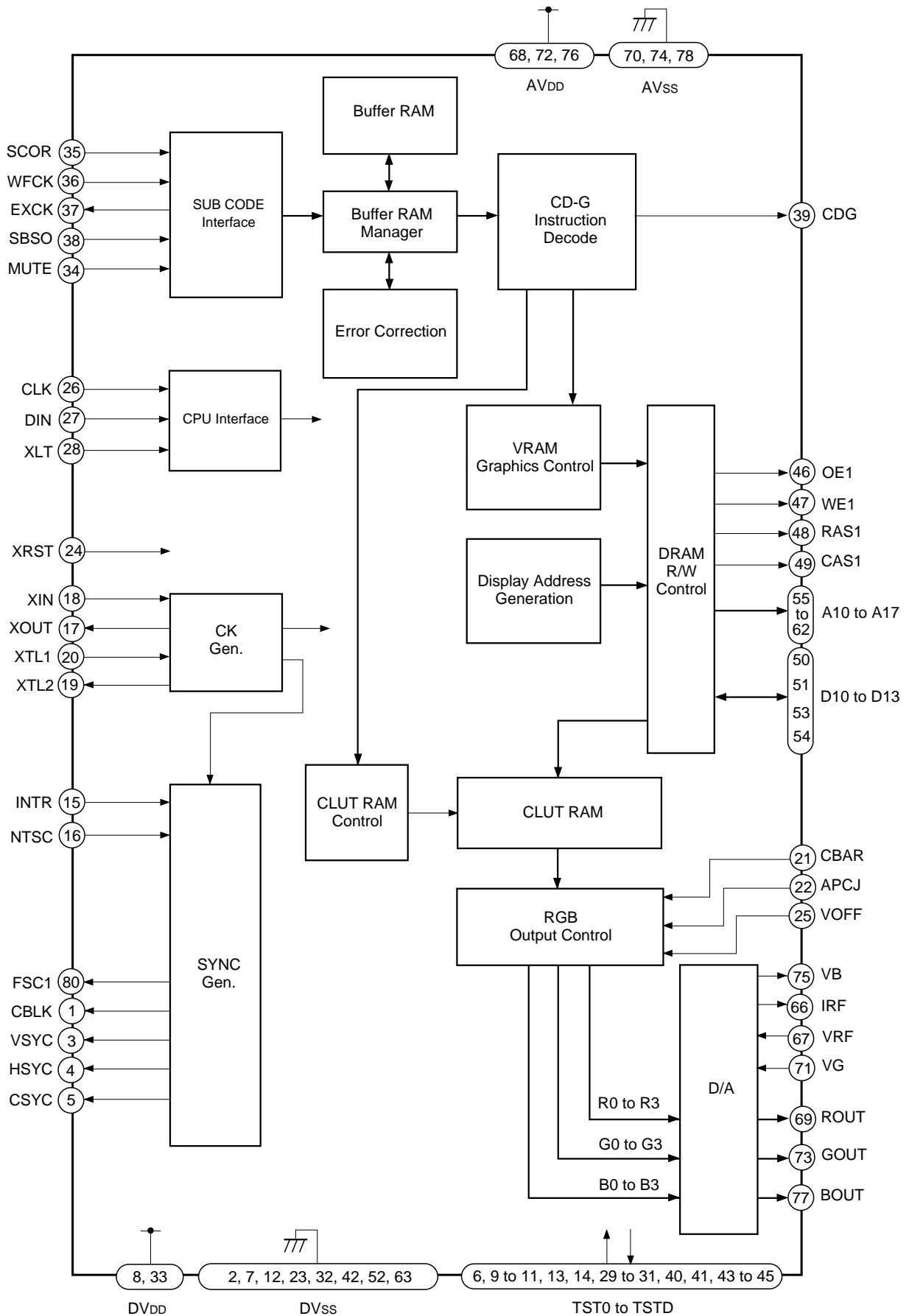
|                         |                  |                                              |    |
|-------------------------|------------------|----------------------------------------------|----|
| • Supply voltage        | V <sub>DD</sub>  | V <sub>SS</sub> -0.5 to +7.0                 | V  |
| • Input voltage         | V <sub>I</sub>   | V <sub>SS</sub> -0.5 to V <sub>DD</sub> +0.5 | V  |
| • Output voltage        | V <sub>O</sub>   | V <sub>SS</sub> -0.5 to V <sub>DD</sub> +0.5 | V  |
| • Operating temperature | T <sub>opr</sub> | -20 to +75                                   | °C |
| • Storage temperature   | T <sub>stg</sub> | -55 to +150                                  | °C |

**Recommended Operating Conditions**

|                       |                  |            |    |
|-----------------------|------------------|------------|----|
| • Supply voltage      | DV <sub>DD</sub> | 5±0.5      | V  |
|                       | AV <sub>DD</sub> | 5±0.5      | V  |
| • Ambient temperature | T <sub>a</sub>   | -20 to +75 | °C |

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Block Diagram



## Pin Description

| Pin No. | Symbol | I/O | Description                                               |
|---------|--------|-----|-----------------------------------------------------------|
| 1       | CBLK   | O   | Composite blanking signal; negative logic                 |
| 2       | DVss   | —   | Digital ground                                            |
| 3       | VSYC   | O   | Vertical sync signal; negative logic                      |
| 4       | HSYC   | O   | Horizontal sync signal; negative logic                    |
| 5       | CSYC   | O   | Composite sync signal; negative logic                     |
| 6       | TST8   | O   | Test pin                                                  |
| 7       | DVss   | —   | Digital ground                                            |
| 8       | DVDD   | —   | Digital power supply                                      |
| 9       | TST9   | O   | Test pin                                                  |
| 10      | TST4   | I   | Test pin                                                  |
| 11      | TST5   | I   | Test pin                                                  |
| 12      | DVss   | —   | Digital ground                                            |
| 13      | TST6   | I   | Test pin                                                  |
| 14      | TST7   | I   | Test pin                                                  |
| 15      | INTR   | I   | Interlace/non-interlace (High/Low) switching signal       |
| 16      | NTSC   | I   | NTSC/PAL (High/Low) select signal                         |
| 17      | XOUT   | O   | 14.31818MHz (NTSC 4fsc) crystal oscillator circuit output |
| 18      | XIN    | I   | 14.31818MHz (NTSC 4fsc) crystal oscillator circuit input  |
| 19      | XTL2   | O   | 17.734475MHz (PAL 4fsc) crystal oscillator circuit output |
| 20      | XTL1   | I   | 17.734475MHz (PAL 4fsc) crystal oscillator circuit input  |
| 21      | CBAR   | I   | Color bar output select signal; positive logic            |
| 22      | APCJ   | I   | APC-adjusting input signal; positive logic                |
| 23      | DVss   | —   | Digital ground                                            |
| 24      | XRST   | I   | Reset input signal; negative logic                        |
| 25      | VOFF   | I   | R, G, B output mute select signal; positive logic         |
| 26      | CLK    | I   | Data write clock signal from CPU                          |
| 27      | DIN    | I   | Serial data input signal from CPU                         |
| 28      | XLT    | I   | Data latch signal from CPU                                |
| 29      | TSTA   | O   | Test pin                                                  |
| 30      | TSTB   | O   | Test pin                                                  |
| 31      | TSTC   | O   | Test pin                                                  |
| 32      | DVss   | —   | Digital ground                                            |
| 33      | DVDD   | —   | Digital power supply                                      |
| 34      | MUTE   | I   | Subcode data mute signal; positive logic                  |

| Pin No. | Symbol | I/O | Description                                                            |
|---------|--------|-----|------------------------------------------------------------------------|
| 35      | SCOR   | I   | Subcode sync signal from CD DSP; positive logic                        |
| 36      | WFCK   | I   | Write frame clock signal from CD DSP                                   |
| 37      | EXCK   | O   | Subcode data readout clock signal to CD DSP                            |
| 38      | SBSO   | I   | Subcode data P to W serial input signal from CD DSP                    |
| 39      | CDG    | O   | Disc identification signal                                             |
| 40      | TSTD   | O   | Test pin                                                               |
| 41      | TST3   | I   | Test pin                                                               |
| 42      | DVss   | —   | Digital ground                                                         |
| 43      | TST2   | I   | Test pin                                                               |
| 44      | TST1   | I   | Test pin                                                               |
| 45      | TST0   | I   | Test pin                                                               |
| 46      | OE1    | O   | DRAM output enable signal; negative logic                              |
| 47      | WE1    | O   | DRAM write enable signal; negative logic                               |
| 48      | RAS1   | O   | DRAM row address strobe signal; negative logic                         |
| 49      | CAS1   | O   | DRAM column address strobe signal; negative logic                      |
| 50      | D10    | I/O | DRAM data bus (LSB)                                                    |
| 51      | D11    | I/O | DRAM data bus                                                          |
| 52      | DVss   | —   | Digital ground                                                         |
| 53      | D12    | I/O | DRAM data bus                                                          |
| 54      | D13    | I/O | DRAM data bus (MSB)                                                    |
| 55      | A10    | O   | DRAM address (LSB)                                                     |
| 56      | A11    | O   | DRAM address                                                           |
| 57      | A12    | O   | DRAM address                                                           |
| 58      | A13    | O   | DRAM address                                                           |
| 59      | A14    | O   | DRAM address                                                           |
| 60      | A15    | O   | DRAM address                                                           |
| 61      | A16    | O   | DRAM address                                                           |
| 62      | A17    | O   | DRAM address (MSB)                                                     |
| 63      | DVss   | —   | Digital ground                                                         |
| 64      | N.C.   | —   |                                                                        |
| 65      | N.C.   | —   |                                                                        |
| 66      | IRF    | O   | Connect a resistance 15 times the output resistance.                   |
| 67      | VRF    | I   | Sets the full-scale value of RGB output signal.                        |
| 68      | AVDD1  | —   | Analog power supply for R channel/DA converter                         |
| 69      | ROUT   | O   | Analog red signal output                                               |
| 70      | AVss1  | —   | Analog ground for R channel/DA converter                               |
| 71      | VG     | I   | Connect a power supply through an approximately 0.1 $\mu$ F capacitor. |

| Pin No. | Sumbol            | I/O | Description                                                           |
|---------|-------------------|-----|-----------------------------------------------------------------------|
| 72      | AV <sub>DD2</sub> | —   | Analog power supply for G channel/DA converter                        |
| 73      | GOUT              | O   | Analog green signal output                                            |
| 74      | AV <sub>SS2</sub> | —   | Analog ground for G channel/DA converter                              |
| 75      | VB                | O   | Connect GND through an approximately 0.1 $\mu$ F capacitor.           |
| 76      | AV <sub>DD3</sub> | —   | Analog power supply for B channel/DA converter                        |
| 77      | BOUT              | O   | Analog blue signal output                                             |
| 78      | AV <sub>SS3</sub> | —   | Analog ground for B channel/DA converter                              |
| 79      | N.C.              | —   |                                                                       |
| 80      | FSC1              | O   | 3.58MHz (NTSC), 4.43MHz (PAL) clock output (sub carrier clock signal) |

## Electrical Characteristics

## 1. DC Characteristics

(V<sub>DD</sub> = 5V±10%, V<sub>SS</sub> = 0V, Topr = -20 to +75°C)

| Item                                       | Symbol                              | Conditions                                           | Min.                 | Typ.               | Max.               | Unit |
|--------------------------------------------|-------------------------------------|------------------------------------------------------|----------------------|--------------------|--------------------|------|
| Supply current                             | I <sub>DD</sub>                     | Operating state                                      |                      |                    | 100                | mA   |
| High level input voltage (1)               | V <sub>IH1</sub>                    |                                                      | 2.2                  |                    |                    | V    |
| Low level input voltage (1)                | V <sub>IL1</sub>                    |                                                      |                      |                    | 0.8                | V    |
| High level input voltage (2)               | V <sub>IH2</sub>                    |                                                      | 0.7V <sub>DD</sub>   |                    |                    | V    |
| Low level input voltage (2)                | V <sub>IL2</sub>                    |                                                      |                      |                    | 0.3V <sub>DD</sub> | V    |
| High level input voltage (3)               | V <sub>t1+</sub>                    |                                                      | 2.2                  |                    |                    | V    |
| Low level input voltage (3)                | V <sub>t1-</sub>                    |                                                      |                      |                    | 0.8                | V    |
| TTL Schmitt hysteresis                     | V <sub>t1+</sub> - V <sub>t1-</sub> |                                                      |                      | 0.4                |                    | V    |
| High level input voltage (4)               | V <sub>t2+</sub>                    |                                                      | 0.8V <sub>DD</sub>   |                    |                    | V    |
| Low level input voltage (4)                | V <sub>t2-</sub>                    |                                                      |                      |                    | 0.2V <sub>DD</sub> | V    |
| CMOS Schmitt hysteresis                    | V <sub>t2+</sub> - V <sub>t2-</sub> |                                                      |                      | 0.6                |                    | V    |
| Input current of pull-up input (5)         | I <sub>IN</sub>                     | V <sub>IN</sub> = 0V                                 | -40                  | -100               | -240               | μA   |
| High level output voltage (6)              | V <sub>OH1</sub>                    | I <sub>OH1</sub> = -2mA                              | V <sub>DD</sub> -0.8 |                    |                    | V    |
| Low level output voltage (6)               | V <sub>OL1</sub>                    | I <sub>OL1</sub> = 4mA                               |                      |                    | 0.4                | V    |
| High level output voltage (7)              | V <sub>OH2</sub>                    | I <sub>OH1</sub> = -4mA                              | V <sub>DD</sub> -0.8 |                    |                    | V    |
| Low level output voltage (7)               | V <sub>OL2</sub>                    | I <sub>OL1</sub> = 8mA                               |                      |                    | 0.4                | V    |
| High level output voltage (8)              | V <sub>OH3</sub>                    | I <sub>OH1</sub> = -6mA                              | V <sub>DD</sub> -0.8 |                    |                    | V    |
| Low level output voltage (8)               | V <sub>OL3</sub>                    | I <sub>OL1</sub> = 4mA                               |                      |                    | 0.4                | V    |
| Input leak current                         | I <sub>IL1</sub>                    |                                                      | -10                  |                    | 10                 | μA   |
| Oscillation cell logic threshold           | LV <sub>th</sub>                    |                                                      |                      | 0.5V <sub>DD</sub> |                    | V    |
| Oscillation cell high level input voltage  | V <sub>IH</sub>                     |                                                      | 0.7V <sub>DD</sub>   |                    |                    | V    |
| Oscillation cell low level input voltage   | V <sub>IL</sub>                     |                                                      |                      |                    | 0.3V <sub>DD</sub> | V    |
| Oscillation cell feedback resistance       | R <sub>FB</sub>                     | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>DD</sub> | 250k                 | 1M                 | 2.5M               | Ω    |
| Oscillation cell high level output voltage | V <sub>OH</sub>                     | I <sub>OH</sub> = -3mA                               | 0.5V <sub>DD</sub>   |                    |                    | V    |
| Oscillation cell low level output voltage  | V <sub>OL</sub>                     | I <sub>OL</sub> = 3mA                                |                      |                    | 0.5V <sub>DD</sub> | V    |

## 1-1. Classification of input pins

- (1) TTL level input:  
DIN, XLT, D10 to D13
- (2) CMOS level input:  
INTR, NTSC, SCOR, SBSO, MUTE, APCJ, VOFF, CBAR, TST0 to TST7
- (3) TTL Schmitt input:  
CLK
- (4) CMOS Schmitt input:  
XRST, WFCK
- (5) Pull-up input:  
D10 to D13

**1-2. Classification of output pins**

- (6) Normal output:  
FSC1, CBLK, VSYC, HSYC, CSYC, A10 to A17, D10 to D13, OE1, WE1, EXCK, TST8 to TSTD
- (7) Powered output:  
CDG
- (8) Proportional output:  
RAS1, CAS1

**1-3. Oscillation cell**

Input : XIN, XTL1  
Output : XOUT, XTL2

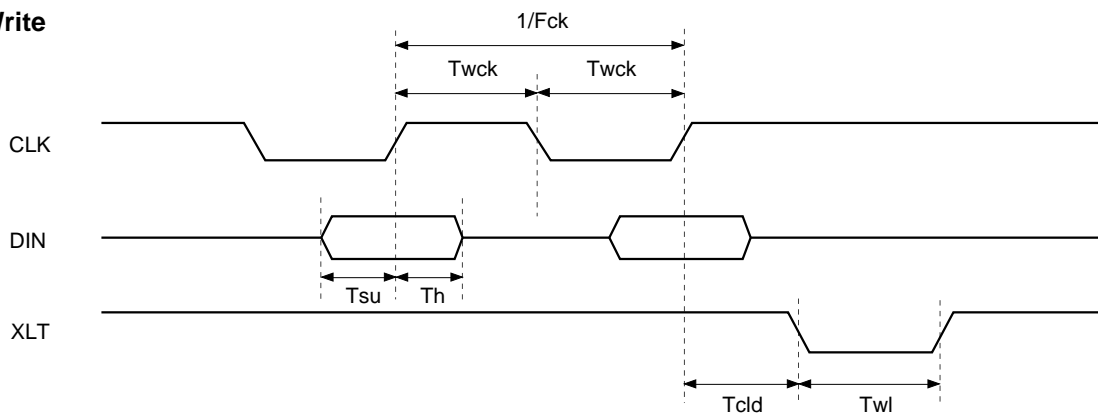
**1-4. I/O pin capacitances** ( $V_{DD} = V_I = 0V, f = 1MHz$ )

| Item             | Symbol           | Min. | Typ. | Max. | Unit |
|------------------|------------------|------|------|------|------|
| Input pin        | C <sub>IN</sub>  |      |      | 9    | pF   |
| Output pin       | C <sub>OUT</sub> |      |      | 11   | pF   |
| Input/output pin | C <sub>I/O</sub> |      |      | 11   | pF   |

**2. AC Characteristics** ( $V_{DD} = 5V \pm 10\%, V_{SS} = 0V, T_{opr} = -20$  to  $+75^\circ C, Output Load = 75pF$ )

**2-1. CPU interface**

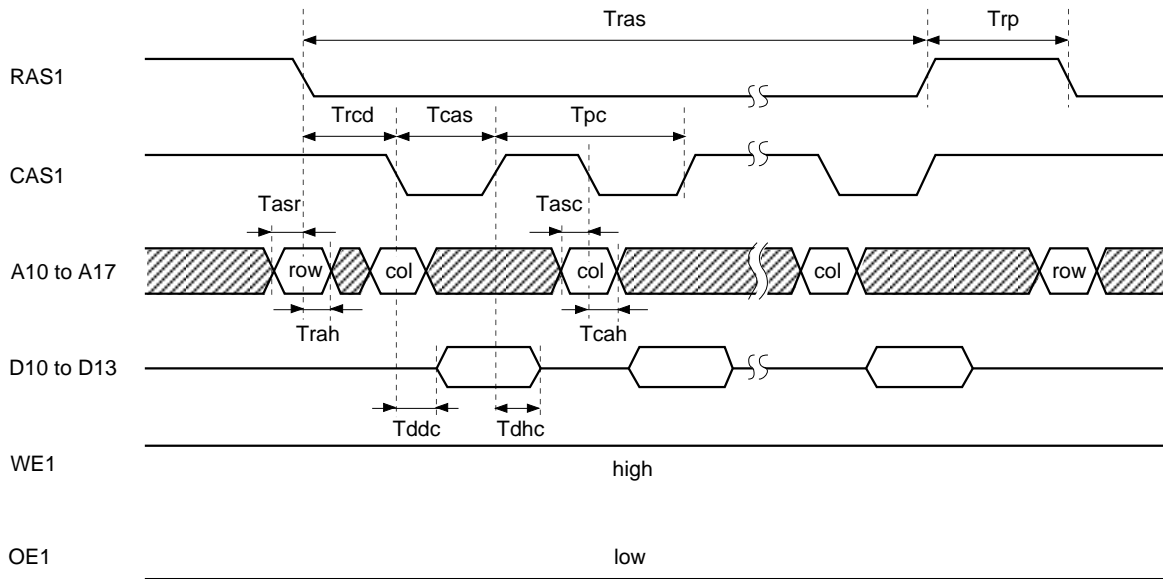
**(1) Write**



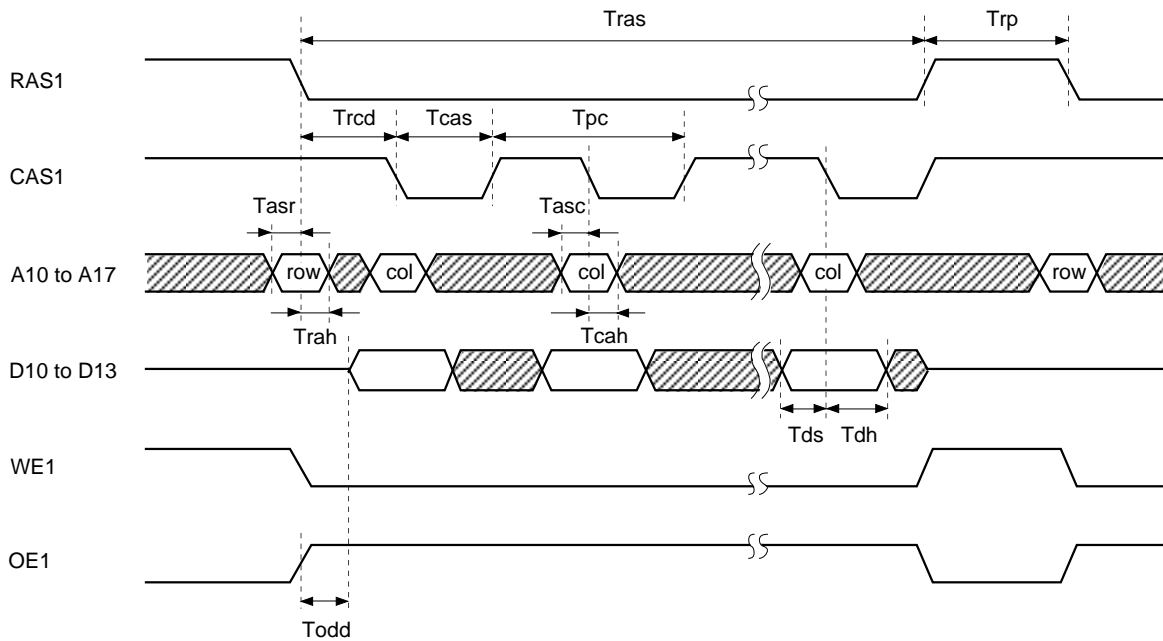
| Item                   | Symbol | Min. | Typ. | Max. | Unit |
|------------------------|--------|------|------|------|------|
| Clock frequency        | Fck    |      |      | 0.65 | MHz  |
| Clock pulse width      | Twck   | 750  |      |      | ns   |
| Setup time (for CLK ↑) | Tsu    | 300  |      |      | ns   |
| Hold time (for CLK ↑)  | Th     | 300  |      |      | ns   |
| CLK – XLT delay time   | Tcld   | 300  |      |      | ns   |
| Latch pulse width      | Twl    | 750  |      |      | ns   |

2-2. DRAM interface

(1) Read (page mode)



(2) Write (page mode)

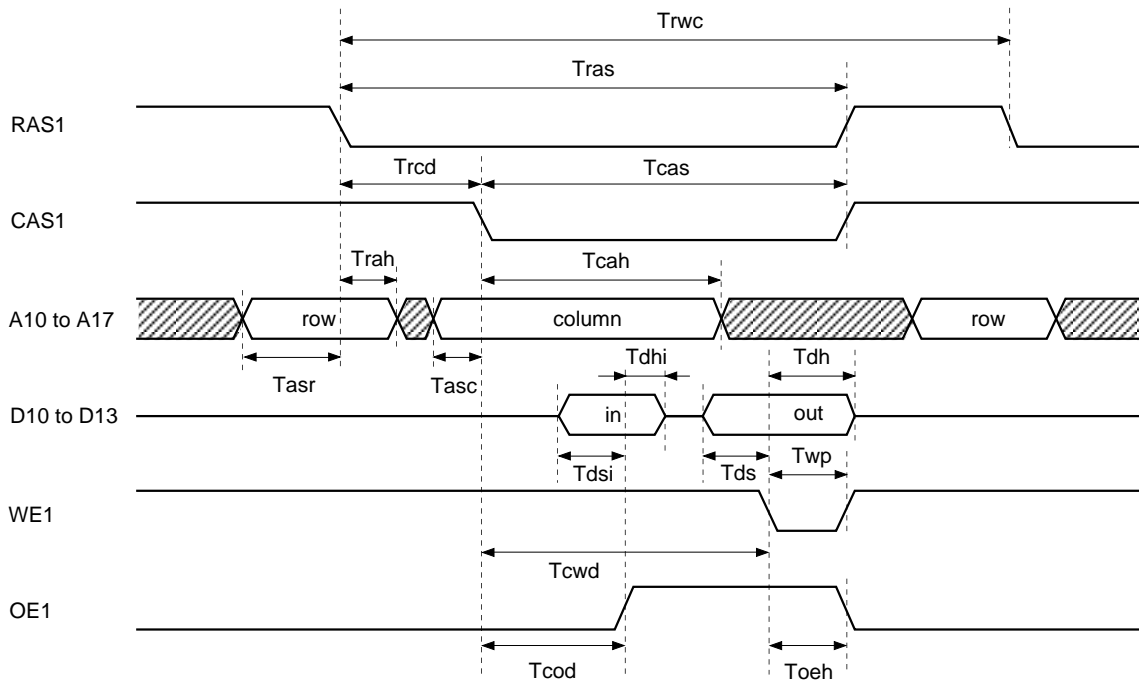




( $T_w = 1/f$ , f: master clock frequency)

| Item                                   | Symbol | Min.        | Typ.   | Max.       | Unit |
|----------------------------------------|--------|-------------|--------|------------|------|
| RAS pulse width                        | Tras   | $3T_w - 10$ |        |            | ns   |
| RAS precharge width                    | Trp    |             | $2T_w$ |            | ns   |
| RAS – CAS delay time                   | Trcd   |             | $2T_w$ |            | ns   |
| CAS pulse width                        | Tcas   |             | $T_w$  |            | ns   |
| Page mode cycle time                   | Tpc    |             | $2T_w$ |            | ns   |
| Row address setup time (for RAS, ↓)    | Tasr   | $2T_w - 45$ |        |            | ns   |
| Row address hold time (for RAS, ↓)     | Trah   | $T_w - 15$  |        |            | ns   |
| Column address setup time (for CAS, ↓) | Tasc   | $T_w - 35$  |        |            | ns   |
| Column address hold time (for CAS, ↓)  | Tcah   | $T_w$       |        |            | ns   |
| Data input delay time (for CAS, ↓)     | Tddc   |             |        | $T_w - 10$ | ns   |
| Data float time (relative to CAS, ↑)   | Tdhc   | 10          |        |            | ns   |
| Data output setup time (for CAS, ↓)    | Tds    | $T_w - 50$  |        |            | ns   |
| Data output hold time (for CAS, ↓)     | Tdh    | $T_w - 15$  |        |            | ns   |
| Data output delay time (for OE, ↑)     | Todd   | $T_w$       |        |            | ns   |

**(3) Read modify write**



(Tw = 1/f, f: master clock frequency)

| Item                                  | Symbol | Min.     | Typ. | Max. | Unit |
|---------------------------------------|--------|----------|------|------|------|
| RAS pulse width                       | Tras   |          | 7Tw  |      | ns   |
| Read/write cycle                      | Trwc   |          | 9Tw  |      | ns   |
| RAS-CAS delay time                    | Trcd   |          | 2Tw  |      | ns   |
| CAS pulse width                       | Tcas   |          | 5Tw  |      | ns   |
| CAS-WE delay time                     | Tc wd  |          | 4Tw  |      | ns   |
| WE pulse width                        | Twp    |          | Tw   |      | ns   |
| OE hold time (for WE ↓)               | Toeh   |          | Tw   |      | ns   |
| CAS-OE delay time                     | Tcod   |          | 2Tw  |      | ns   |
| Row address setup time (for RAS ↓)    | Tasr   | 2Tw – 45 |      |      | ns   |
| Row address hold time (for RAS ↓)     | Trah   | Tw – 15  |      |      | ns   |
| Column address setup time (for CAS ↓) | Tasc   | Tw – 35  |      |      | ns   |
| Column address hold time (for CAS ↓)  | Tcah   | 5Tw      |      |      | ns   |
| Data input setup time (for OE ↑)      | Tdsi   | 35       |      |      | ns   |
| Data input hold time (for OE ↑)       | Tdhi   | 0        |      |      | ns   |
| Data output setup time (for WE ↓)     | Tds    | Tw – 50  |      |      | ns   |
| Data output hold time (for WE ↓)      | Tdh    | Tw – 15  |      |      | ns   |

### 3. Built-in DAC Characteristics

#### Recommended operating conditions

| Item                    | Symbol              | Ratings    | Unit |
|-------------------------|---------------------|------------|------|
| Supply voltage          | AVDD1, AVDD2, AVDD3 | 4.5 to 5.5 | V    |
| Reference input voltage | VRF                 | 0.5 to 2.0 | V    |

#### Electrical characteristics

(VDD = 5V, VRF = 2V, R = 200Ω, Ta = 25°C)

| Item                                   | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|----------------------------------------|--------|------------|------|------|------|------|
| Resolution                             | n      |            |      | 4    |      | bit  |
| Differential linearity error           | ED     |            | -0.5 |      | +0.5 | LSB  |
| Integral linearity error               | EL     |            | -1.0 |      | +1.0 | LSB  |
| Full-scale output voltage              | VFS    |            | 1.9  | 2.0  | 2.1  | V    |
| Full-scale output current              | IFS    |            |      | 10   | 15   | mA   |
| Assured precision output voltage range | Voc    |            | 0.5  | 2.0  | 2.1  | V    |

## Description of Functions

### 1. Pin Description

#### 1-1. Subcode data interface

Inputs subcode data and subcode sync detection signals using the following pins. These pins can be directly connected to Sony signal processing LSI for CD.

- 1) SCOR  
Inputs the signal that indicates detection of either subcode sync S0 or S1. Connect this pin to the SCOR pin of CD DSP.
- 2) WFCK  
Inputs WFCK (Write Frame Clock). Connect this pin to the WFCK pin of CD DSP.
- 3) EXCK  
Outputs the clock to read data from the SBSO pin. Connect this pin to the EXCK pin of CD DSP.
- 4) SBSO  
Serially inputs the subcode data P to W. Connect this pin to the SBSO pin of CD DSP.
- 5) MUTE  
Inputs the signal to mute subcode data inputs. This pin is in the mute state when High signal is input.

#### 1-2. CPU interface

Inputs data and sends commands to the CXD1807Q using the following pins.

- 1) CLK  
Inputs the clock to input serial data from the external CPU.
- 2) DIN  
Inputs serial data from the external CPU.
- 3) XLT  
Inputs the signal to latch serial data from the external CPU. The pin latches serial data at the falling edge of this signal.

#### 1-3. DRAM interface

The screen data are stored in the external DRAM. The DRAM read/write function is controlled using the following pins. Use a 64K × 4-bit DRAM with an access time of 100ns or less.

- 1) RAS1  
Indicates the row address is effective. Connect this pin to the RAS pin of the external DRAM.
- 2) CAS1  
Indicates the column address is effective. Connect this pin to the CAS pin of the external DRAM.
- 3) A10 to A17 (8 pins)  
Outputs DRAM addresses. Connect these pins to the A0 to A7 pins of the external DRAM, respectively.
- 4) D10 to D13 (4 pins)  
Inputs and outputs DRAM data. Connect these pins to the D0 to D3 pins of the external DRAM, respectively.
- 5) WE1  
Outputs the write enable signal of DRAM. Connect this pin to the WE pin of the external DRAM.
- 6) OE1  
Outputs the output enable signal of DRAM. Connect this pin to the OE pin of the external DRAM.

#### 1-4. Sync signal generation

Various sync signals are output from the following pins by dividing the clock frequency.

- 1) INTR  
Switches either interlace or non-interlace to display the image. The interlace display selected for High.
- 2) NTSC  
Inputs the signal for selecting either NTSC or PAL mode to output the sync signal. The NTSC mode selected for High.
- 3) FSC1  
Outputs the signal with a quarter frequency of clock input to the XIN pin (NTSC) or to the XTL1 pin (PAL). This signal has the same frequency as the color signal subcarrier.
- 4) CBLK  
Outputs the composite blanking signal. Switched to Low during the blanking period.
- 5) VSYC  
Outputs the vertical sync signal. Negative logic.
- 6) HSYC  
Outputs the horizontal sync signal. Negative logic.
- 7) CSYC  
Outputs the composite sync signal. Negative logic.

#### 1-5. RGB data output

- 1) VOFF  
Mute input for R, G, and B outputs. When this pin is set to High, all the screens for the RGB output show the color set by the external CPU; the initial color setting is blue.
- 2) CBAR  
When this pin is set to High, a color bar pattern is output from the RGB pin; the bar width varies with the color.
- 3) APCJ  
When this pin is set to High, a black-and-white cross-hatch screen is output from the RGB pin.
- 4) ROUT  
The red data analog output. It can be extracted by connecting a resistor; an output resistance of 200 $\Omega$  should be connected.
- 5) GOUT  
The green data analog output. It can be extracted by connecting a resistor; an output resistance of 200 $\Omega$  should be connected.
- 6) BOUT  
The blue data analog output. It can be extracted by connecting a resistor; an output resistance of 200 $\Omega$  should be connected.
- 7) VB  
Connect this pin to ground through a capacitor of approximately 0.1 $\mu$ F.
- 8) IRF  
Connect a resistor equal to 15 times the RGB signal output resistance (3k $\Omega$  resistance).
- 9) VRF  
Sets the full-scale output value through external resistance dividing.
- 10) VG  
Connect this pin to a power supply through a capacitor of approximately 0.1 $\mu$ F.

**1-6. Clock**

## 1) XIN, XOUT

In the NTSC mode, input the master clock (14.31818MHz) of this LSI. An oscillation circuit can be made by connecting X'TAL to the XIN and XOUT pins. (The capacitor values depend on the crystal oscillator.)  
When not used, XIN should be connected to GND.

## 2) XTL1, XTL2

In the PAL mode, input the master clock (17.734475MHz) of this LSI. An oscillation circuit can be made by connecting the X'TAL to the XTL1 and XTL2 pins. (The capacitor values depend on the crystal oscillator.)  
When not used, XTL1 should be connected to GND.

**1-7. Others**

## 1) XRST

Reset input. When this pin is set to Low, this LSI is reset.

## 2) CDG

The output goes to High after detection of a subcode input CD-G command. This signal is cleared by a reset input from the XRST pin.

## 3) TST0 to TSTD

Test pins. (These pins used for the shipping test of the LSI.)  
Fix the TST0 to TST7 pins to Low.

**2. CPU Interface**

Each command can be input to this LSI by inputting address or data to the three pins; DIN, XLT and CLK, with the timing shown in Fig. 1.

**Description of Each Command**

The following explains the various functions of each command. The relations between the address and data of each command are summarized in Table 1.

**2-1. Color setting commands for VOFF (address = CH)**

The VOFF pin can make the screen monochromatic; the color then used is set using this command.

| D7         | D6 | D5    | D4          | D3 | D2 | D1 | D0 |
|------------|----|-------|-------------|----|----|----|----|
| RGB select |    | (MSB) | colour data |    |    | —  | —  |

The color is set using 4 bits for each of R, G and B. RGB select is used to select which of the colors R, G or B is to be set.

| D7 | D6 | Color selected |
|----|----|----------------|
| 0  | 0  | Red            |
| 0  | 1  | Green          |
| 1  | 0  | Blue           |
| 1  | 1  | Don't care     |

On reset, the values Red=[0000], Green=[0000], Blue=[1111] are set.

**2-2. Graphic channel setting command (address = DH)**

This command sets and releases each of the 16 graphic channels.

|                   |    |    |    |            |    |    |    |
|-------------------|----|----|----|------------|----|----|----|
| D7                | D6 | D5 | D4 | D3         | D2 | D1 | D0 |
| (MSB) Channel No. |    |    |    | Channel ON | —  | —  | —  |

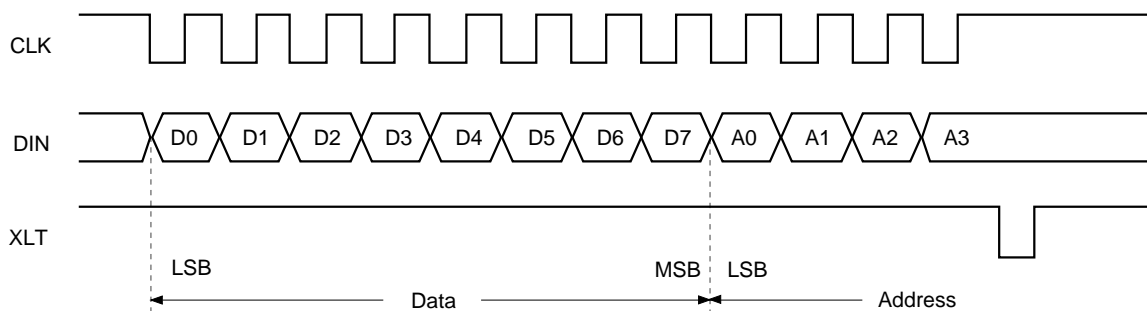
(1) Channel ON

High ... The channel selected by the channel No. is set to High.

Low ... The channel selected by the channel No. is reset to Low.

Of the CD-G commands, the Write FONT and EOR FONT commands are executed only when the channel No. for those commands is set. On reset, only CH0 and CH1 can be set and the others are released.

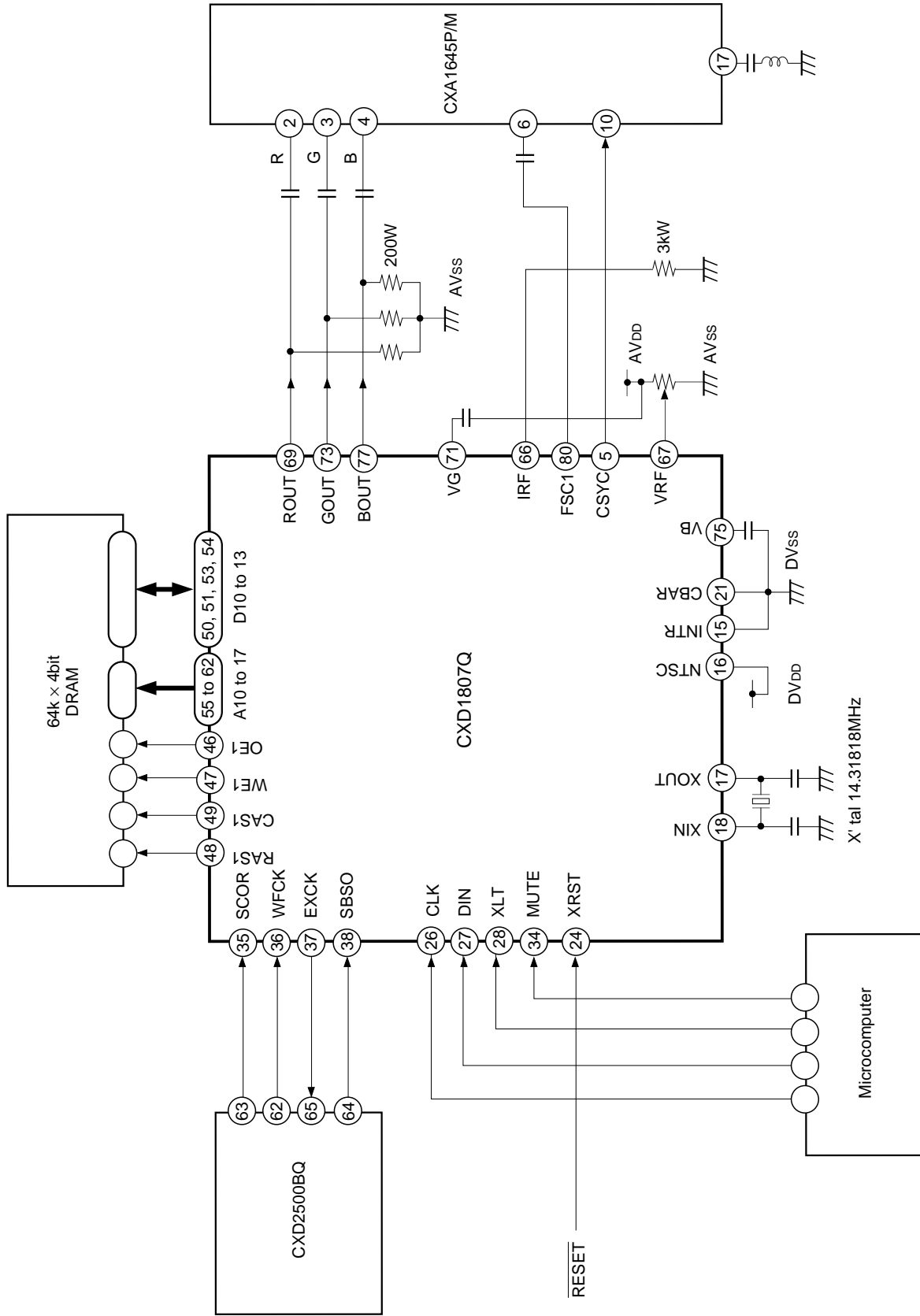
**Fig. 1. CPU interface data format**



**Table 1. List of CPU commands**

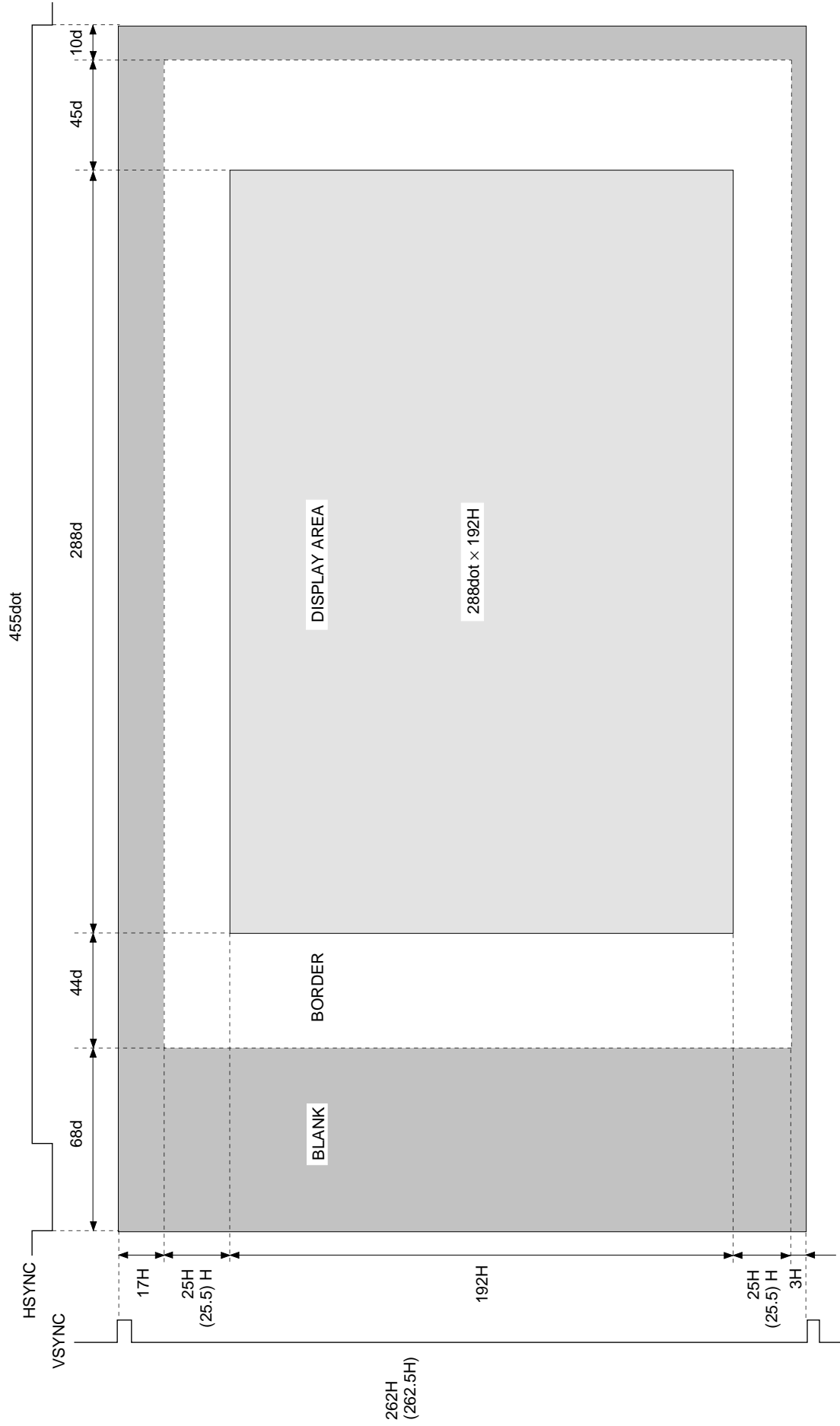
| Register name | Command                 | Address |    |    |    | Data 1      |                       |    |                       | Data 2 |    |    |    |
|---------------|-------------------------|---------|----|----|----|-------------|-----------------------|----|-----------------------|--------|----|----|----|
|               |                         | A3      | A2 | A1 | A0 | D7          | D6                    | D5 | D4                    | D3     | D2 | D1 | D0 |
| 6             | Reserved                | 0       | 1  | 1  | 0  |             |                       |    |                       |        |    |    |    |
| 7             | Reserved                | 0       | 1  | 1  | 1  |             |                       |    |                       |        |    |    |    |
| 8             | Reserved                | 1       | 0  | 0  | 0  |             |                       |    |                       |        |    |    |    |
| 9             | Reserved                | 1       | 0  | 0  | 1  |             |                       |    |                       |        |    |    |    |
| A             | Reserved                | 1       | 0  | 1  | 0  |             |                       |    |                       |        |    |    |    |
| B             | Reserved                | 1       | 0  | 1  | 1  |             |                       |    |                       |        |    |    |    |
| C             | Color setting for VOFF  | 1       | 1  | 0  | 0  | RGB Select  | Color Data (MSB 2bit) |    | Color Data (LSB 2bit) |        | —  | —  |    |
| D             | Graphic channel setting | 1       | 1  | 0  | 1  | Channel No. |                       |    | ch-ON                 | —      | —  | —  |    |
| E             | Reserved                | 1       | 1  | 1  | 0  |             |                       |    |                       |        |    |    |    |
| F             | Reserved                | 1       | 1  | 1  | 1  |             |                       |    |                       |        |    |    |    |

Application Circuit (NTSC mode)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

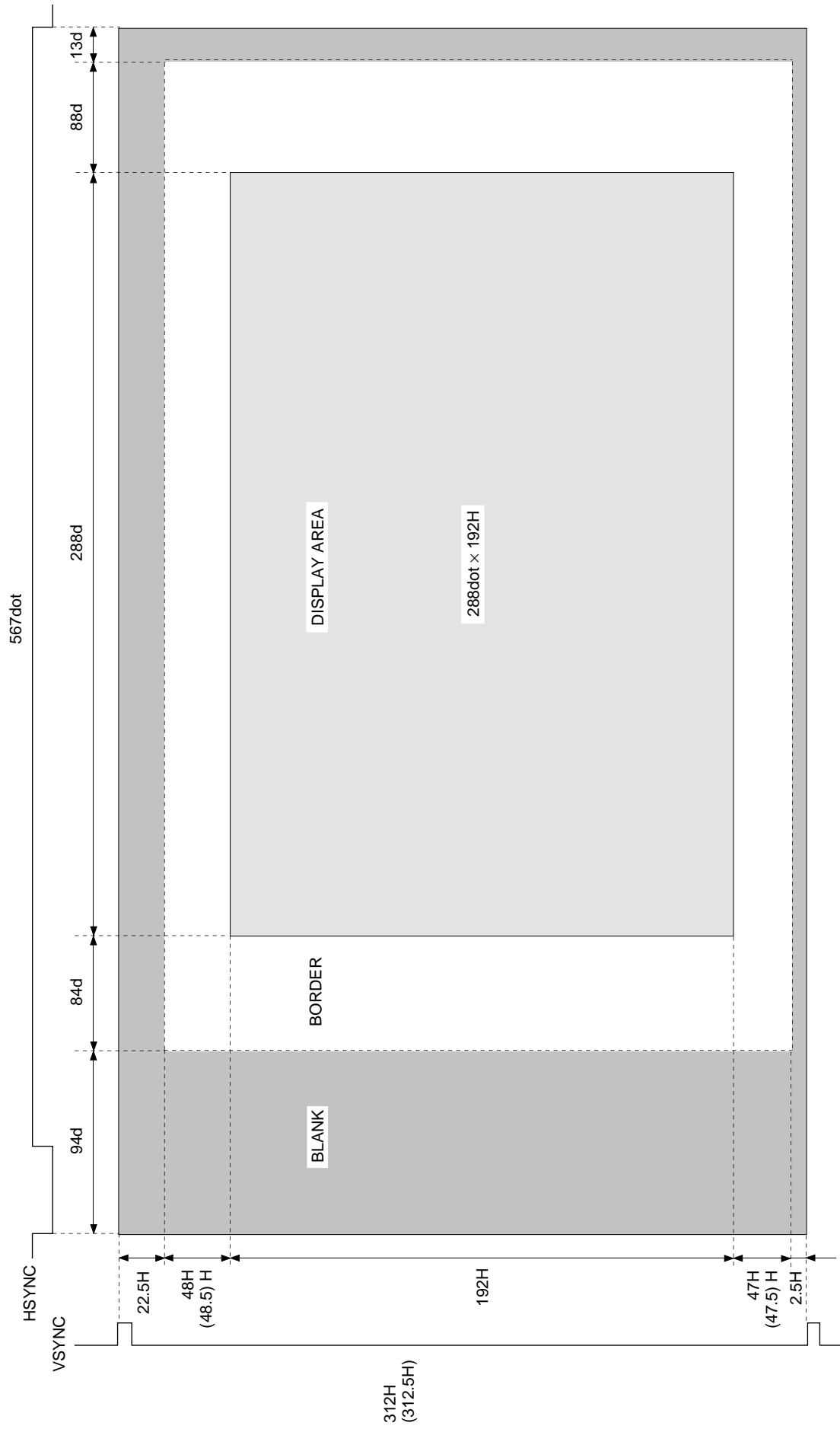
Fig.2. NTSC Screen Composition



( ) Interface display inside parentheses.



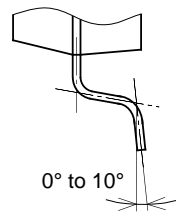
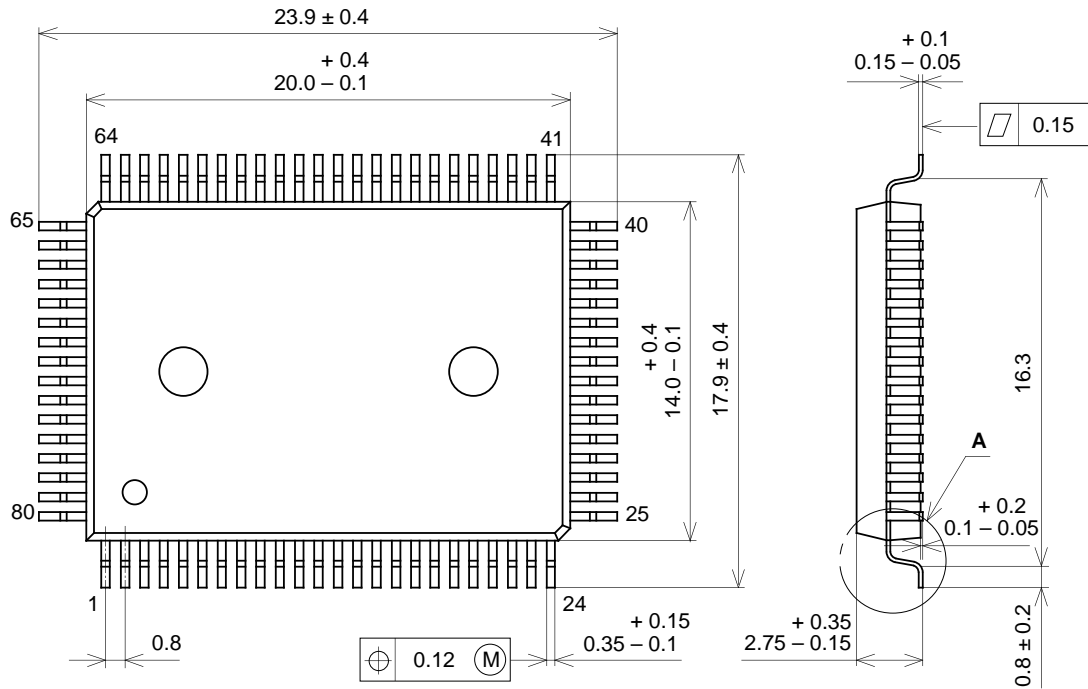
Fig. 3. PAL Screen Composition



( ) Interlace display inside parentheses.

Package Outline Unit: mm

80PIN QFP (PLASTIC)



DETAIL A

|            |                  |
|------------|------------------|
| SONY CODE  | QFP-80P-L01      |
| EIAJ CODE  | *QFP080-P-1420-A |
| JEDEC CODE | _____            |

PACKAGE STRUCTURE

|                  |                   |
|------------------|-------------------|
| PACKAGE MATERIAL | EPOXY RESIN       |
| LEAD TREATMENT   | SOLDER PLATING    |
| LEAD MATERIAL    | COPPER / 42 ALLOY |
| PACKAGE WEIGHT   | 1.6g              |