SONY

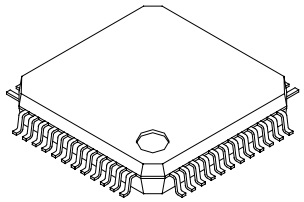
CXA3026AQ

8-bit 140MSPS Flash A/D Converter

Description

The CXA3026AQ is an 8-bit high-speed flash A/D converter capable of digitizing analog signals at the maximum rate of 140MSPS. ECL, PECL or TTL can be selected as the digital input level in accordance with the application. The TTL digital output level allows 1:2 demultiplexed output.

48 pin QFP (Plastic)



LEAD TREATMENT: PALLADIUM PLATING

Features

- Differential linearity error: ±0.5LSB or less
- Integral linearity error: ±0.5LSB or less
- High-speed operation with a maximum conversion rate of 140MSPS
- Low input capacitance: 21 pF
- Wide analog input bandwidth: 150 MHz
- Low power consumption: 790 mW
- Low error rate
- Excellent temperature characteristics
- 1:2 demultiplexed output
- 1/2 frequency divided clock output (with reset function)
- Compatible with ECL, PECL and TTL digital input levels
- Single +5 V power supply operation available
- Surface mounting package

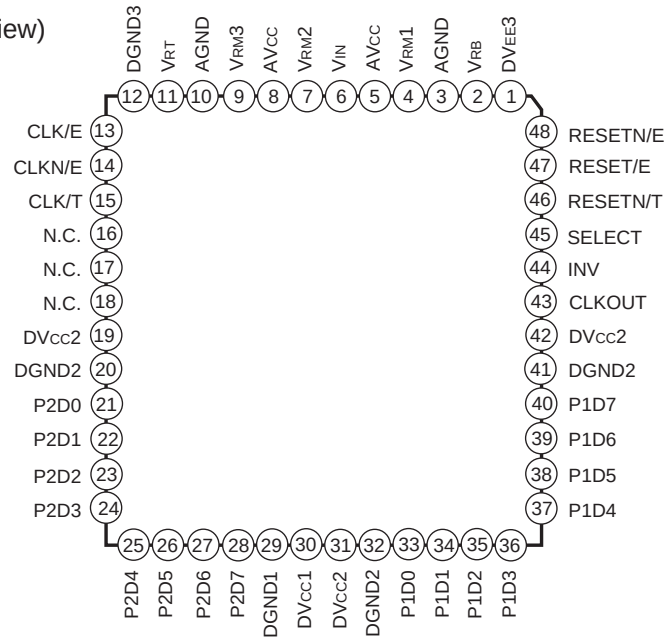
Structure

Bipolar silicon monolithic IC

Applications

- Magnetic recording (PRML)
- Communications (QPSK, QAM)
- LCDs
- Digital oscilloscopes

Pin Configuration (Top View)



E96304C92

Absolute Maximum Ratings (Ta = 25 °C)

			Unit
• Supply voltage	AV_{CC}, $DV_{CC}1$, $DV_{CC}2$	–0.5 to +7.0	V
	DGND3	–0.5 to +7.0	V
	$DV_{EE}3$	–7.0 to +0.5	V
	DGND3 – $DV_{EE}3$	–0.5 to +7.0	V
• Analog input voltage	V_{IN}	V_{RT} – 2.7 to AV_{CC}	V
• Reference input voltage	V_{RT}	2.7 to AV_{CC}	V
	V_{RB}	V_{IN} – 2.7 to AV_{CC}	V
	$\|V_{RT} - V_{RB}\|$	2.5	V
• Digital input voltage	ECL (∗∗∗/E∗1)	$DV_{EE}3$ to +0.5	V
	PECL (∗∗∗/E)	–0.5 to DGND3	V
	TTL (∗∗∗/T, INV)	–0.5 to $DV_{CC}1$	V
	other (SELECT)	–0.5 to $DV_{CC}1$	V
	VID∗2 (|∗∗∗/E – ∗∗∗N/E|)	2.7	V
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	2	W

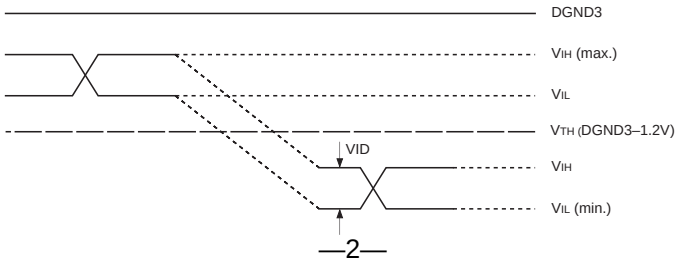
(when mounted on a glass fabric base epoxy board with 50mm x 50mm, 1.6mm thick)

Recommended Operating Conditions

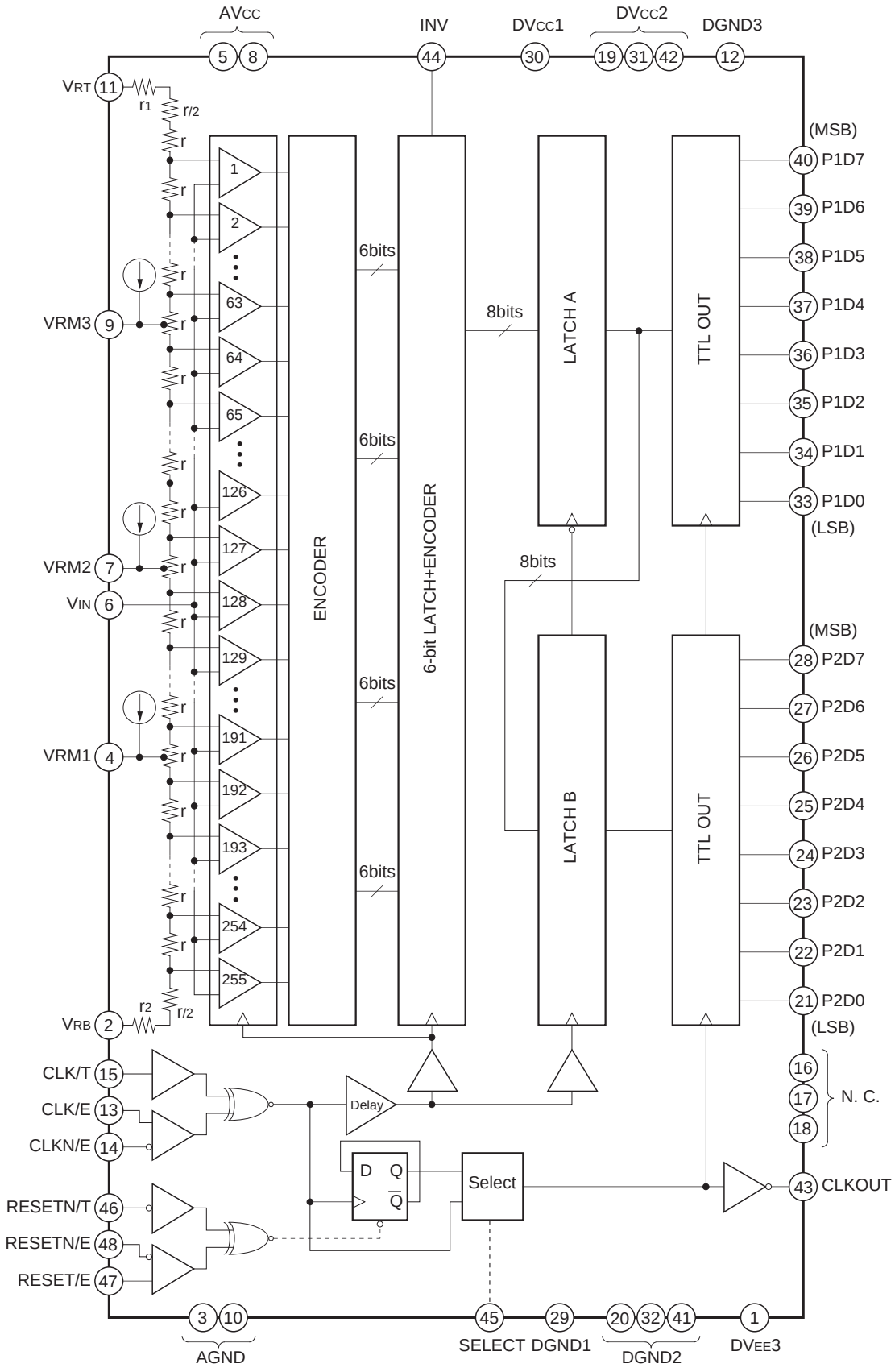
			With a single power supply			With dual power supplies			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
• Supply voltage	$DV_{CC}1$, $DV_{CC}2$, AV_{CC}		+4.75	+5.0	+5.25	+4.75	+5.0	+5.25	V
	DGND1, DGND2, AGND		–0.05	0	+0.05	–0.05	0	+0.05	V
	DGND3		+4.75	+5.0	+5.25	–0.05	0	+0.05	V
	$DV_{EE}3$		–0.05	0	+0.05	–5.5	–5.0	–4.75	V
• Analog input voltage	V_{IN}		V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
• Reference input voltage	V_{RT}		+2.9		+4.1	+2.9		+4.1	V
	V_{RB}		+1.4		+2.6	+1.4		+2.6	V
	$\|V_{RT} - V_{RB}\|$		1.5		2.1	1.5		2.1	V
• Digital input voltage	ECL (∗∗∗/E)	: V_{IH}			DGND3 – 1.05			DGND3 – 0.5	V
		: V_{IL}			DGND3 – 3.2			DGND3 – 1.4	V
	PECL (∗∗∗/E)	: V_{IH}	DGND3 – 1.05		DGND3 – 0.5				V
		: V_{IL}	DGND3 – 3.2		DGND3 – 1.4				V
	TTL (∗∗∗/T, INV)	: V_{IH}	2.0			2.0			V
		: V_{IL}			0.8			0.8	V
	other (SELECT)	: V_{IH}		$DV_{CC}1$			$DV_{CC}1$		V
		: V_{IL}		DGND1			DGND1		V
	VID∗2 (|∗∗∗/E – ∗∗∗N/E|)		0.4	0.8		0.4	0.8		V
• Maximum conversion rate	Fc (Straight mode)		100			100			MSPS
	(DMUX mode)		140			140			MSPS
• Ambient temperature	Ta		–20		+75	–20		+75	°C

∗1 ∗∗∗/E and ∗∗∗/T indicate CLK/E and CLK/T, etc. for the pin name.
∗2 VID: Input Voltage Differential

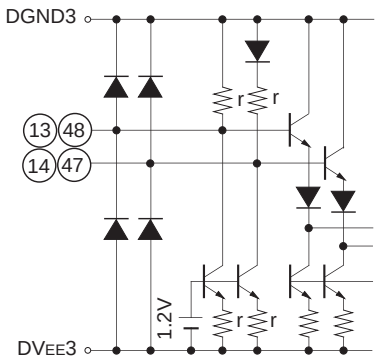
ECL and PECL switching level

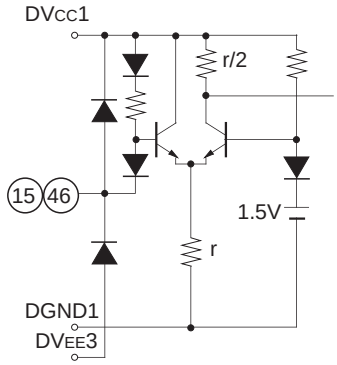
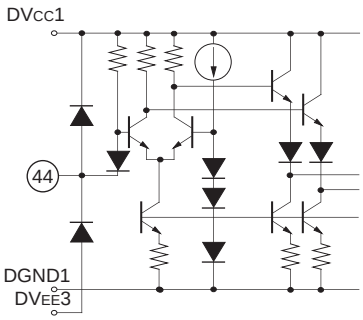
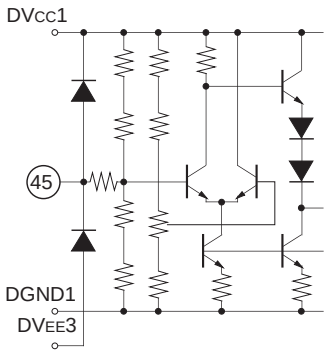


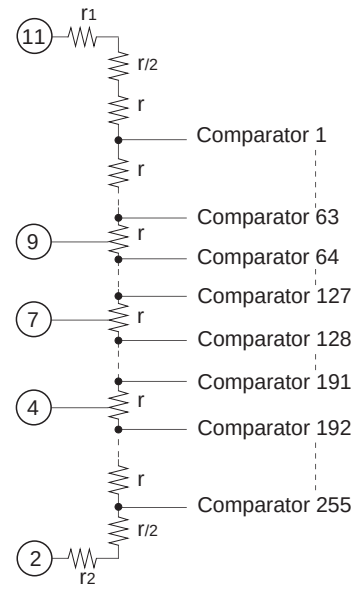
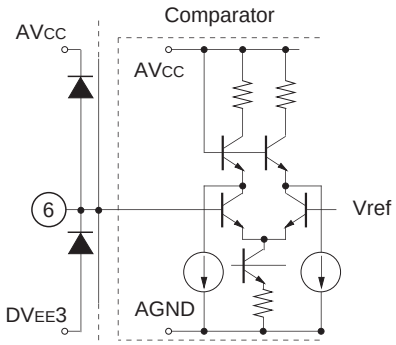
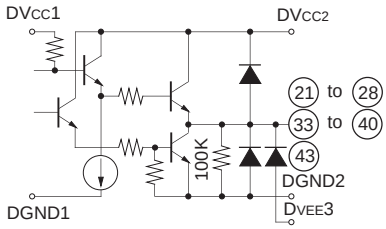
Block Diagram



Pin Description and I/O Pin Equivalent Circuit

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
3, 10	AGND		GND		Analog ground. Separated from the digital ground.
5, 8	AV_{CC}		+5 V (typ.)		Analog power supply. Separated from the digital power supply.
20, 29 32, 41	DGND1 DGND2		GND		Digital ground.
19, 30 31, 42	$DV_{CC}1$ $DV_{CC}2$		+5 V (typ.)		Digital power supply.
12	DGND3		+5 V (Typ.) (With a single power supply) GND (With dual power supplies)		Digital power supply. Ground for ECL input. +5 V for PECL and TTL input.
1	$DV_{EE}3$		GND (With a single power supply) –5 V (Typ.) (With dual power supplies)		Digital power supply. –5 V for ECL input. Ground for PECL and TTL input.
16, 17 18	N.C.				No connected pin. Not connected with the internal circuits.
13	CLK/E	I	ECL/ PECL		Clock input.
14	CLKN/E	I			CLK/E complementary input. When left open, this pin goes to the threshold potential. Only CLK/E can be used for operation, but complementary input is recommended to attain fast and stable operation.
48	RESETN/E	I			Reset input. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
47	RESET/E	I			RESETN/E complementary input. When left open, this pin goes to the threshold voltage. Only RESETN/E can be used for operation.

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
15	CLK/T	I	TTL		Clock input.
46	RESETN/T	I			Reset input. When left open, this input goes to high level. When the input is set to low level, the built-in CLK frequency divider circuit can be reset.
44	INV	I	TTL		Data output polarity inversion input. When left open, this input goes to high level. (See Table 1. I/O Correspondence Table.)
45	SELECT		VCC or GND		Data output mode selection. (See Table 2. Operating Mode Table.)

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
11	V_{RT}	I	4.0 V (typ.)		Top reference voltage. By-pass to AGND with a 1 µF tantal capacitor and a 0.1 µF chip capacitor.
9	$V_{RM}3$		$V_{RB} + \frac{3}{4}(V_{RT} - V_{RB})$		Reference voltage mid point. By-pass to AGND with a 0.1 µF chip capacitor.
7	$V_{RM}2$		$V_{RB} + \frac{2}{4}(V_{RT} - V_{RB})$		Reference voltage mid point. By-pass to AGND with a 0.1 µF chip capacitor.
4	$V_{RM}1$		$V_{RB} + \frac{1}{4}(V_{RT} - V_{RB})$		Reference voltage mid point. By-pass to AGND with a 0.1 µF chip capacitor.
2	V_{RB}	I	2.0 V (typ.)		Bottom reference voltage. By-pass to AGND with a 1 µF tantal capacitor and a 0.1 µF chip capacitor.
6	V_{IN}	I	VRT to VRB		Analog input.
33 to 40	P1D0 to P1D7	O	TTL		Port 1 side data output.
21 to 28	P2D0 to P2D7	O			Port 2 side data output.
43	CLKOUT	O			Clock output. (See Table 2. Operating Mode Table.)

Electrical Characteristics

($DV_{CC}1, 2$, AV_{CC}, DGND3 = +5 V, DGND1, 2, AGND, $DV_{EE}3$ = 0 V, V_{RT} = 4 V, V_{RB} = 2 V, Ta = 25 °C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution				8		bits
DC characteristics						
Integral linearity error	E_{IL}	V_{IN} = 2 Vp-p, Fc = 5MSPS			±0.5	LSB
Differential linearity error	E_{DL}				±0.5	LSB
Analog input						
Analog input capacitance	C_{IN}	V_{IN} = +3.0 V + 0.07 Vrms		21		pF
Analog input resistance	R_{IN}		4		50	kΩ
Analog input current	I_{IN}		0		500	µA
Reference input						
Reference resistance	Rref*3		75	115	155	Ω
Reference current	Iref*4		9.7	17.4	28	mA
Offset voltage V_{RT} side	EOT		2		15	mV
V_{RB} side	EOB		2		10	mV
Digital input (ECL, PECL)						
Digital input voltage: High	V_{IH}		DGND3 – 1.05		DGND3 – 0.5	V
: Low	V_{IL}		DGND3 – 3.2		DGND3 – 1.4	V
Threshold voltage	V_{TH}			DGND3 – 1.2		V
Digital input current: High	I_{IH}	V_{IH} = DGND3 – 0.8 V	–50		+50	µA
: Low	I_{IL}	V_{IL} = DGND3 – 1.6 V	–75		0	µA
Digital input capacitance					5	pF
Digital input (TTL)						
Digital input voltage: High	V_{IH}		2.0			V
: Low	V_{IL}				0.8	V
Threshold voltage	V_{TH}			1.5		V
Digital input current: High	I_{IH}	V_{IH} = 3.5 V	–50		0	µA
: Low	I_{IL}	V_{IL} = 0.2 V	–500		0	µA
Digital input capacitance					5	pF
Digital output (TTL)						
Digital output voltage : High	V_{OH}	I_{OH} = –2 mA	2.4			V
: Low	V_{OL}	I_{OL} = 1 mA			0.5	V
Switching characteristics						
Maximum conversion rate	Fc	DMUX mode	140			MSPS
Aperture jitter	Taj			10		ps
Sampling delay	Tds		3	4.5	6	ns
Clock high pulse width	Tpw1	CLK	3.0			ns
Clock low pulse width	Tpw0	CLK	3.0			ns
RESET Signal setup time	T_rs	RESETN – CLK	3.5			ns
RESET Signal hold time	T_rh	RESETN – CLK	0			ns
CLKOUT output delay	Td_clk	(C_L = 5 pF)	4.5	7	8	ns
Data output delay	Tdo1	DMUX mode (C_L = 5 pF)	T*5	T + 1	T + 2	ns
	Tdo2	(C_L = 5 pF)	6.5	8	10	ns
Output rise time	Tr	0.8 to 2.0 V (C_L = 5 pF)		2		ns
Output fall time	Tf	0.8 to 2.0 V (C_L = 5 pF)		2		ns

*These characteristics are for PECL input,unless otherwise specified.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics						
Input bandwidth		V_{IN} = 2 Vp-p, –3 dB	150			MHz
S/N ratio		Fc = 140MSPS, fin = 1 kHz Fs DMUX mode		46		dB
		Fc = 140MSPS, fin = 34.999 MHz Fs DMUX mode		40		dB
Error rate		Fc = 140MSPS, fin = 1 kHz Fs DMUX mode Error>16LSB			10^{-12}	TPS*6
		Fc = 140MSPS, fin = 34.999 MHz Fs DMUX mode Error>16LSB			10^{-9}	TPS
		Fc = 100MSPS, fin = 24.999 MHz Fs Straight mode Error>16LSB			10^{-9}	TPS
Power supply						
Supply current	I_{CC}		110	150	180	mA
Supply current	I_{EE}		0.4	0.6	0.8	mA
Power consumption	Pd*7		570	790	960	mW

*3 Rref: Resistance value between V_{RT} and V_{RB}

*4 $Iref = \frac{V_{RT} - V_{RB}}{Rref}$

*5 $T = \frac{1}{Fc}$

*6 TPS: Times Per Sample

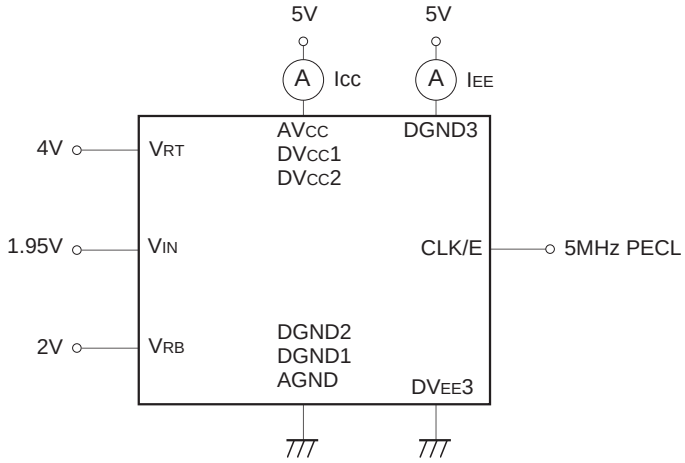
*7 $Pd = (I_{CC} + I_{EE})\ V_{CC} + \frac{(V_{RT} - V_{RB})^2}{Rref}$

V_{IN}	Step	INV															
		1								0							
		D7							D0	D7							D0
V_{RT}	255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	254	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
	⋮				⋮								⋮				
V_{RM2}	128	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	127	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	⋮				⋮								⋮				
	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
V_{RB}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

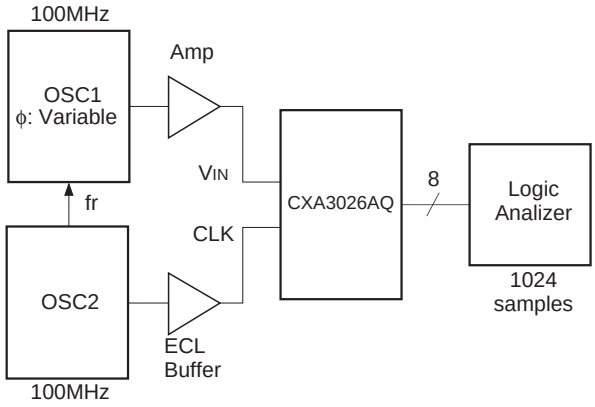
Table 1. I/O Correspondence Table

Electrical Characteristics Measurement Circuit

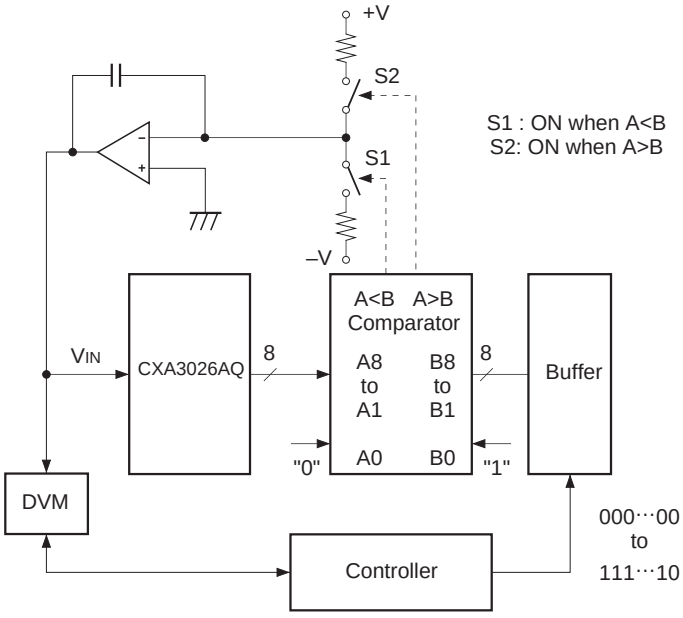
Current Consumption Measurement Circuit



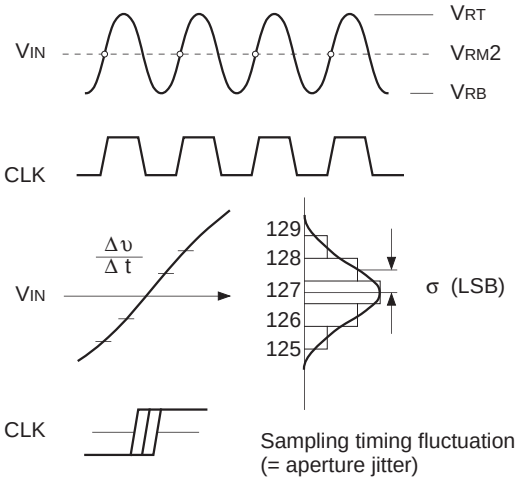
Sampling Delay Measurement Circuit
Aperture Jitter Measurement Circuit



Integral Linearity Error Measurement Circuit
Differential Linearity Error Measurement Circuit



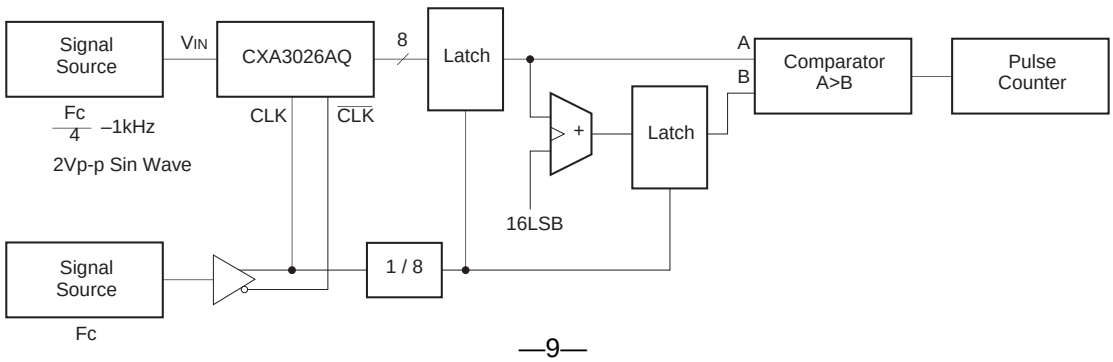
Aperture Jitter Measurement Method



Where σ(LSB) is the deviation of the output codes when the largest slew rate point is sampled at the clock which has exactly the same frequency as the analog input signal, the aperture jitter Taj is:

$$Taj = \sigma / \frac{\Delta\upsilon}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f\right)$$

Error Rate Measurement Circuit



Description of Operating Modes

The CXA3026AQ has two types of operating modes which are selected with Pin 45 (SELECT).

Operating mode	SELECT	Maximum conversion rate	Data output	Clock output
DMUX mode	V_{CC}	140MSPS	Demultiplexed output 70 Mbps	The input clock is 1/2 frequency divided and output. 70 MHz
Straight mode	GND	100MSPS	Straight output 100 Mbps	The input clock is inverted and output. 100 MHz

Table 2. Operating Mode Table

1. DMUX mode (See Application Circuit 1– (1), (2) and (3).)

Set the SELECT pin to V_{CC} for this mode. In this mode, the clock frequency is divided by 2 in the IC, and the data is output after being demultiplexed by this 1/2 frequency divided clock. The 1/2 frequency divided clock, which has adequate setup time and hold time for the output data, is output from the CLKOUT pin.

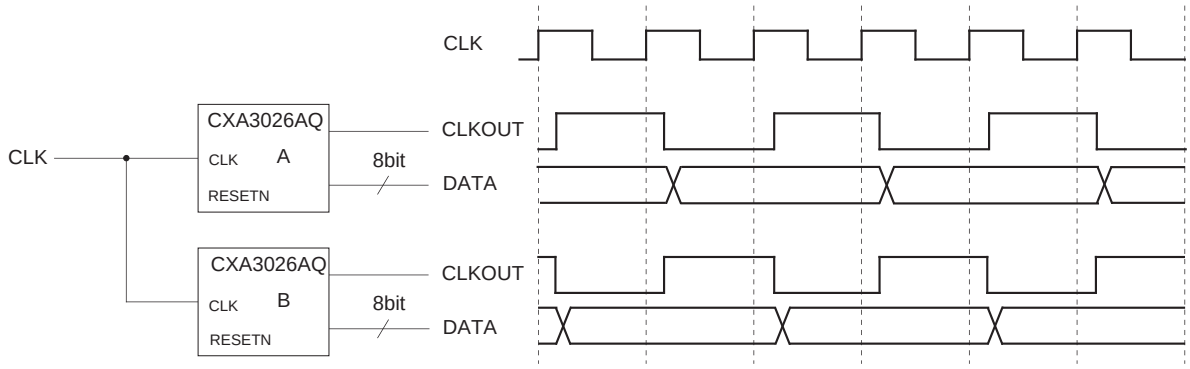
When resetting this 1/2 frequency divided clock, the low level of the RESET signal should be input to the RESETN pin (Pin 46 or 48). The RESET signal requires the setup time ($T_{rs} \geq 3.5$ ns) and hold time ($T_{rh} \geq 0$ ns) to the clock rising edge because it is synchronized with and taken in the clock. Therefore, set the RESET signal to low for T_{rs} (min.) + T_{rh} (min.) = 3.5 ns or longer to the clock rising edge.

The reset period can be extended by making the low level period of the RESET signal longer because the clock output pin is fixed to low (reset) during the low level period at the clock rising edge. If the reset start timing is regarded as not important, the timing where the RESET signal is set from high to low is not so consequence. However, when the reset is released this timing must become significant because the timing is used to commence the 1/2 frequency divided clock. In this case, the setup time (T_{rs}) is also necessary.

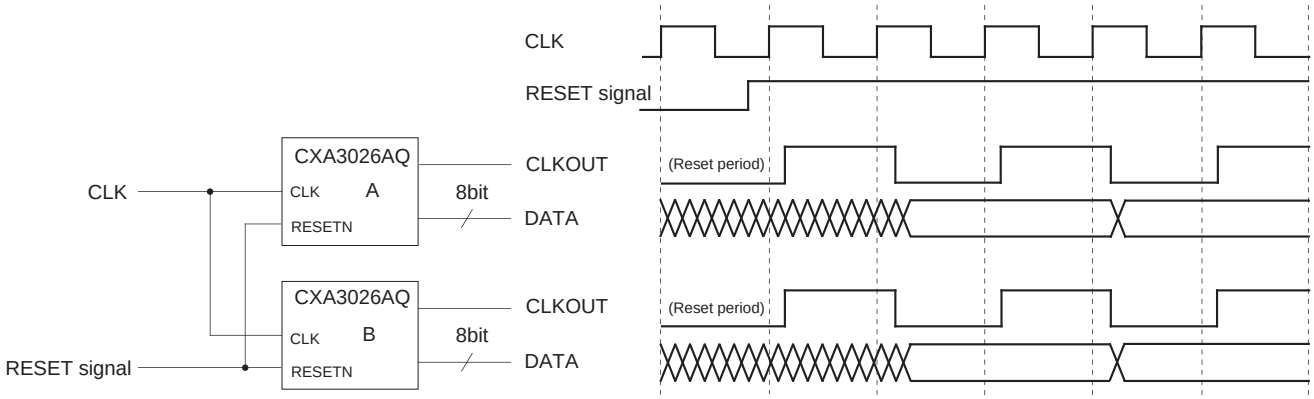
See the timing chart for detail. (This chart shows the example of reset for 2T).

The A/D converter can operate at FC (min.) = 140MSPS in this mode.

When the RESET signal is not used.



When the RESET signal is used.



2. Straight mode (See Application Circuits1- (4), (5) and (6).)

Set the SELECT pin to GND for this mode. In this mode, data output can be obtained in accordance with the clock frequency applied to the A/D converter for applications which use the clock applied to the A/D converter as the system clock.

The A/D converter can operate at Fc (min.) = 100MSPS in this mode.

Digital input level and supply voltage settings

The logic input level for the CXA3026AQ supports ECL, PECL and TTL levels.

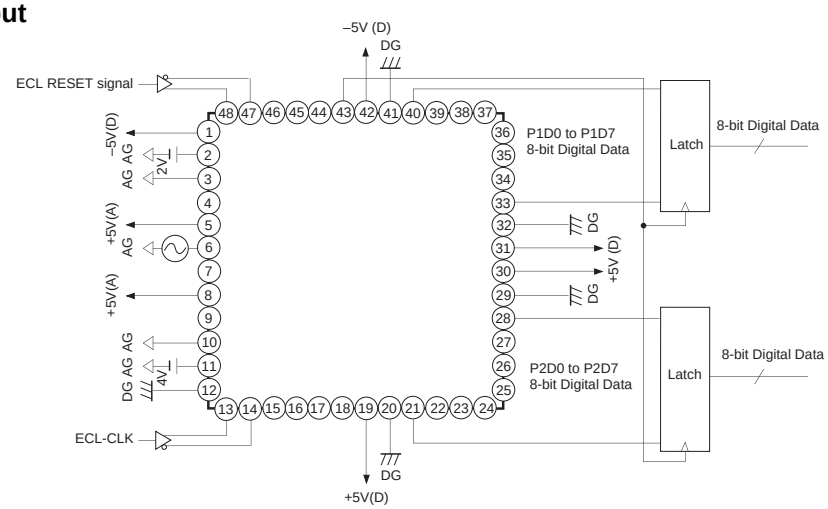
The power supplies ($DV_{EE}3$, DGND3) for the logic input block must be set to match the logic input (CLK and RESET signals) level.

Digital input level	$DV_{EE}3$	DGND3	Supply voltage	Application circuits
ECL	–5 V	0 V	±5 V	(1) (4)
PECL	0 V	+5 V	+5 V	(2) (5)
TTL	0 V	+5 V	+5 V	(3) (6)

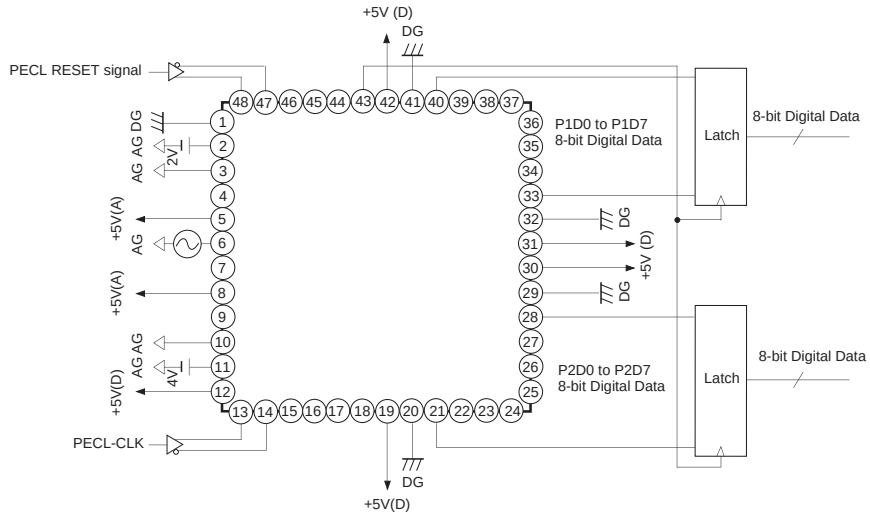
Table 3. Logic Input Level and Power Supply Settings

Application Circuit 1

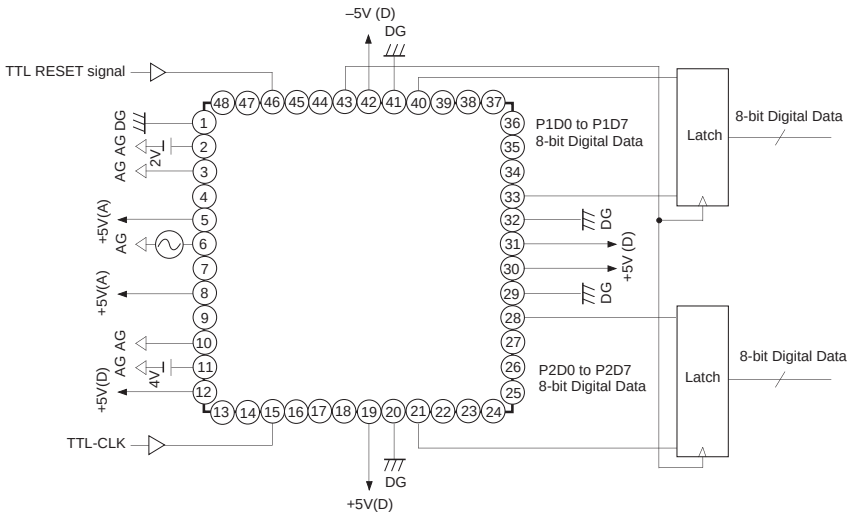
(1) DMUX ECL input



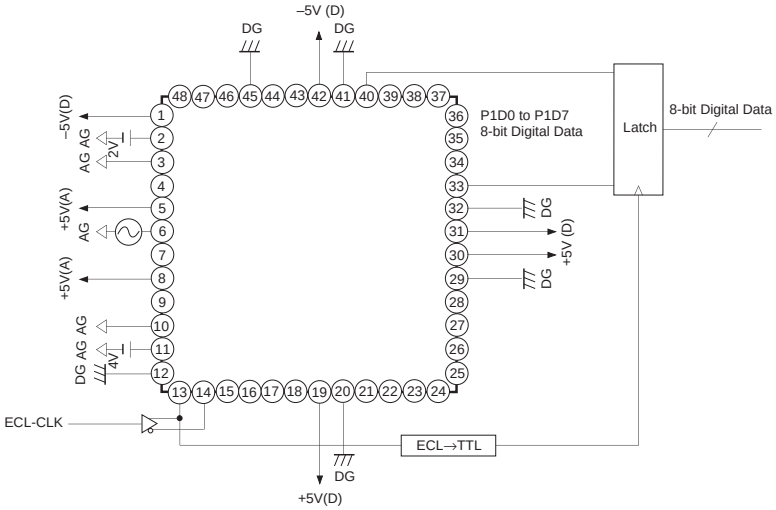
(2) DMUX PECL input



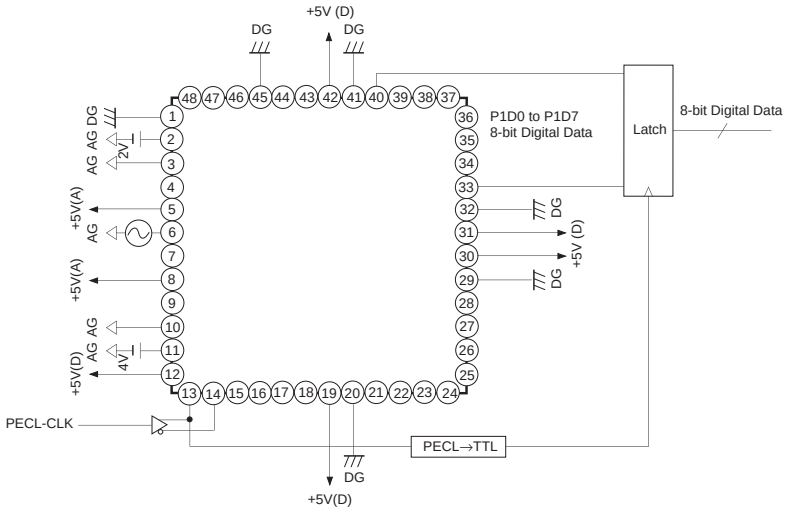
(3) DMUX TTL input



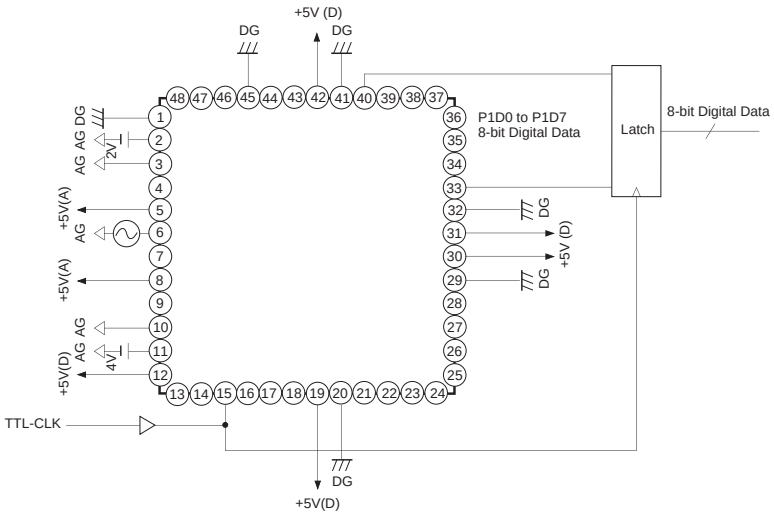
(4) Straight ECL input



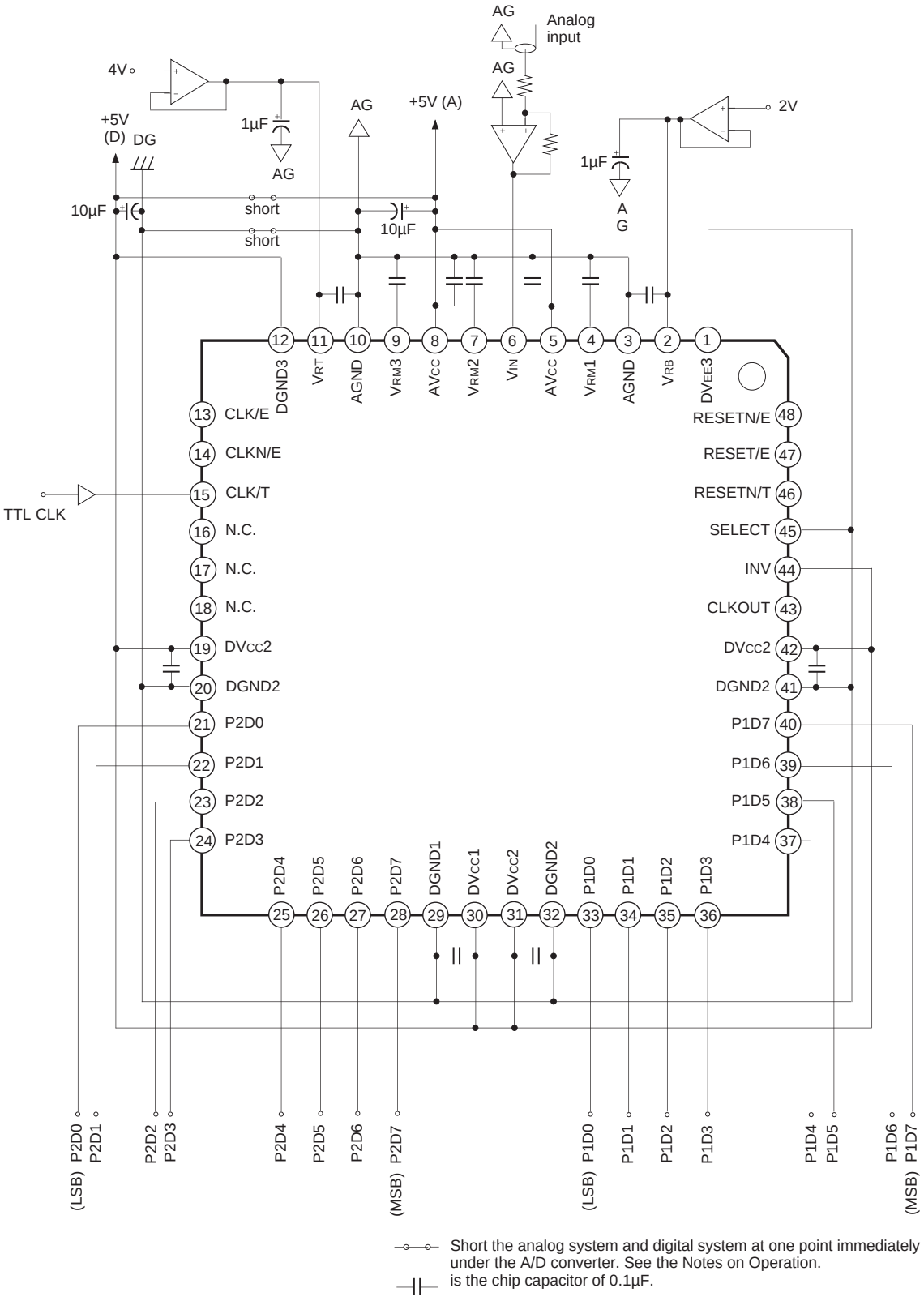
(5) Straight PECL input



(6) Straight TTL input

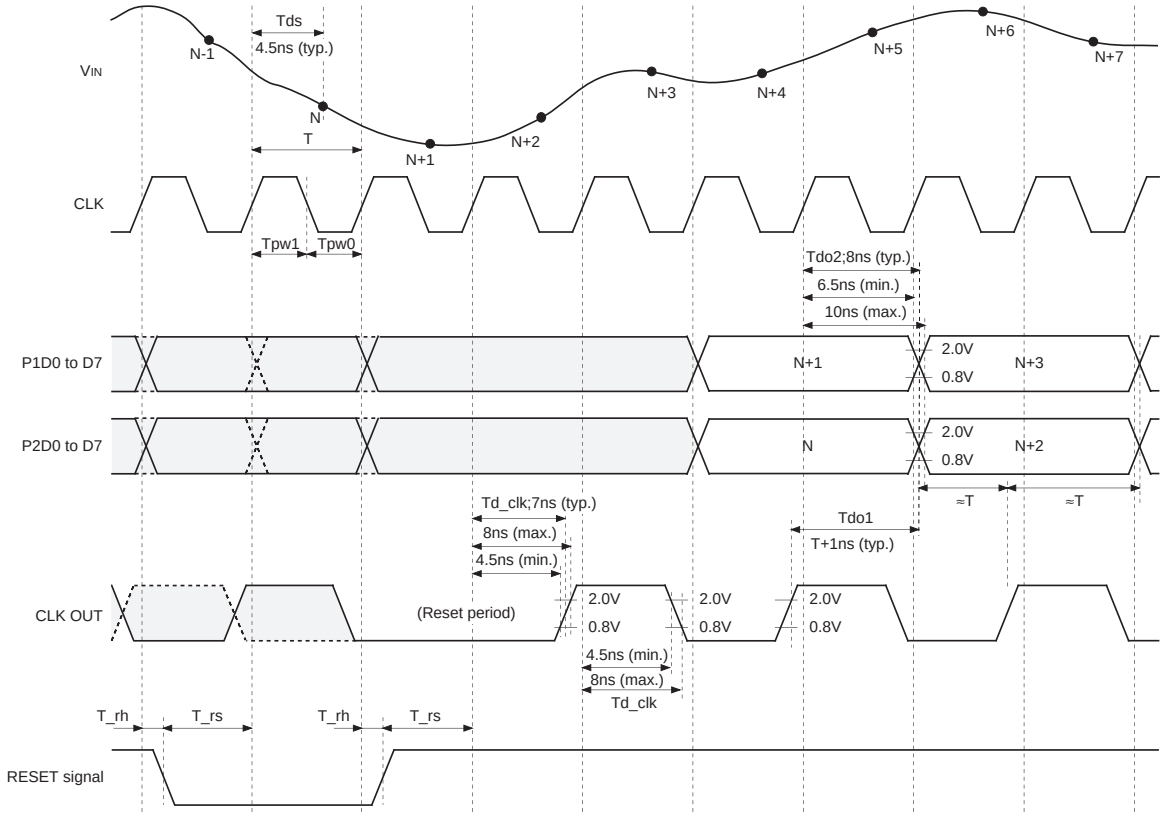


Application Circuit 2 Straight Mode TTL I/O (When a single power supply is used)

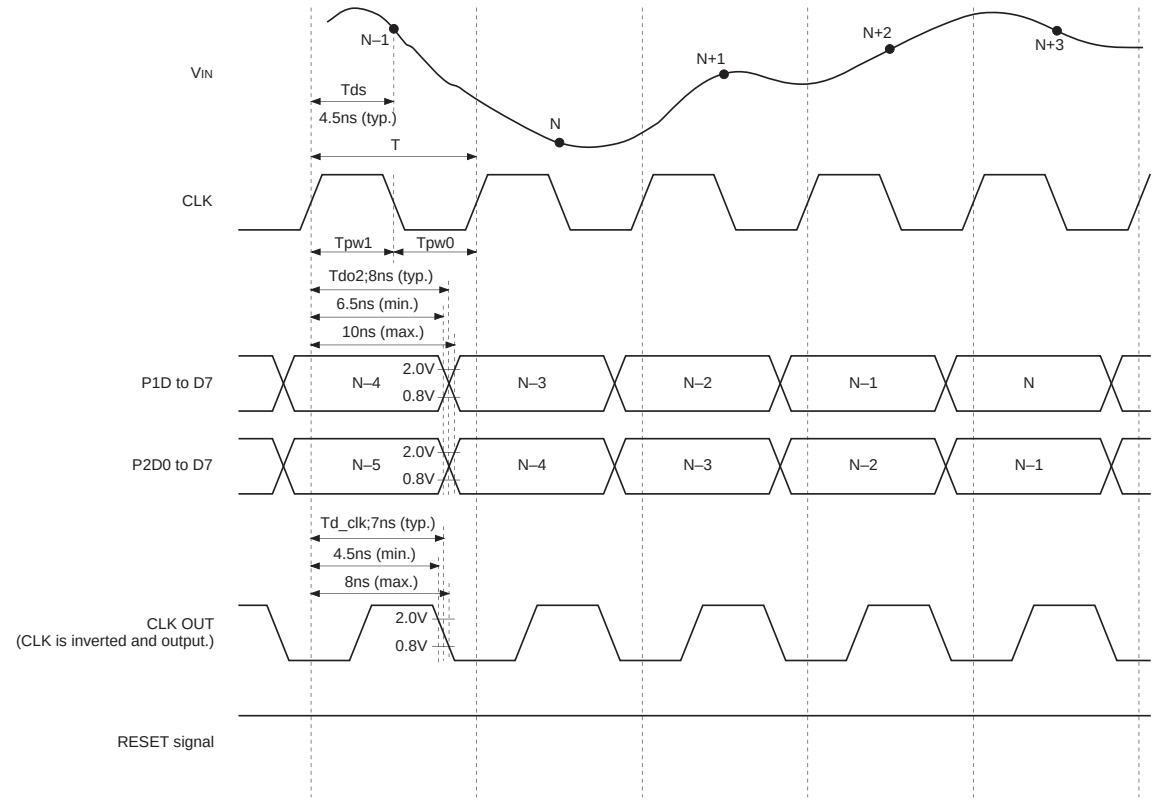


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

DMUX Mode Timing Chart (Select = V_{CC})



Straight Mode Timing Chart (Select = GND)



A/D Converter and Peripheral Circuit Timing

In the maximum clock rate of the DEMUX Mode, the timing of 3 channels of ADC CLKOUT in same phase is described in detail as below.

For example, the CLK OUT from one of the ADC is used as the data latch clock. The clock delay and data delay are showed in the following specification, i,e.

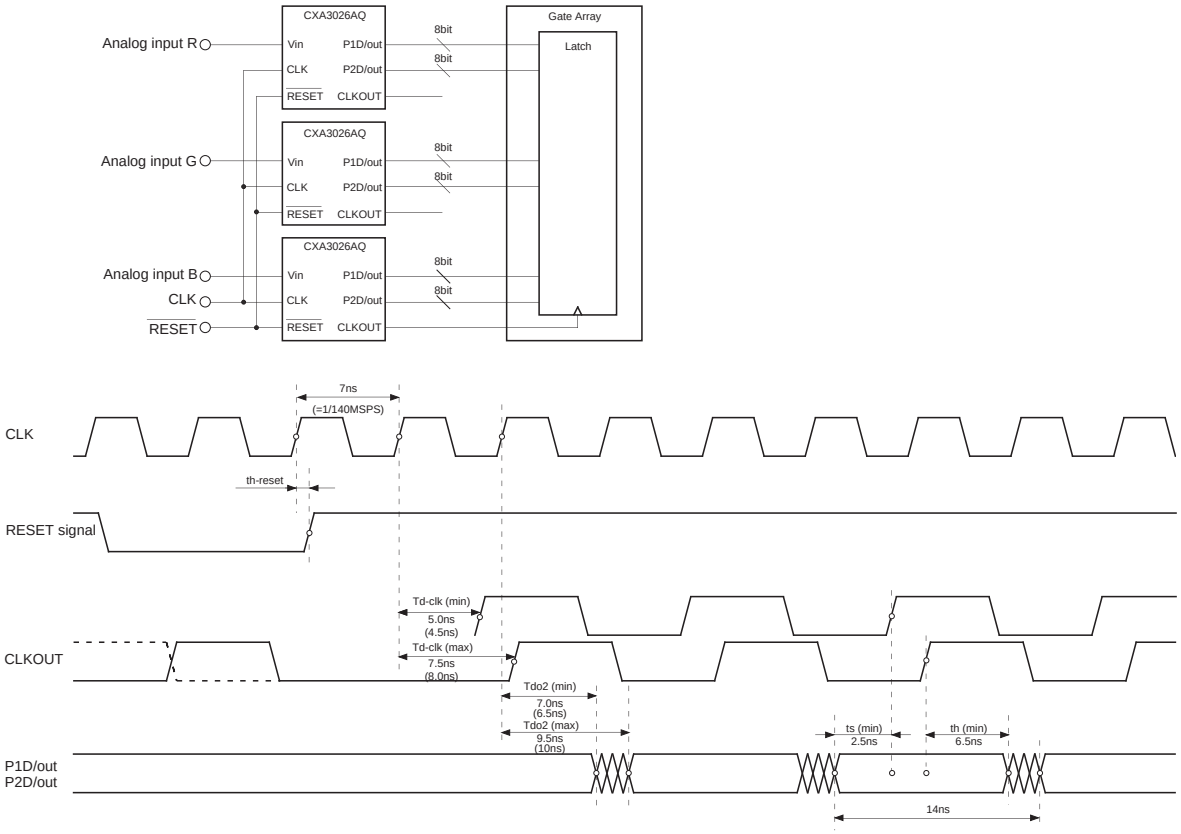
Td_clk 4.5 nS (min.) --- 8.0 nS (max.)
Tdo2 6.5 nS (min.) --- 10 nS (max.)

These values are considered in all the temperature change and power supply variation. When the maximum clock rate 140MSPS is used, the set-up time (ts) is seemed to be very small from above specifications. But the 3 channels of ADC are in the same circuit board, so that the DATA OUT delay and CLK OUT delay will be changed in same trend at the same condition of the temperature change and power supply variation. As a result, 0.5 ns of the delay will be faster, when the highest temperature and highest power supply is used. Also, 0.5 ns of the delay will be later, when the lowest temperature and lowest power supply is used. These delay can be omitted in this case.

When Ta=25 °C, V_{CC}=+5 V, the clock delay and data delay are

Td_clk 5.0 nS (min.) --- 7.5 nS (max.)
Tdo2 7.0 nS (min.) --- 9.5 nS (max.)

The timing of the DATA OUT and CLK OUT with above delay variation is showed in below. Consequently, the set-up time for the data latching can be obtained as ts (min.)=2.5 nS. The output delay change of the DATA OUT and CLK OUT due to the temperature change and the power supply variation should have the same trend of the delay change, the minimum ts=2.5 ns can be guaranteed at any temperature change and power supply variation.

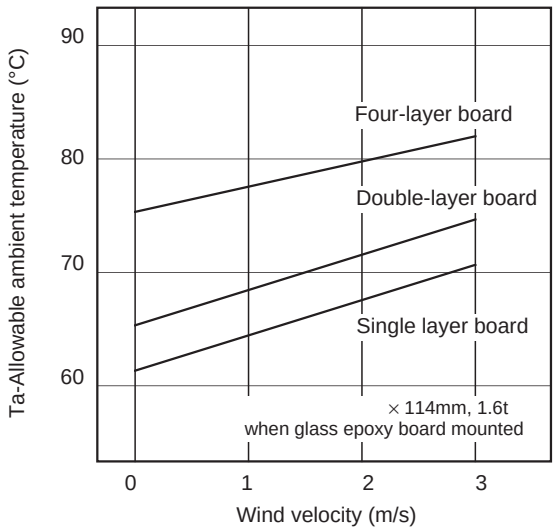


Remark : In the timing chart, the values in the brackets ( ) are included all the temperature change and the power supply variation.

Notes on Operation

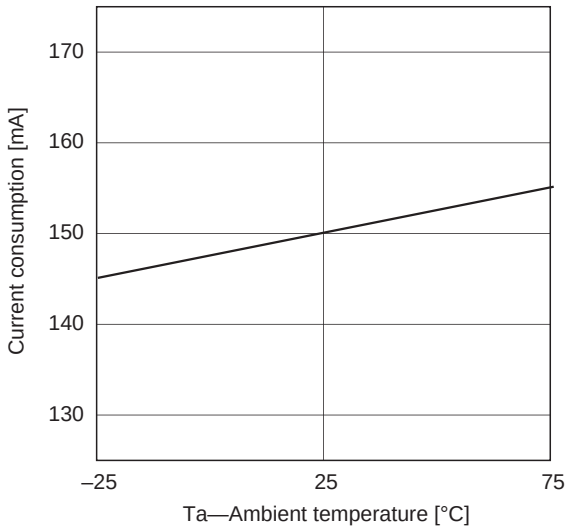
- The CXA3026AQ is a high-speed A/D converter which is capable of TTL, ECL and PECL level clock input. Characteristic impedance should be properly matched to ensure optimum performance during high-speed operation.
- The power supply and grounding have a profound influence on converter performance. The power supply and grounding method are particularly important during high-speed operation. General points for caution are as follows.
  - — The ground pattern should be as large as possible. It is recommended to make the power supply and ground patterns wider at an inner layer using a multi-layer board.
  - — To prevent interference between AGND and DGND and between AV_{CC} and DV_{CC}, make sure the respective patterns are separated. To prevent a DC offset in the power supply pattern, connect the AV_{CC} and DV_{CC} lines at one point each via a ferrite-bead filter Shorting the AGND and DGND patterns in one place immediately under the A/D converter improves A/D converter performance.
  - — Ground the power supply pins (AV_{CC}, $DV_{CC}1$, $DV_{CC}2$, $DV_{EE}3$) as close to each pin as possible with a 0.1 µF or larger ceramic chip capacitor.
    (Connect the AVcc pin to the AGND pattern and the $DV_{CC}1$, $DV_{CC}2$ and $DV_{EE}3$ pins to the DGND pattern.)
  - — The digital output wiring should be as short as possible. If the digital output wiring is long, the wiring capacitance will increase, deteriorating the output slew rate and resulting in reflection to the output waveform since the original output slew rate is quite fast.
- The analog input pin V_{IN} has an input capacitance of approximately 21 pF. To drive the A/D converter with proper frequency response, it is necessary to prevent performance deterioration due to parasitic capacitance or parasitic inductance by using a large capacity drive circuit. keeping wiring as short as possible, and using chip parts for resistors and capacitors, etc.
- The V_{RT} and V_{RB} pins must have adequate by-pass to protect them from high-frequency noise. By-pass them to AGND with approximately 1 µF tantal capacitor and, 0.1 µF chip capacitor as short as possible.
- If the CLK/E pin is not used, by-pass this pin to DGND with an approximately 0.1 µF capacitor. At this time, approximately DGND3 – 1.2 V voltage is generated. However, this is not recommended for use as threshold voltage V_{BB} as it is too weak.
- When the digital input level is ECL or PECL level, ∗∗∗/E pins should be used and ∗∗∗/T pins left open. When the digital input level is TTL, ∗∗∗/T pins should be used and ∗∗∗/E pins left open.
- The CXA3026AQ uses the package with low thermal resistance, but the resistance varies according to the board used. Therefore, cool the package by air cooling and others referring to the right graph.

Allowable ambient temperature vs. Wind velocity

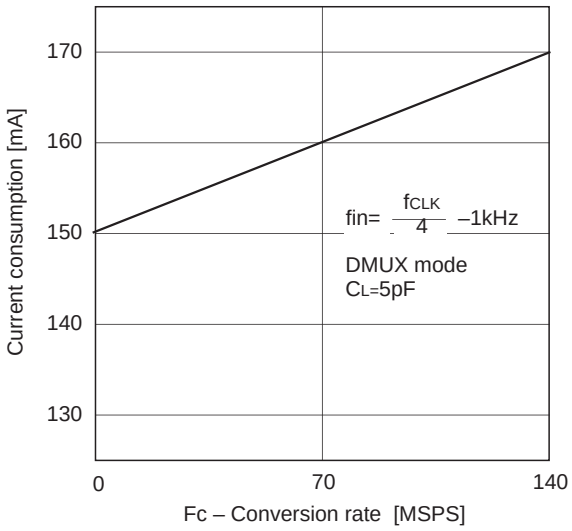


Example of Representative Characteristics

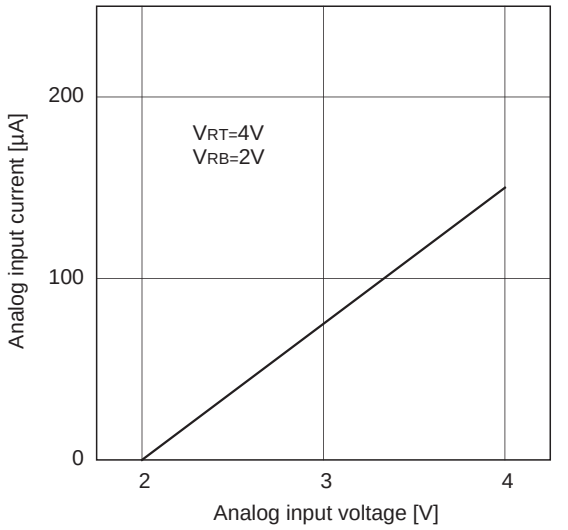
Current consumption vs. Ambient temperature characteristics



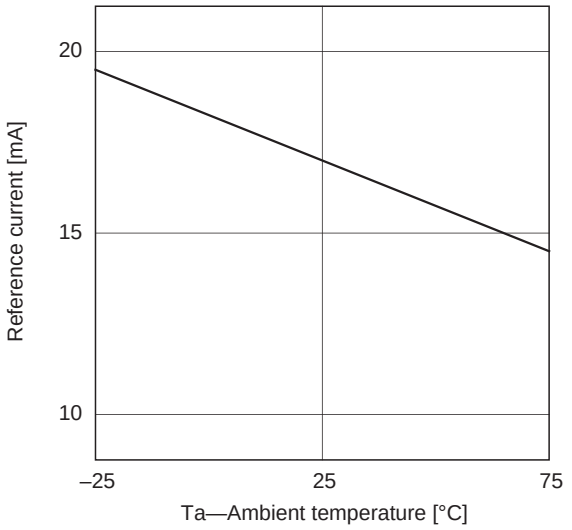
Current consumption vs. Conversion rate characteristics response



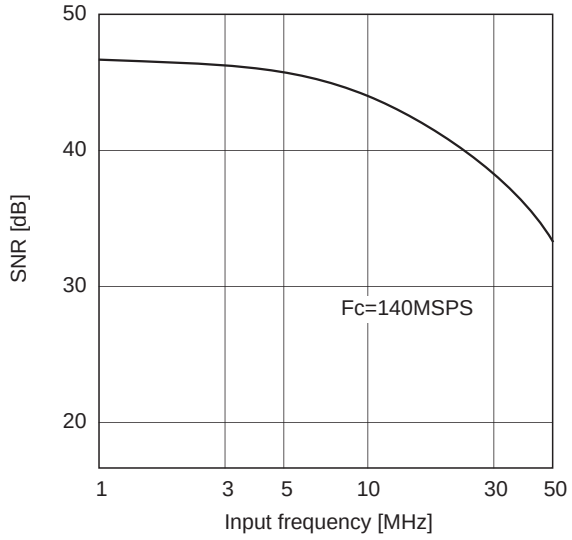
Analog input current vs. Analog input voltage characteristics



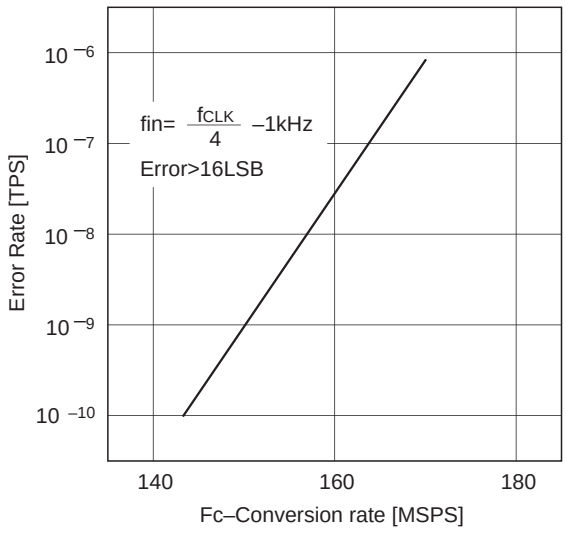
Reference current vs. Ambient temperature characteristics



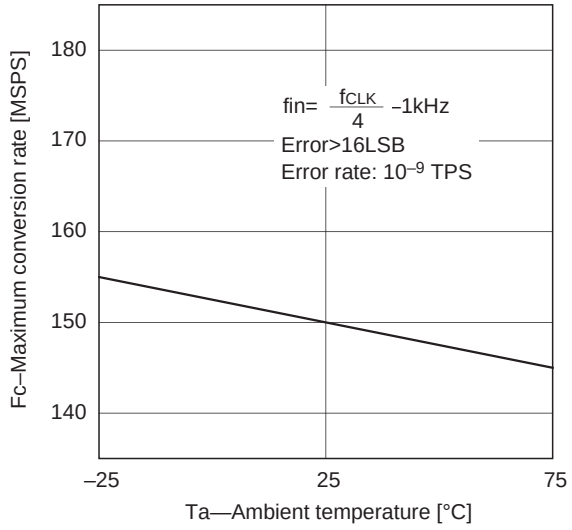
SNR vs. Input frequency response



Error rate vs. Conversion rate characteristics



Maximum conversion rate vs. Ambient temperature characteristics



CXA3026AQ Evaluation Board

Description

The CXA3026AQ Evaluation Board is a special board designed to maximize and facilitate the evaluation performance of the CXA3026AQ. After latching the CXA3026AQ output data with a frequency divided clock, the analog signal can be regenerated by a 10-bit high-speed D/A converter. The latched data can also be extracted externally via a 24-pin cable connector.

Features

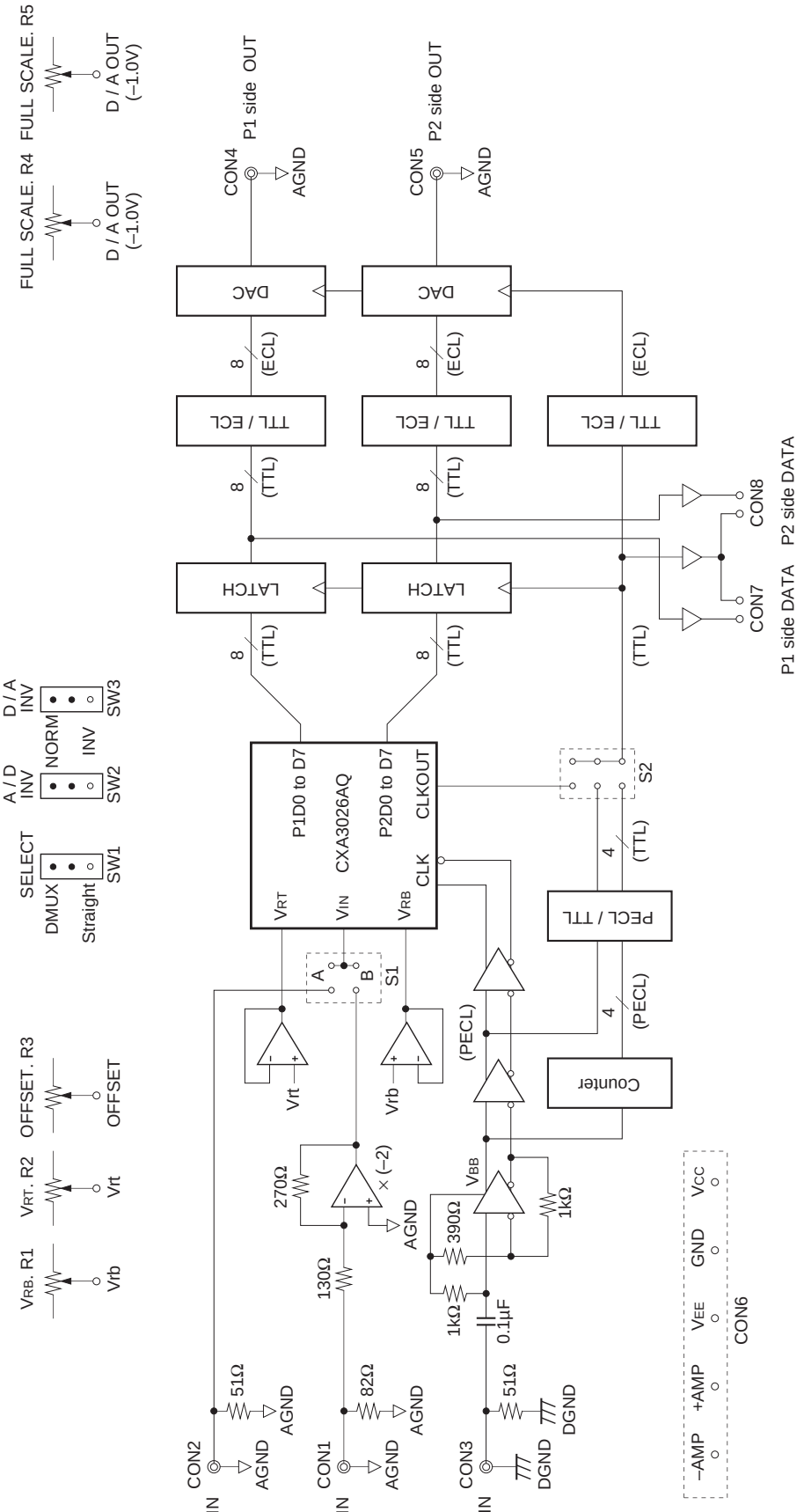
- Resolution: 8 bits
- Maximum conversion rate: 140MSPS (min.)
- Supply voltage: ±5.0 V
- Dual analog input pins: DIR.IN: AC coupling input pin
  AMP.IN: Operational amplifier input pin
- Clock frequency division: 1/1 to 1/16

Absolute Maximum Ratings

• Supply voltage	V_{CC}	–0.5 to +7.0	V
	V_{EE}	–7.0 to +0.5	V
	+AMP	–0.5 to +7.0	V
	–AMP	–7.0 to +0.5	V

Recommended Operating Conditions		Min.	Typ.	Max.	
• Supply voltage	V_{CC}	+4.75	+5.0	+5.25	V
	GND		0		V
	V_{EE}	–5.50	–5.0	–4.75	V
	+AMP	+3	+5	+7	V
	–AMP	–7	–5	–3	V
	| (+AMP) – (–AMP) |	9	10	11	V
• Analog input	AMP. IN	–0.75	0	+1.05	V
	DIR. IN	1.5	2.0	2.2	Vp-p
• Clock input	CLK. IN	0.8	1.0	1.2	Vp-p

Block Diagram



Pin Description and I/O Level

Pin No.	Symbol	I/O	Standard I/O level	Current	Description
CON1	AMP. IN	I	0.95 Vp-p		Doubles the analog input signal amplitude using the operational amplifier. The input impedance is 50 Ω.
CON2	DIR. IN	I	2.0 Vp-p		AC coupling input. Suitable for sine waves and other repeating waveforms. The input impedance is 50 Ω.
CON3	CLK. IN	I	1.0 Vp-p		The CXA3026AQ operates at the PECL level clock using the sine wave-to-PECL conversion circuit. The input impedance is 50 Ω.
CON4	P1 side OUT	O	0 to –1 V		Allows the D/A converted waveform of the CXA3026AQ port 1 side data to be observed. The output impedance is 50 Ω.
CON5	P2 side OUT	O	0 to –1 V		Allows the D/A converted waveform of the CXA3026AQ port 2 side data to be observed. The output impedance is 50 Ω.
CON6	V_{CC}	I	+5.0 V	0.8A	The inside of the board is divided into analog and digital systems.
	GND	I	0 V		
	V_{EE}	I	–5.0 V	–0.6A	
	+AMP	I	+5.0 V	40 mA	+ side power supply for the operation amplifier.
	–AMP	I	–5.0 V	–40 mA	– side power supply for the operation amplifier.
CON7	P1 side DATA	O	TTL		The CXA3026AQ port 1 side data output is latched at the frequency divided clock and then output.
CON8	P2 side DATA	O	TTL		The CXA3026AQ port 2 side data output is latched at the frequency divided clock and then output.

Board Adjustments and Settings

1. V_{RB}.R1: CXA3026AQ V_{RB} voltage adjusting volume.
2. V_{RT}.R2: CXA3026AQ V_{RT} voltage adjusting volume.
3. OFFSET.R3: Adjusting volume for matching the AMP.IN input and DIR.IN input signal ranges to the CXA3026AQ input range.
4. FULL SCALE.R4: Full-scale adjusting volume for the port 1 D/A output. (–1 V: Typ.)
5. FULL SCALE.R5: Full-scale adjusting volume for the port 2 D/A output. (–1 V: Typ.)
6. S1: Switching junction for the dual analog input pins.
   Set as follows according to the input pins used.

Symbol \ Junction	A	B
AMP.IN	OPEN	SHORT
DIR.IN	0.1 µF	10 kΩ

7. S2: Setting junction for the clock frequency division ratio. The operating speed after latching is determined by the frequency division ratio set here.
   When set to CLK OUT, it operates according to the CXA3026AQ clock output.
8. SW1 SELECT: CXA3026AQ output mode selector switch.
9. SW2 A/D INV: CXA3026AQ output polarity inversion switch.
10. SW3 D/A INV: D/A converter output polarity inversion switch.

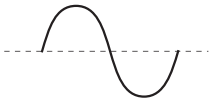
Notes on Board Operation

1. The factory settings for the CXA3026AQ Evaluation Board are as follows.

V_{RB}.R1 = 1.5 V V_{RT}.R2 = 3.0 V OFFSET.R3 = 2.25 V	FULL SCALE.R4 = –1 V FULL SCALE.R5 = –1 V	S1 A ··· OPEN, B···SHORT S2 8 ··· SHORT (1/8 frequency division)

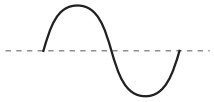
When using the board in this condition, the input signals should be input at the amplitudes shown below. (The frequency is set as desired.)

Analog input signal: CON1 (AMP.IN)



0V center, 800mVp-p or less

Clock input signal: CON3 (CLK.IN)



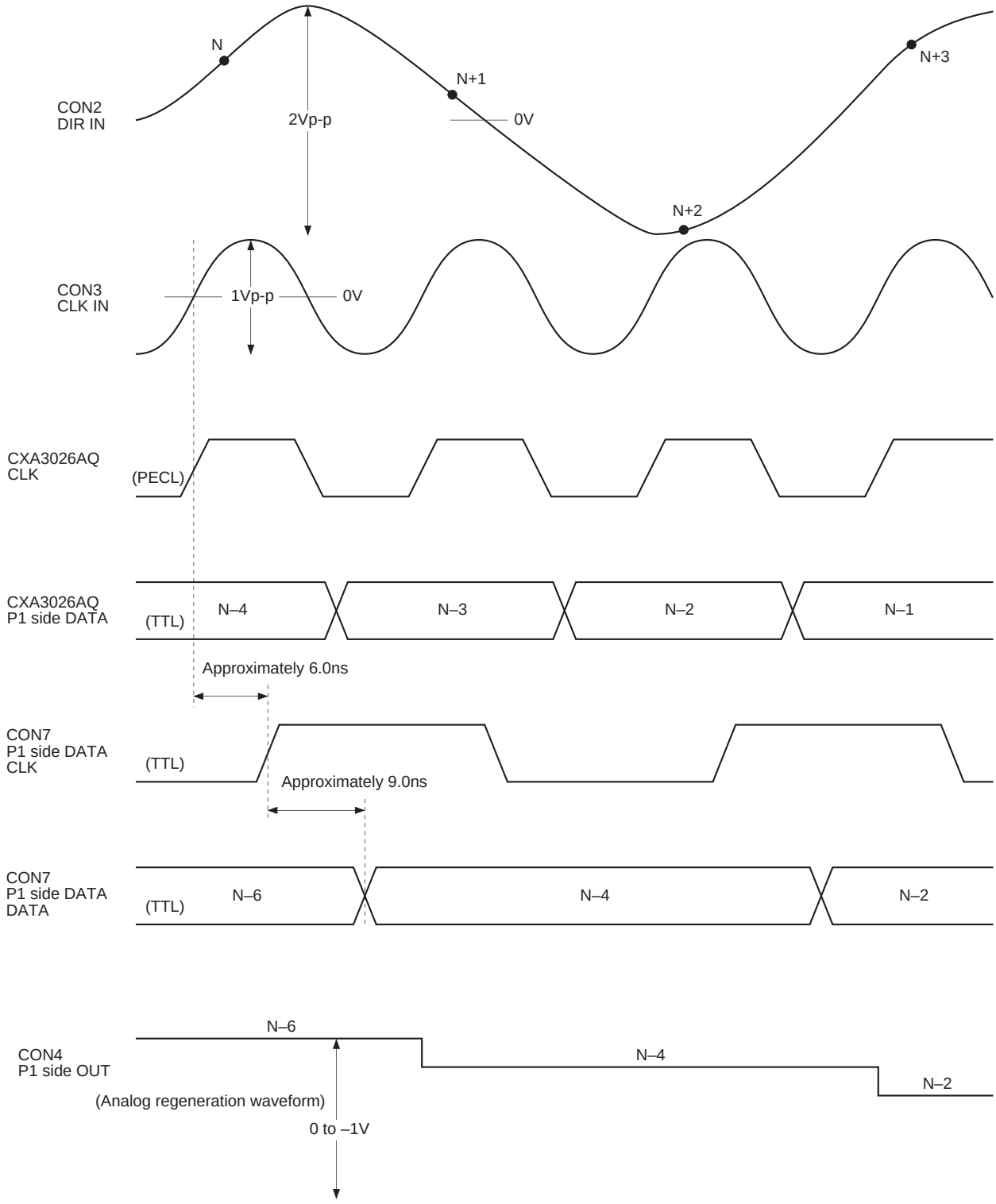
0V center, 1.0Vp-p

2. When the analog signal is input from the CON1 (AMP.IN) pin, IC2:CLC404 limits the input dynamic range of the A/D converter's analog input signal according to the +AMP and –AMP supply voltages. The power supply for the operational amplifier can also be shifted to +AMP = +7.0 V and –AMP = –3.0 V to allow use with a wider input dynamic range.

3. When the analog input signal is a sine wave or other repeating waveform, the signal can be input from the CON2 (DIR.IN) pin with AC coupling. In these cases, the input dynamic range is not limited by the +AMP and –AMP supply voltages, but the V_{RT} level may be limited by IC3:NJM3403A. Therefore, the power supply for the operational amplifier should be shifted in the same manner as in 2. above.

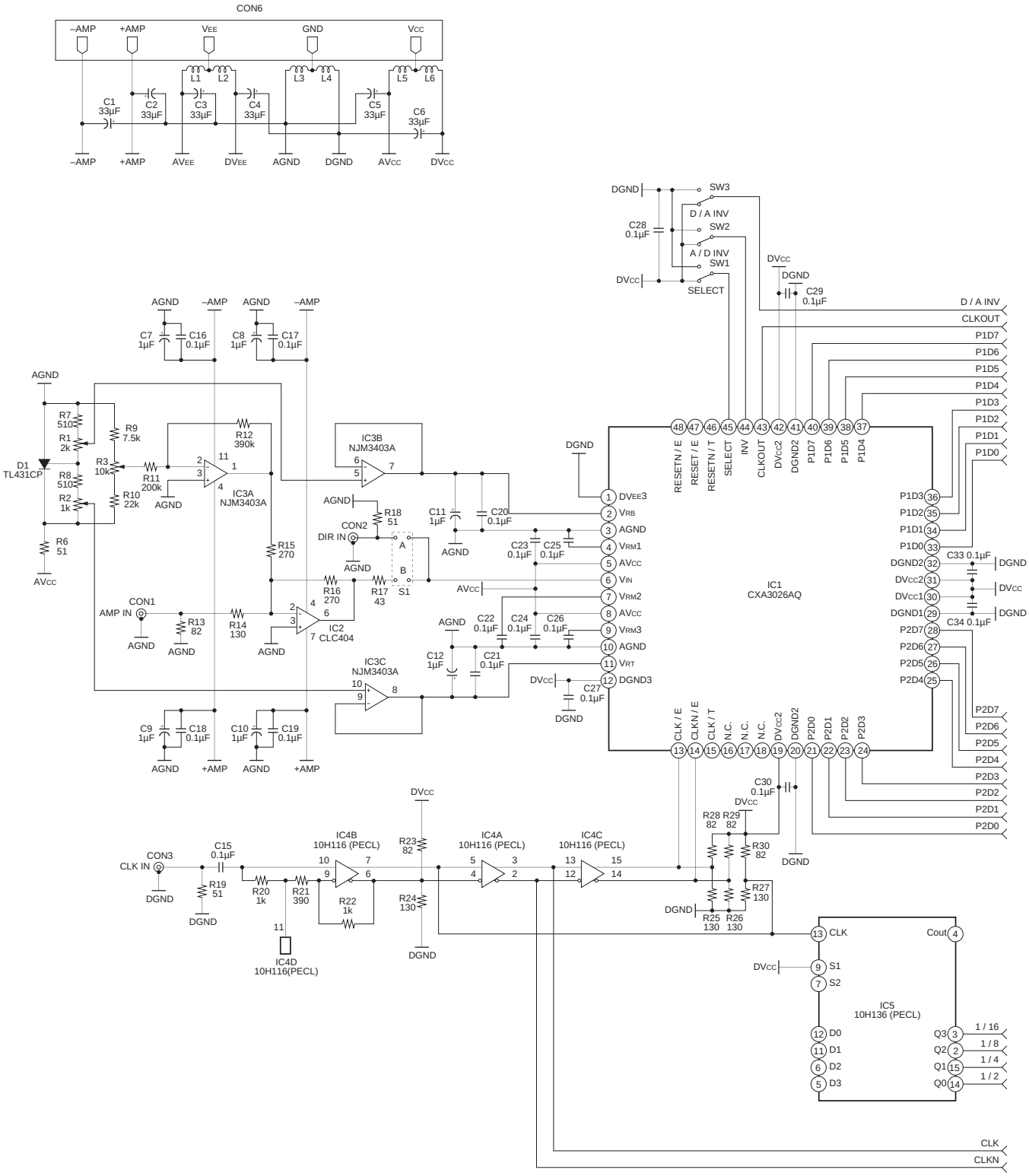
4. In the evaluation board of the CXA3026AQ,CLC404 (Comlinear) is employed for IC2 to drive the analog input signal. Though,CLC505 (Comlinear) can also be used instead of CLC404, there should be a little change in the peripheral circuit in this case.

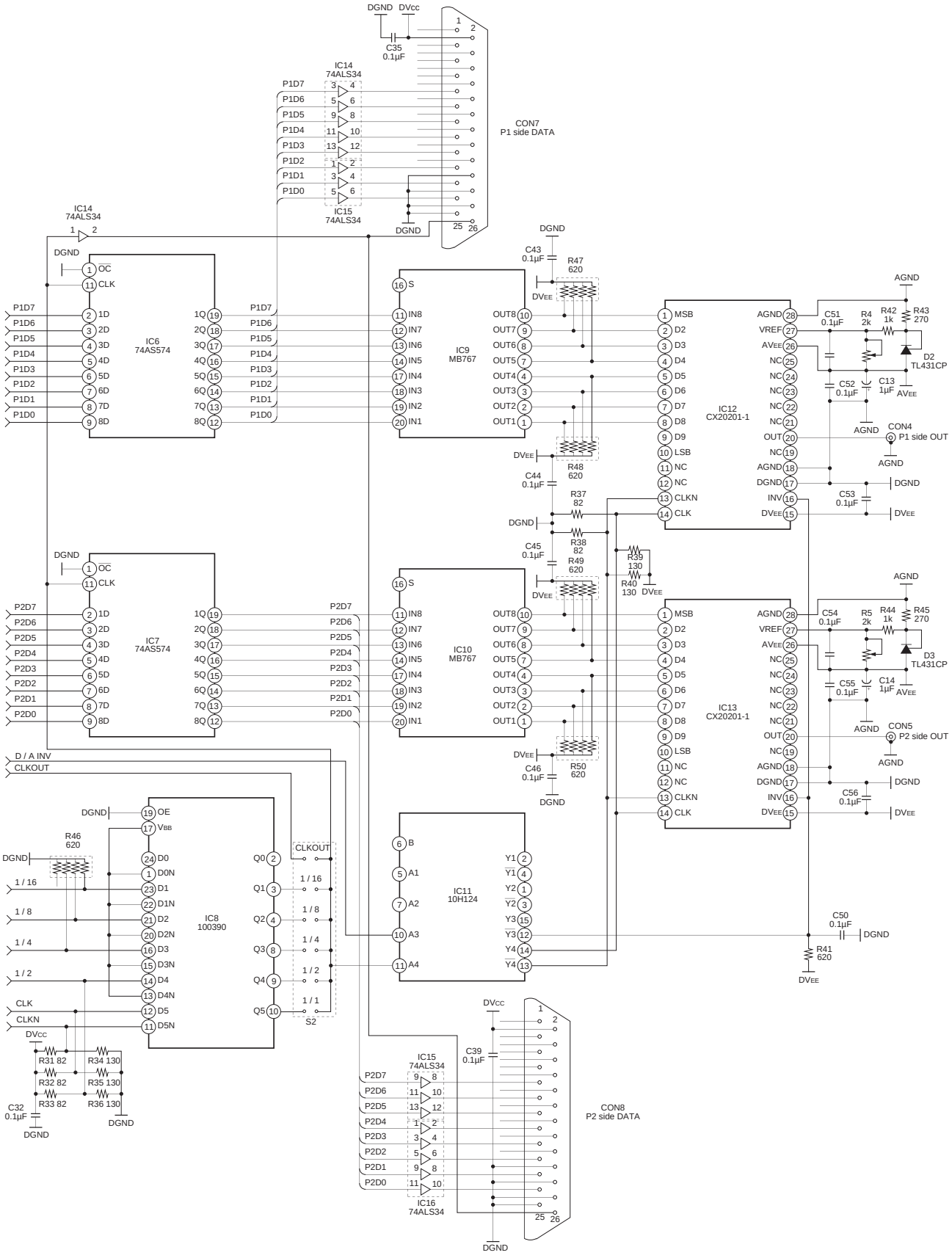
CXA3026AQ Evaluation Board Timing Chart



Operating Conditions
- CXA3026AQ operating mode : Straight mode
- Anaiong : DIR IN pin input
- S2 setting : 1/2 frequency divided clock

Circuit Diagram



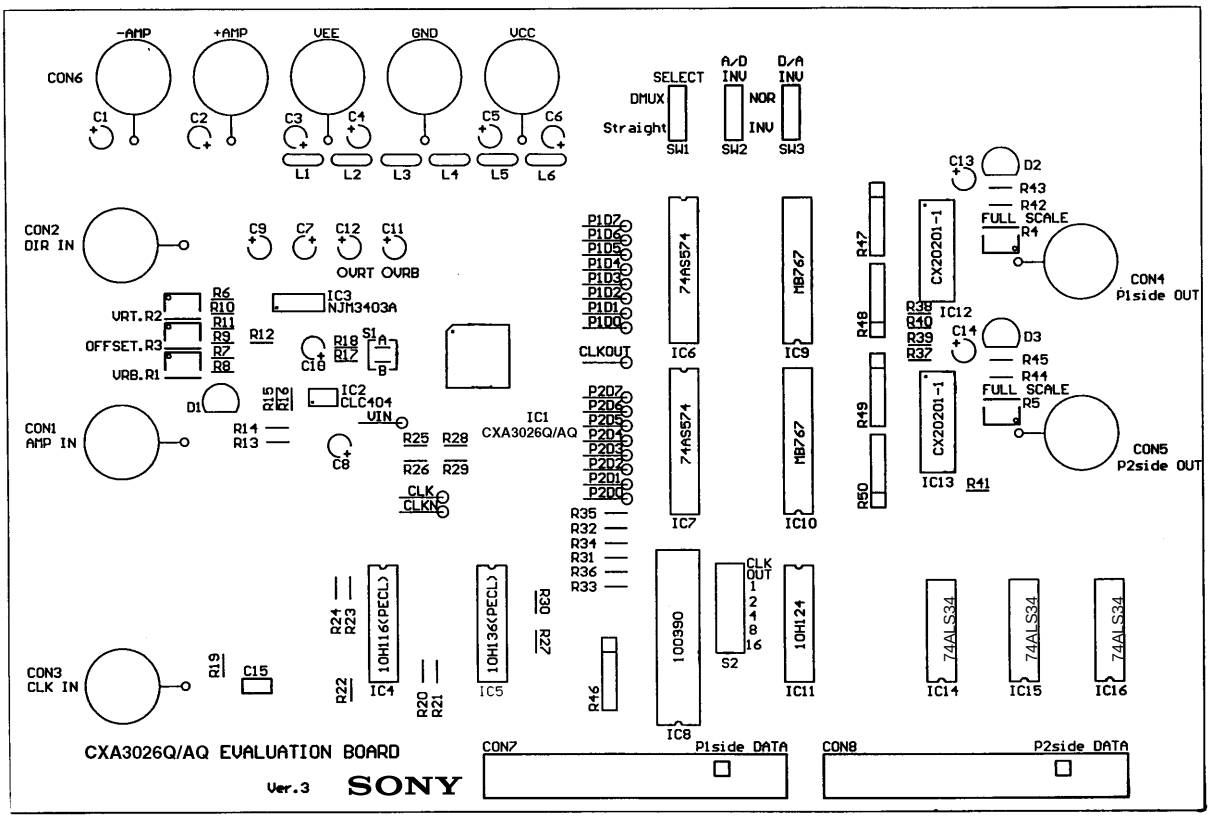

DGND DVcc
C35 0.1µF
IC14 74ALS34
IC15 74ALS34
CON7 P1 side DATA
P1D7 P1D6 P1D5 P1D4 P1D3 P1D2 P1D1 P1D0
IC6 74AS574
IC9 MB767
IC12 CX20201-1
IC7 74AS574
IC10 MB767
IC13 CX20201-1
IC11 10H124
IC8 100390
IC16 74ALS34
CON8 P2 side DATA
CON4 P1 side OUT
CON5 P2 side OUT
D2 TL431CP
D3 TL431CP
AGND
DGND
DVEE
AVEE
D / A INV
CLKOUT
CLK
CLKN
S2
R31 82
R32 82
R33 82
R34 130
R35 130
R36 130
C32 0.1µF
C39 0.1µF
C50 0.1µF
R41 620
R46 620
R47 620
R48 620
R49 620
R50 620
R37 82
R38 82
R39 130
R40 130
R42 1k
R43 270
R44 1k
R45 270
R4 2k
R5 2k
C51 0.1µF
C52 0.1µF
C53 0.1µF
C54 0.1µF
C55 0.1µF
C56 0.1µF
C13 1µF
C14 1µF
C43 0.1µF
C44 0.1µF
C45 0.1µF
C46 0.1µF

Component List

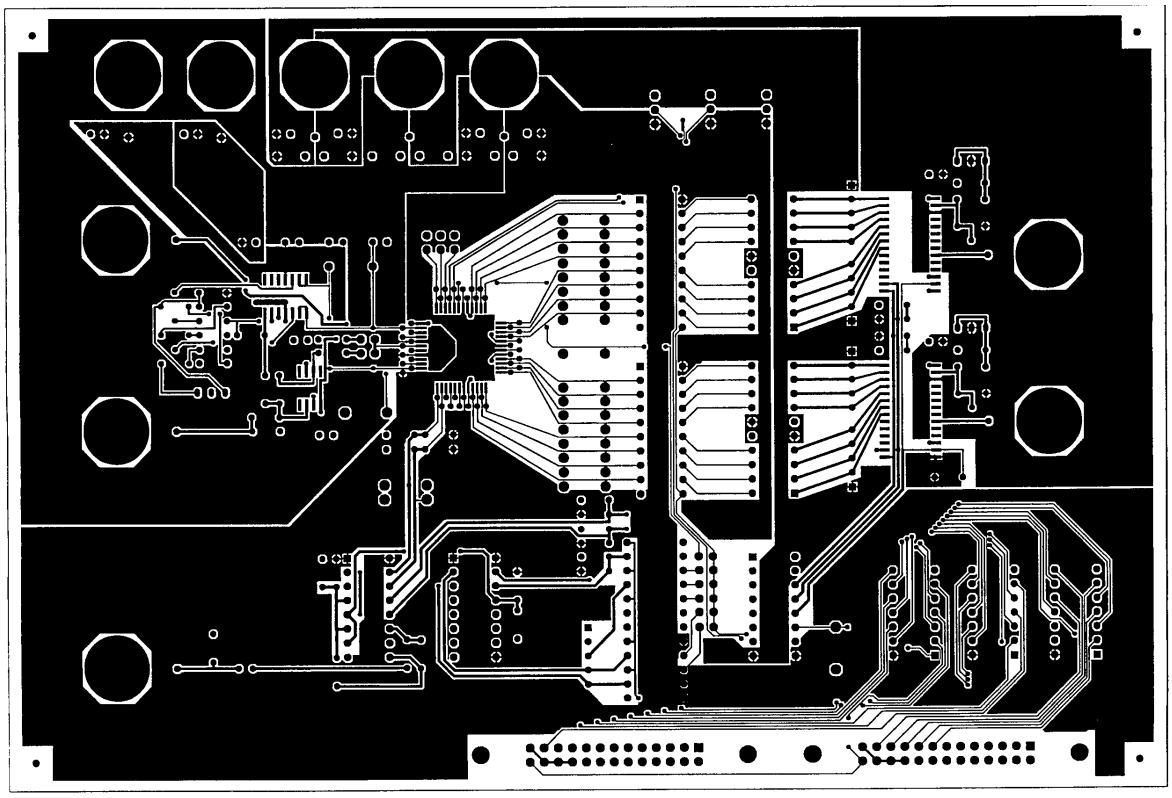
No.	Product name	Function
IC1	CXA3026AQ	8-bit A/D converter
IC2	CLC404AJE	OP-AMP
IC3	NJM3403AM	OP-AMP
IC4	MC10H116L	ECL Buffer
IC5	MC10H136L	ECL Countor
IC6, 7	74AS574N	TTL Latch
IC8	100390	PECL→TTL conversion
IC9, 10	MB767P	TTL→ECL conversion
IC11	MC10H124L	TTL→ECL conversion
IC12, 13	CXA20201A-1	10-bit D/A converter
IC14 to 16	74ALS34	TTL Buffer
D1 to 3	TL431CP	Shunt regulator
SW1 to 3	ATE1D-2F3-10	Toggle switch
S1, 2	JX-1	Short pin
CON1 to 5	01K0315	BNC connector
CON6	TJ-563	Power supply connector
CON7, 8	(FAP-2601-1202)	Flat cable connector
L1 to 6	ZBF503D-00	Ferrite-bead filter
C1 to 6	Tantal capacitor	33µF
C7 to 12	Tantal capacitor	1µF
C15	Ceramic capacitor	0.1µF
All parts other than those listed above		
	Chip capacitor	0.1µF

No.	Product name	Function
R2	RJ-5W-1K	1kΩ volume resistor
R1, 4, 5	RJ-5W-2K	2kΩ volume resistor
R3	RJ-5W-10K	10kΩ volume resistor
R46 to 50	RGLD4X621J	620Ω network resistor
R6, 18, 19	FRD-25SR (0.25W)	51Ω
R7.8	FRD-25SR (0.25W)	510Ω
R9	FRD-25SR (0.25W)	7.5kΩ
R10	FRD-25SR (0.25W)	22kΩ
R11	FRD-25SR (0.25W)	200kΩ
R12	FRD-25SR (0.25W)	390kΩ
R13, 23, 28 to 33, 37, 38	FRD-25SR (0.25W)	82Ω
R14, 24 to 27, 34 to 36, 39, 40	FRD-25SR (0.25W)	130Ω
R15, 16, 43, 45	FRD-25SR (0.25W)	270Ω
R17	FRD-25SR (0.25W)	43Ω
R20, 22, 42, 44	FRD-25SR (0.25W)	1kΩ
R21	FRD-25SR (0.25W)	390Ω
R41	FRD-25SR (0.25W)	620Ω

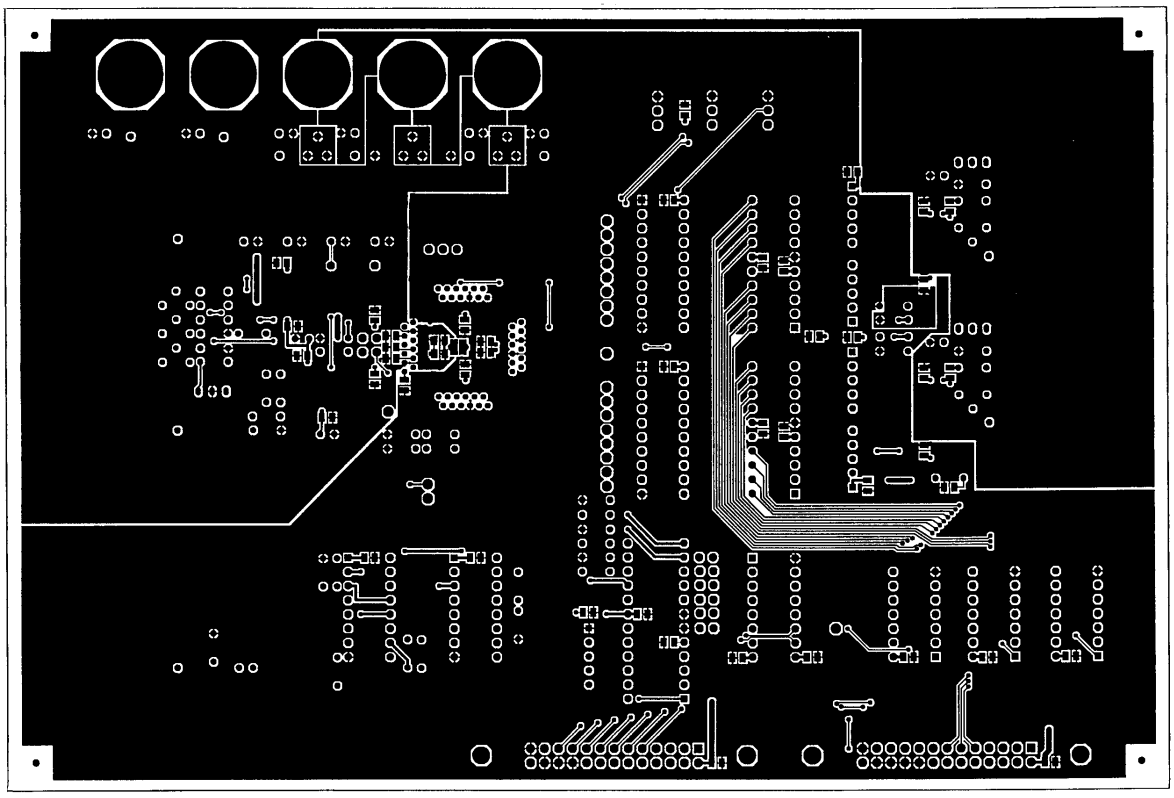
∗ CON7 and 8 are not mounted when boards are shipped. (Manufacturer: YAMAICHI Electronics Co., Ltd.)



Component side silk diagram



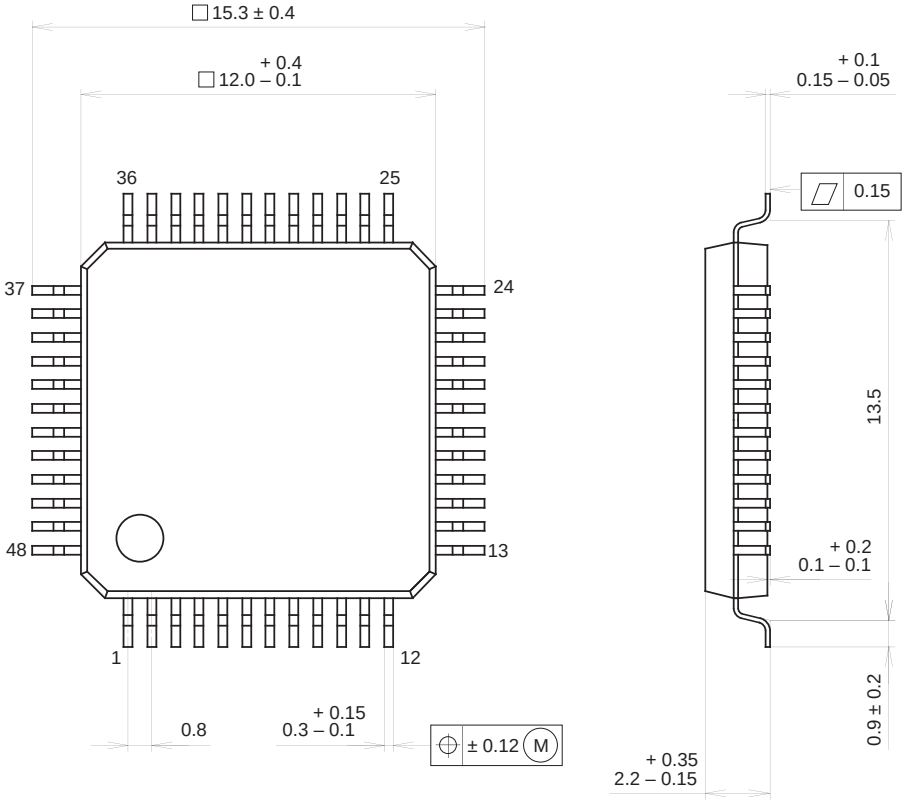
Component side pattern diagram



Solder side pattern diagram

Package Outline Unit : mm

48PIN QFP (PLASTIC)



SONY CODE	QFP-48P-L04
EIAJ CODE	∗QFP048-P-1212-B
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).