YAMAHA LSI

YGV606B

AVDP

Advanced Video Display Processor

■ OUTLINE

The AVDP is the ideal VDP (video display processor) for display screen control of consumer TVs. It has a number of high level display and drawing functions. Therefore, graphic systems for OSD, education equipment, children's toys, etc., can all be easily realized at nominal cost.

■ FEATURES

Display functions

• Display mode	Bitmap graphics and sprite
• Display resolution	NTSC : 368 × 240 (480) PAL : 368 × 280 (560) Numbers in parentheses indicate interlace alternate mode.
• Number of display colors	Built-in color pallet, 256 colors out of a selection of 260,000 colors can be displayed. This makes it possible to display natural images. Simultaneous 16 color/256 color/32768 color (when using two AVDPs) display.
• Scroll	Scrollable in all directions. An XY coordinate image space (bitmap) can be set freely in any screen structure. A scroll display area of any size can be set in the image space.
• Sprite	Two 32 × 32 dot sprites can be displayed. Color can be displayed in dot units.
• Color bus	An external superimposed display can be constructed using the output of the color bus. Multiple plane structure with multiple AVDPs is possible through the color bus input terminal.
• Others	Display window can be set and mosaic display is possible. Divided screen display is possible. Linear RGB output through the built-in DAC.

YAMAHA CORPORATION

YGV606 CATALOG
CATALOG No.: LSI-4GV606B2
1995. 12

Drawing functions

- Command types: Block transfer (Rectangle area, point)
  Linear drawing
  Border color detection
- Drawing attributes: Logical operation (NOT, AND, OR, EOR, etc.)
  Transparent color process
  Bit write mask
  Drawing area clipping
- Drawing speed: A maximum of 560 nsec/dot

Others

- VRAM: Uses 1M and 4M DRAMs, only one is required for an active VRAM construction.

  16-color, 1-screen mode

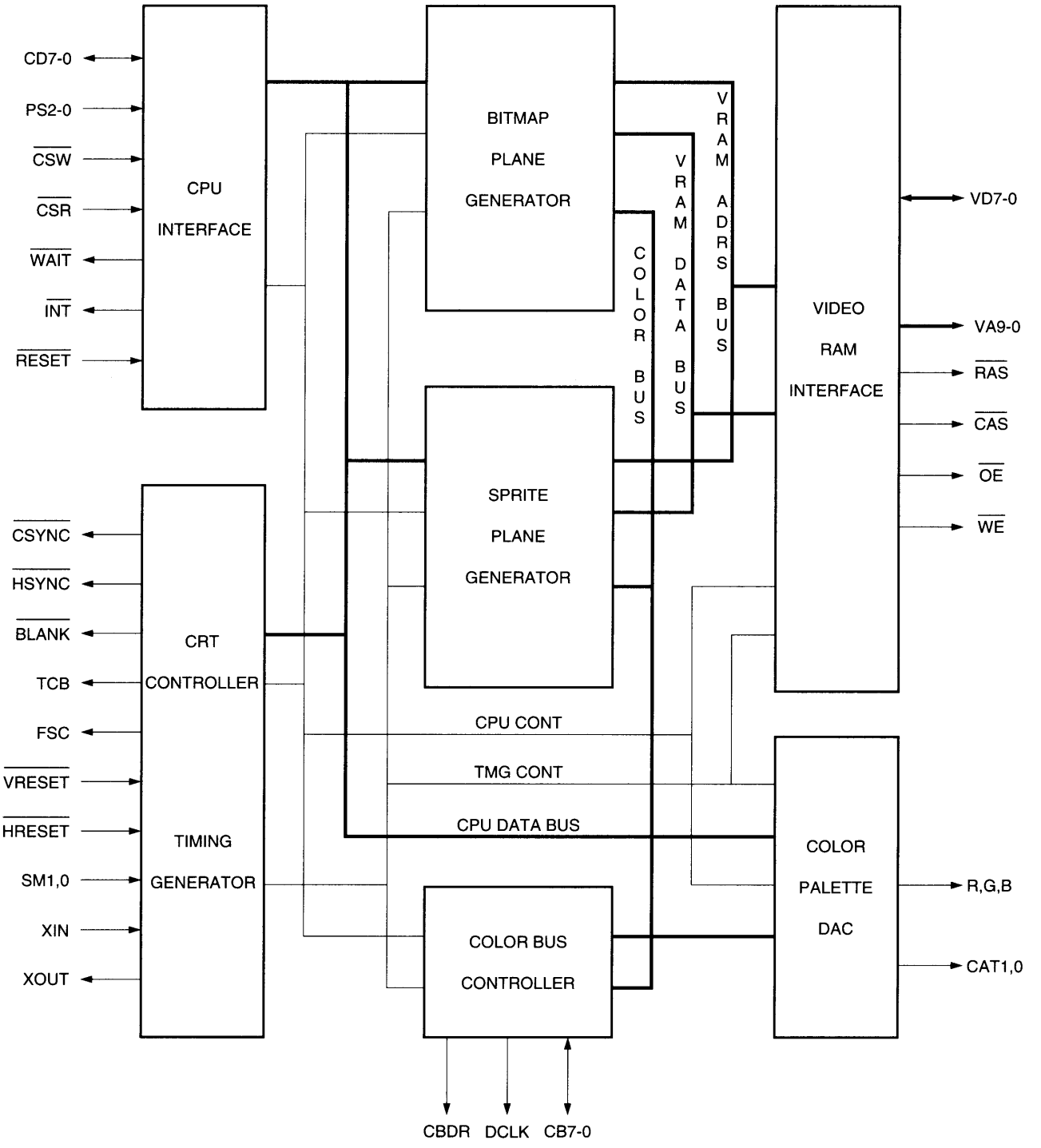
  VRAM capacity 256K dots : 256K word × 4 bits × 1
  1M dots : 1M word × 4 bits × 1

  Modes other than the above

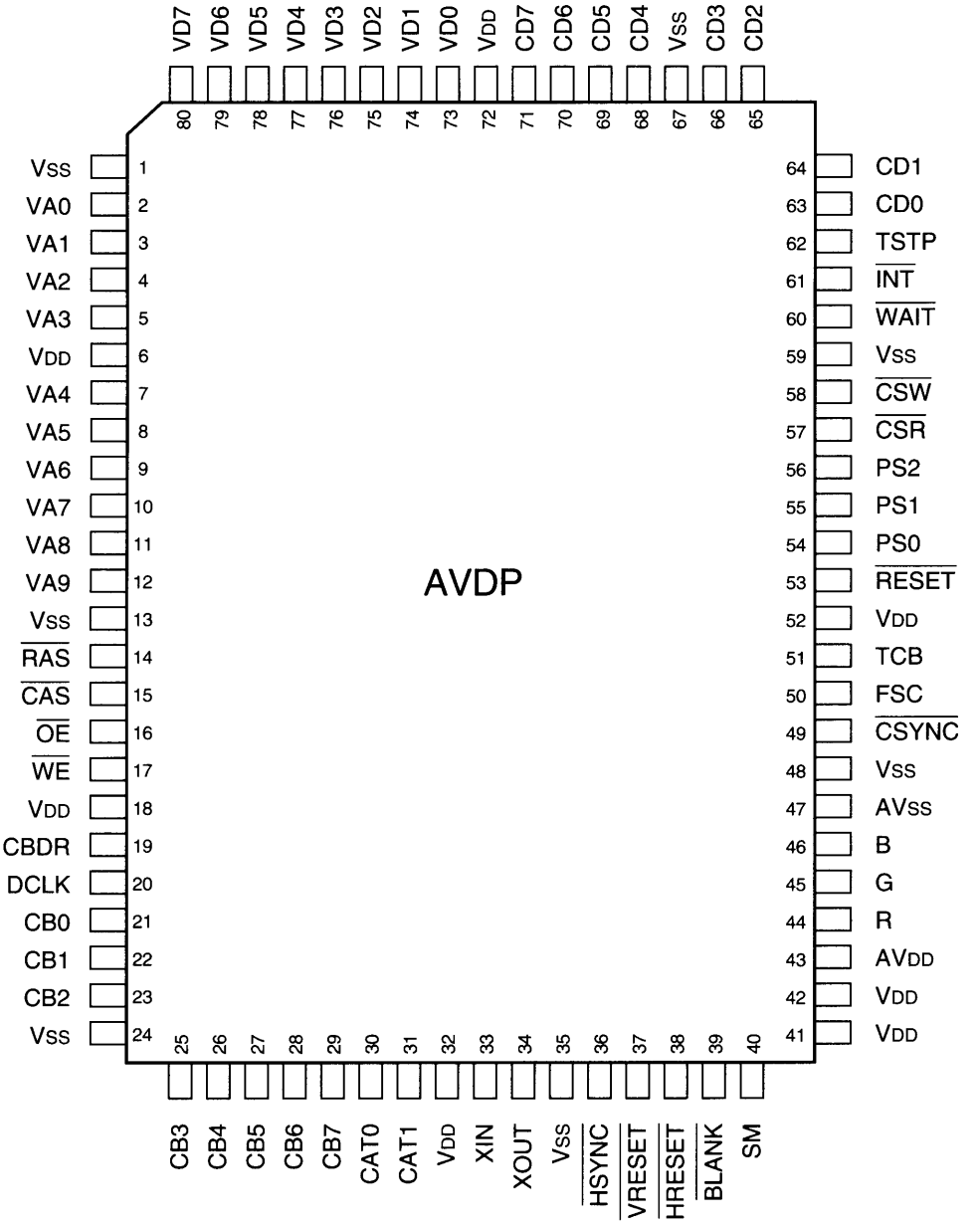
  VRAM capacity 256K dots : 256K word × 4 bits × 2
  512K dots : 512K word × 8 bits × 1
  1M dots : 1M word × 4 bits × 2

- CPU interface: 8-bit parallel data bus
  Wait function during VRAM access
  Various interruption functions (Vertical display period completion, display position, drawing command completion)
  High-speed register and color pallet access is made possible by an automatic address increment function.
- Package: 80-pin plastic QFP, CMOS, 5 V single power supply

■ BLOCK DIAGRAM



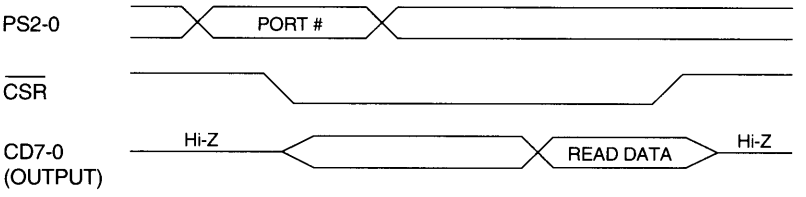
■ PIN ASSIGNMENT



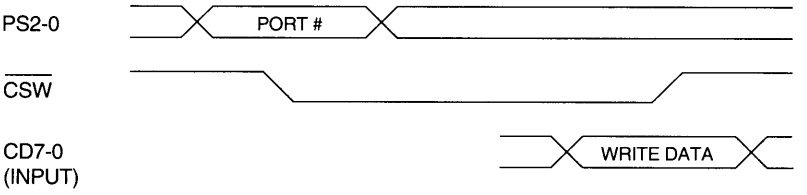
■ TERMINAL FUNCTION

1) CPU interface

- CD7-0 (I/O)
  8-bit bi-directional CPU data bus.
- PS2-0 (I)
  I/O port No. specification input. Selects P#6 – P#0 of AVDP.
- $\overline{CSW}$ (I)
  Strobe signal input for AVDP data write from the CPU.
- $\overline{CSR}$ (I)
  Strobe signal input for AVDP data read out from the CPU.



CPU-AVDP READ CYCLE



CPU-AVDP WRITE CYCLE

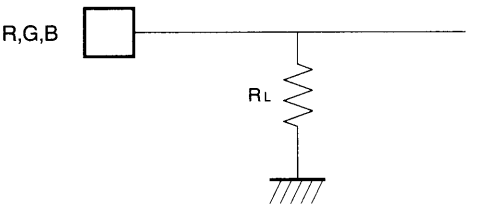
- $\overline{WAIT}$ (O: Open drain output)
  Output of wait signal to the CPU.
- $\overline{INT}$ (O: Open drain output)
  Output of the interruption request signal to the CPU.
- $\overline{RESET}$ (I)
  Power on reset input. AVDP is initialized during low level.

2) VRAM interface

- VD7-0 (I/O)
  VRAM data bus.
- VA9-0 (O)
  VRAM address bus.
- $\overline{RAS}$ (O)
  DRAM row address strobe signal for VRAM.
- $\overline{CAS}$ (O)
  DRAM column address strobe signal for VRAM.
- $\overline{OE}$ (O)
  DRAM data output enable signal for VRAM.
- $\overline{WE}$ (O)
  DRAM write enable signal for VRAM.

3) CRT interface

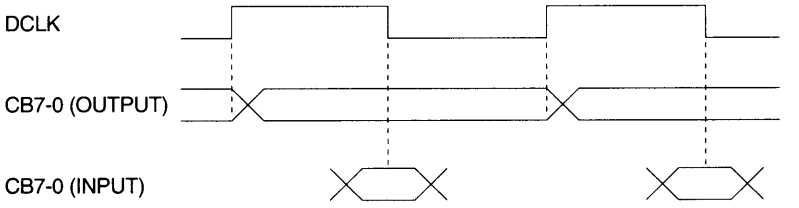
• R, G, B (O: analog output)
Linear RGB output.



• CAT 1, 0 (O)
Attribute timing output of the color code. It is output at the linear RGB output timing of the color code in accordance with AT1 and AT0 of the color palette.

• CB7-0 (I/O)
Display color code output of the AVDP (2 dots earlier than the linear RGB), or display color code input to the AVDP.

• DCLK (O)
Dot clock output. The input and output of the terminals CB7 to 0 synchronize this clock.



• CBDR (O)
This shows the input and output status of terminals CB7 to 0
When the level of CBDR is low, CB7 to 0 function as an input terminal. Conversely, when the level of CBDR is high, CB7 to 0 function as an output terminal.

• $\overline{\text{CSYNC}}$ (O)
Composite synchronizing signal or vertical synchronous signal.

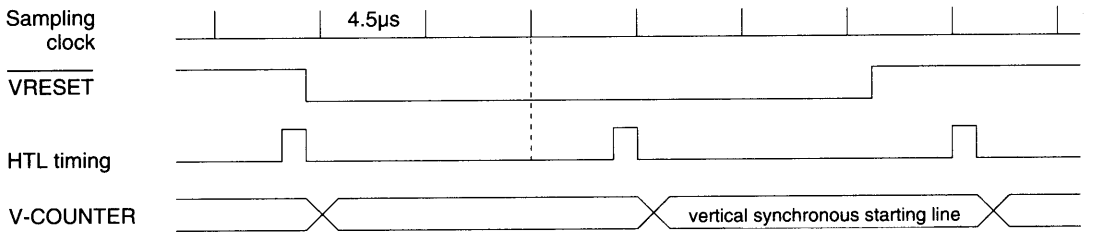
• $\overline{\text{HSYNC}}$ (O)
Horizontal synchronous signal. Equalizing pulse is not inserted. The synchronous signal width can be selected from two types: normal width and 50% duty width.

• $\overline{\text{BLANK}}$ (O)
Retrace line blanking interval.

• FSC (O)
Sub-carrier clock output for NTSC video encoder. It is effective only in NTSC mode.

• $\overline{\text{VRESET}}$ (I)

Vertical timing reset input. The input signal to this terminal is sampled with a cycle clock of approx. 4.5 µsec, when low level is detected three times in succession, the internal V counter is reset to the vertical synchronous starting line of the even number field at the next HTL timing (HSYNC starting timing).



• $\overline{\text{HRESET}}$ (I)

Horizontal timing reset input. AVDP horizontal timing is set to the horizontal synchronous starting position during the fall of this signal. The phase of the dot clock in relation to the main clock is fixed. It can be used for synchronization when using two AVDP's (same clock input) but cannot be used otherwise.

• TCB (O)

Color burst insertion timing signal.

• SM (I)

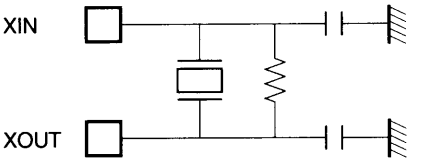
Scan mode selection input.

SM	Scan mode
High	NTSC
Low	PAL

4) Clock

• XIN (I), XOUT (O)

Crystal oscillator connection terminal. External transmission clock should be input to the XIN terminal.



5) Power supply

• AVDD, AVSS (I)

Analog power supply input for RGB.

• VDD, VSS (I)

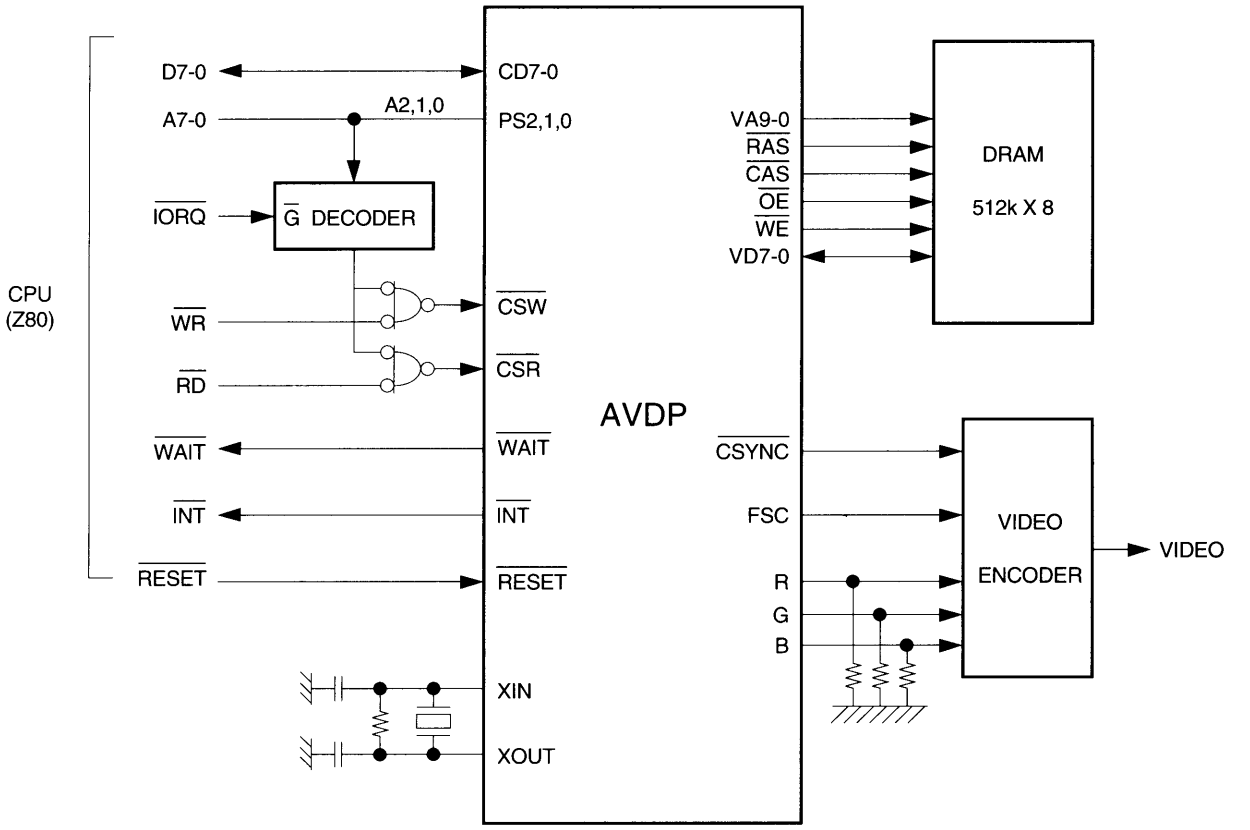
Digital power supply input.

6) Others

• TSTP (I)

Input for internal circuit test. Normally used when high or N.C. is input. When low level is input, the operation cannot be guaranteed.

■ SYSTEM CONFIGURATION EXAMPLE



■ ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5~+7.0	V
Input terminal voltage	V_I	–0.5~V_{DD}+0.5	V
Output terminal voltage	V_O	–0.5~V_{DD}+0.5	V
Output terminal current	I_O	–20~+20	mA
Storage temperature	Tstg	–50~+125	°C

• Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.75	5.00	5.25	V
Supply voltage	V_{SS}		0		V
Low-level Input voltage (except for the XIN terminal)	V_{IL}	–0.3		0.8	V
High-level Input voltage (except for the XIN terminal)	V_{IH}	2.0		V_{DD}+0.3	V
Low-level Input voltage (the XIN terminal)	V_{IL}	–0.3		1.5	V
High-level Input voltage (the XIN terminal)	V_{IH}	3.5		V_{DD}+0.3	V
Ambient operating temperature	Top	0		70	°C

• Electrical Characteristics Under Recommended Operating Conditions

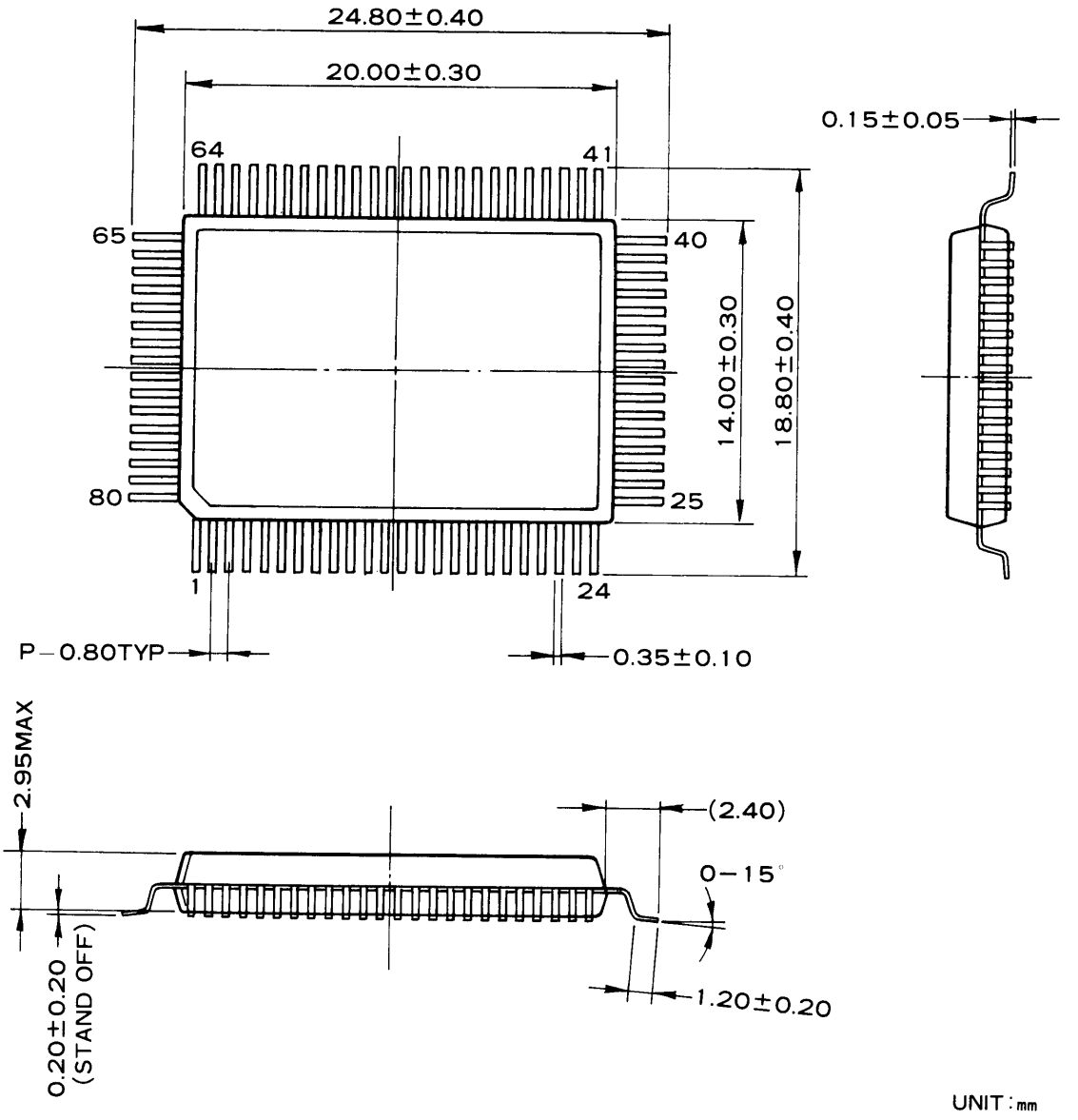
• DC Characteristics

Item	Symbol	Measuring conditions	Min.	Typ.	Max.	Unit
Low-level output voltage	V_{OL}	I_{OL}=1.6 mA			0.4	V
High-level output voltage (except for the OPEN DRAIN terminal)	V_{OH}	I_{OH}=–1.0 mA	4.0			V
Input leakage current	I_{LI}				10	µA
Output leakage current	I_{LO}				25	µA
Power consumption	I_{DD}				60	mA

• Terminal capacity

Item	Symbol	Min.	Typ.	Max.	Unit
Input terminal capacity	C_I			8	pF
Output terminal capacity	C_O			10	
Input/Output terminal capacity	C_{IO}			12	

■ EXTERNAL DIMENSION



Note : The LSIs for surface mount need especial consideration on storage and soldering conditions. For detailed information, please contact your nearest agent of yamaha.

■ MEMO

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