PRELIMINARY

VES9600

SINGLE CHIP

DVB-T

CHANNEL RECEIVER

FEATURES

- 2K and 8K COFDM demodulator (Fully DVB-T compliant : ETS 300-744).
- All modes supported including hierarchical modes.
- On chip 9-bit ADC.
- Digital down conversion.
- Fully automatic transmission parameters detection.
- Crystal or VCXO clock generation.
- Frequency offset estimator to speed up the scan.
- RF Tuner input power measurement
- On chip FEC decoder, full DVB-T compliant.
- Parallel or serial transport stream interface.
- DSP based synchronization.
- BER measurement
- SNR estimation
- Channel frequency response output.
- Channel impulse response output.
- Controllable dedicated I2C tuner bus.
- 2 low frequency spare DAC. ($\Delta\Sigma$)
- Spare I/O.
- I2C bus interface, for easy control.
- CMOS 0.35µm technology.

APPLICATIONS

- DVB-T fully compatible.
- Digital data transmission using COFDM modulations.

DESCRIPTION

The VES9600 is a single chip channel receiver for 2K and 8K COFDM modulated signals based on the ETSI specification (ETSI 300 744). The device interfaces directly to an IF signal, which is sampled by a 9-bit AD converter.
The VES9600 performs all the COFDM demodulation tasks from IF signal to the MPEG2 transport stream. An internal DSP core manages the synchronization and the control of the demodulation process.
After base band conversion and FFT, the channel frequency response is estimated based on the scattered pilots, and filtered in both time and frequency domains. This estimation is used as a correction on the signal, carrier by carrier. A common phase error and estimator is used to deal with the tuner phase noise.
The FEC decoder is automatically synchronized thanks to the frame synchronization algorithm that uses the TPS information included in the modulation. Finally descrambling according to DVB-T standard, is achieved at the Reed Solomon output.

This device is controlled via an I2C bus. The chip provides a switchable tuner I2C bus to be disconnected from the I2C master when not necessary. The DSP software code can be fed to the chip via the master I2C bus or via a dedicated I2C bus (Eeprom).

Designed in 0.35 µm CMOS technology and housed in a 208-pin MQFP package, the VES9600 operates over the commercial temperature range.

CAUTION

This document is preliminary and is subject to change. Contact a VLSI Technology representative to determine if this is the current information on this device.

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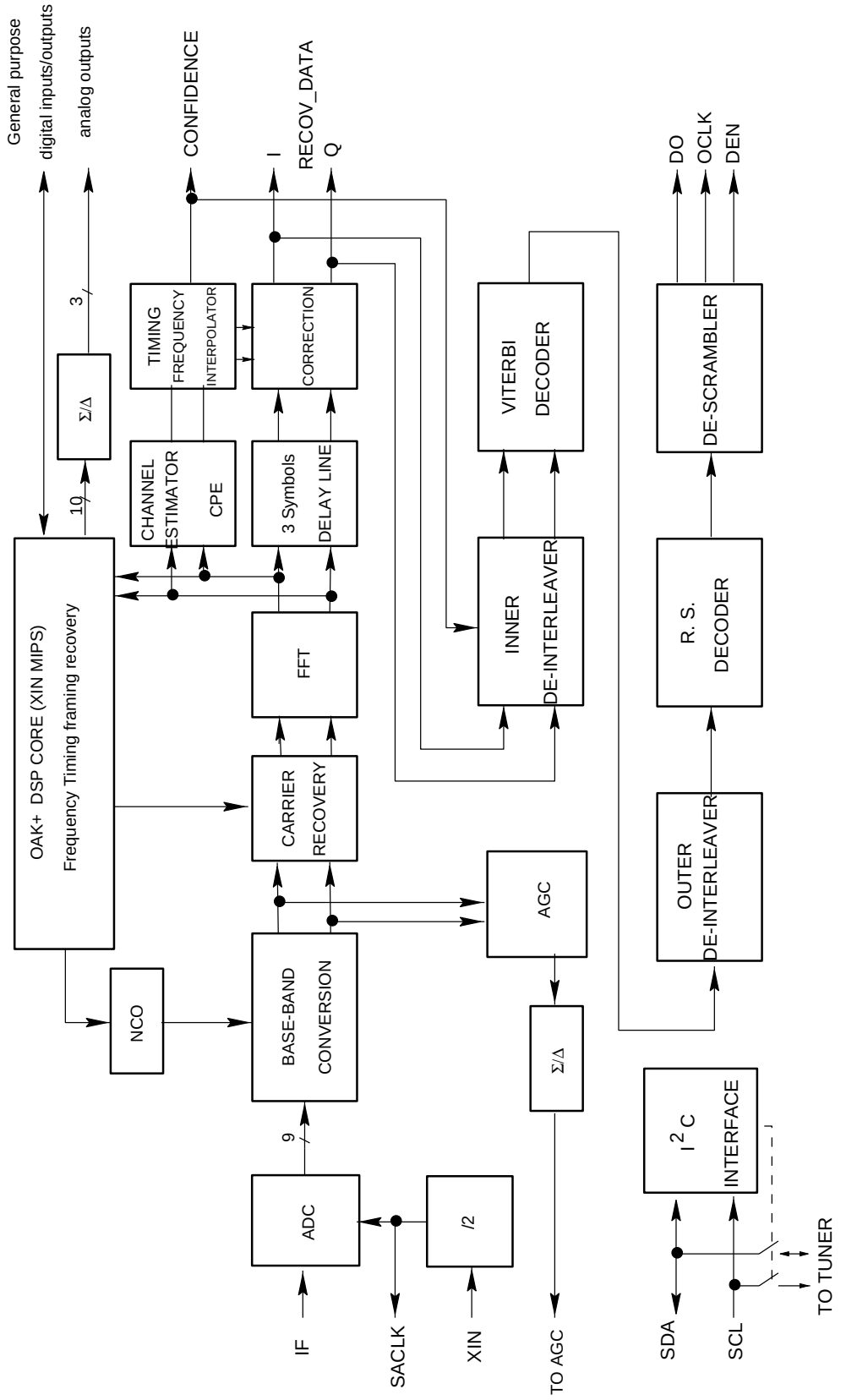
VES9600 Data sheet revision history

Revision number	**Observation**
Rev1.0	Engineering document
Rev1.1	Typo errors
Rev1.2	Pin 7, 17, 70 & 200 from VCC to VDD

FIGURE 1 : FUNCTIONAL BLOCK DIAGRAM



INPUT - OUTPUT SIGNAL DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
CLOCK AND RESET SIGNALS			
CLR#	32	I	reset signal, active low
XIN	8	I	Crystal oscillator input pin. When USE_NCO pin is high a third overtone XTAL should be connected between the XIN and XOUT pins. When USE_NCO pin is low a VCXO should be connected between XIN and via a RC filter to the CTRL_VCXO output.
XOUT	9	O	Crystal oscillator output pin.
SACLK	25	O (5V)	Sampling frequency output. This output clock can be fed to an external (10-bit) ADC as sampling clock. SACLK= XIN/2
USE_NCO	33	I	When low the chip is in VCXO mode else in NCO mode
CTRL_VCXO	26	O (5V)	If not in NCO mode, control of an external sampling VCXO (after low-pass filtering)
CLK_X1	181	O (5V)	Internal SACLK equivalent monitoring output.
CLK_X2	180	O (5V)	Internal SACLK* 2 equivalent monitoring output.
DEMODULATOR SIGNALS			
FI[9:0]	12-13-14-15-16-19-20-21-22-23	I	Input data from an external ADC, FI must be tied to ground when not used, positive notation (from 0 to 1023) or two's complement notation (from -512 to 511).
FFT_WIN_IN	81	I	to be connected to FFT_WIN_OUT in default mode.
FFT_WIN_OUT	82	O (3.3)	Output signal, indicating the start of the active data; equals 1 during complex sample 0 of the active FFT block
VAGC	27	O (5V)	output value from the Delta-Sigma Modulator, used to control a log-scaled amplifier (after analog filtering)
RECOV_DATA [7:0]	168-169-170-171-172-173-174-175	O (3.3)	Demodulator output signal (after channel correction), synchronous with the falling edge of CLK_X1, provided in a multiplexed way, I first. Normal order.
CFND[3 :0]	151-152-153-154	O (3.3)	Multiplexed output bearing the confidence factor during I and channel response square amplitude during Q (4 MSB bits), respectively to RECOV_DATA. (For the channel square amplitude see C2_H2)
H2[3:0]	160-161-162-163	O (3.3)	4 LSB bits of the channel response square amplitude according to CFND.
EN_CLK	150	O (3.3)	enable clk18 to synchronize and phase the RECOV_DATA H2 et CFND outputs. EN_CLK is set to 1 during I and 0 during Q.
D_START	145	O (3.3)	Output signal, indicating the start of the active data out of the equalizer; equals 1 during sample Kmin of the RECOV_DATA current output block, for 2 18MHz clock cycles. CAUTION : sample Kmin does not convey regular data, since it happens to be a continual carrier; it is the first active (non zero) sample of the current OFDM block, but D_VAL and TPS_VAL (see below) will be low.
D_VAL	144	O (3.3)	active when RECOV_DATA corresponds to regular data .
FRAME	147	O (3.3)	Indicate the active data out of the first block in a frame at the demodulation part output. (RECOV_DATA)
SUPER_FRAME	146	O (3.3)	Same as FRAME in 8K; in 2K, active only on the first block of each superframe. Indicates the beginning of a new SUPER-FRAME.
TPS_VAL	143	O (3.3)	active when RECOV_DATA corresponds to TPS demodulated data .
FEL	77	0 (5V)	front end lock. FEL is an output drain output and therefore requires an external pull up resistor.

IT	76	O (5V)	Interrupt line. This output interrupt line can be configured by the I2C interface. See registers Itsel and Itstat. IT is an open drain output and therefore requires an external pull up resistor.

FEC OUTPUTS			
DO[7:0]	118-119-120-121-124-125-126-127	O (3.3)	output data carrying the current sample of the current MPEG2 packet (188 bytes), delivered on the rising edge of OCLK by default. When the serial mode is selected, the output data is delivered by DO[0].
OCLK	113	O (3.3)	Output CLock. OCLK is the output clock for the parallel DO[7:0] outputs. OCLK is internally generated depending on which interface is selected.
DEN	115	O (3.3)	output data validation signal active high during the valid and regular data bytes (may be inverted, see serial bus description).
PSYNC	112	O (3.3)	Pulse SYNChro. This output signal goes high on a rising edge of OCLK when a synchro byte is provided, then goes low until the next synchro byte (may be inverted).
UNCOR	114	O (3.3)	RS error flag, active high on one RS packet if the RS decoder fails in correcting the errors (may be inverted).
FSTART	109	O (3.3)	Frame start active high for one OCLK output clock cycle at the beginning of a new superframe made of 272 OFDM symbols for the 2k mode and made of 68 OFDM symbols for the 8k mode (may be inverted as C3_psync).
DVIT	108	O (3.3)	viterbi output data stream, delivered on the rising hedge of HVIT. You can also find the viterbi output on DO[0] after by-passing the RS and the descrambling.
HVIT	107	O (3.3)	viterbi output data stream clock, according to DVIT.

ON-CHIP ADC SIGNALS			
VIM	48	I	Negative input to the A/D converter. This pin is DC biased to half supply through an internal resistor divider (2x10K resistors). In order to remain in the range of the ADC, the voltage difference between pins VIP and VIM should be between -0.5 and 0.5 volts.
VIP	49	I	Positive input to the A/D converter. This pin is DC biased to half supply through an internal resistor divider (2x10K resistors). In order to remain in the range of the ADC, the voltage difference between pins VIP and VIM should be between –0.5 and 0.5 volts.
CMCAP	42	I	This pin is connected to a tap point on an internal resistor divider used to create CMO and CMI. An external capacitor of value 0.1µf should be connected between this point and ground to provide good power supply rejection from the positive supply at higher frequencies.
RBIAS	39	I	An external resistor of value 3.3kΩ should be connected between this pin and ground to provide good accurate bias currents for the analog circuits on the ADC.
CMI	40	O	This pin provides the common-mode in voltage for the analog circuits on the ADC. It is the buffered version of a voltage derived from an on-chip resistor devider, and has a nominal value of 0.75 x VD3.
CMO	41	O	This pin provides the common-mode out voltage for the analog circuits on the ADC. It is the buffered version of a voltage derived from an on-chip resistor devider, and has a nominal value of 0.5 x VD3.
VREF	45	O	This is the output of an on-chip resistor divider. An external capacitor of value 0.1µf should be connected between this point and ground to provide good power supply rejection from the positive supply at higher frequencies. Reference voltages VREFP and VREFM are derived from the voltage on VREF.
VREFP	44	O	This is a positive voltage reference for the A/D converter. It is derived

			from the voltage on pin VREF through an on-chip fully-differential amplifier. The voltage on this pin is nominally equal to CMO + 0.25 volts.
VREFM	43	O	This is the negative voltage reference for the A/D converter. It is derived from the voltage on pin VREF through an on-chip fully-differential amplifier. The voltage on this pin is nominally equal to CMO- 0.25 volts.
VD1	38	I	Power supply input for the digital switching circuitry (3.3 typ).
VS1	37	I	Ground return for the digital switching circuitry.
VD2	51	I	Power supply input for the analog clock drivers (3.3V typ).
VS2	50	I	Ground return for the analog clock drivers.
VD3	46	I	Power supply input for the analog circuits (3.3V typ).
VS3	47	I	Ground return for analog circuits.
VD4	52	I	Power supply input that connects to an n-well guard ring that surrounds the ADC (3.3V typ).
VS4	36	I	Ground return for the well guard ring that surrounds the ADC.

I2C INTERFACES			
SCL	62	I	I2C serial clock. Up to 700 kbit/s, in this functional mode, I2C slave device
SDA	63	I/O	I2C serial data inout, open drain I/O pad Up to 700 kbit/s, in this functional mode, I2C slave device
SADDR[1:0]	206-207	I	SADDR[1:0] are the 2 LSBs of the I2C address of the VES9600. The MSBs are internally set to 00010. Therefore the complete I2C address of the VES9600 is (MSB to LSB): 0,0,0,1,0,SADDR[1], SADDR[0]
SCL_TUN	64	O	tuner I2C serial clock signal. Can be connected or not to the master I2C bus. (open drain)
SDA_TUN	65	I/O	Tuner I2C data bus. Can be connected or not to the master I2C bus. (open drain)
SCL_EEP	66	O	Extra I2C clock line to download DSP code from an external EEPROM. Optional mode. Can be connected to the master I2C Bus , (open drain)
SDA_EEP	67	I/O	Extra I2C data bus to download DSP code from an external EEPROM. Optional mode. Can be connected to the master I2C Bus. (open drain)
EEPADDR[1:0]	204-205	I	EEPRAD[1:0] are the 2 LSBs of the I2C address of the EEPROM in mode boot alone. The MSBs are internally set to 00010. Therefore the complete I2C address of the EEPROM is (MSB to LSB): 1,0,1,0,0,EEPADDR[1], EEPADDR[0]
EEPSP[1:0]	202-203	I	I2C EEPROM bus speed (SCL_EEP) : 0 : 800Khz; 1 : 400Khz; 2 : 200Khz; 3 : 100Khz.

DSP SIGNALS			
DOWNLOAD_MODE	4	I	processor control, Boot Mode If 0 the DSP download its software from an external eeprom on the dedicated I2C BUS SDA_EEP and SCL_EEP. If 1 the software is downloaded via a host in the I2C register CODE_IN. In this case no need of an external eeprom.
DSP_BIST	3	I	Boot on the bist mode to test the DSP RAM bank. If good SP_OUT[0] = 1 In normal mode of operation, DSP_BIST must be grounded.
SDI_TCK	194	I	Oak+ DSP smart debug interface, SDI+ external JTAG clock
SDI_TDI	195	I	Oak+ DSP smart debug interface, SDI+ JTAG serial output
SDI_TMS	196	I	Oak+ DSP smart debug interface, SDI+ JTAG test mode select
SDI_TDO	197	O	Oak+ DSP smart debug interface, SDI+ JTAG serial output

		(3.3)	
SP_IN[3:0]	72-73-74-75	I	Spare inputs
SP_OUT[7:0]	88-89-90-91-92-93-94-95	O (3.3)	Spare outputs
CTRL[1:0]	84-85	O (3.3)	control detection signal, flag monitoring outputs.
DS_SPARE_1	28	O (5V)	Spare delta-sigma output. Managed by the DSP to handle a low frequency DAC. (automatic first stage tuner AGC measurement for example).
DS_SPARE_2	29	O (5V)	Spare delta-sigma output. Managed by the DSP or by an I2C register to generate an analog level. (after a RC low-pass filter)
TESTADC	55	I	Must be set to “1”

BOUNDARY SCAN			
TCK	187	I	clock signal for boundary-scan. Wired to GND (if not used)
TDI	188	I	Input port for boundary-scan. Wired to GND (if not used)
TMS	190	I	Mode programming signal for boundary-scan. Wired to GND (if not used)
TRST	189	I	Asynchronous reset signal for boundary-scan. Wired to GND (if not used)
TDO	191	O (5V)	Output port for boundary-scan. NC (if not used)

POWER SUPPLIES			
GND	2-10-18-31-69-71-80-87-97-117-123-134-142-149-165-177-183-193-201	GN	Ground level 0 V
VCC	1-30-68-79-192	VCC 5V	Positive Power Supply 5 V typical
VDD	7-17-70-86-96-116-122-133-141-148-164-176-182-200	VDD 3.3V	Positive Power Supply 3.3 V typical

FIGURE 2 : BLOCK DIAGRAM

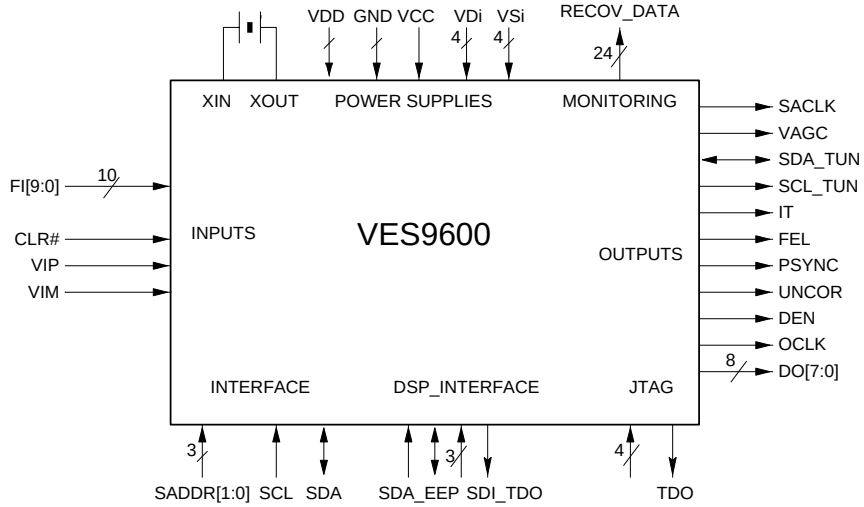


FIGURE 3 : PIN DIAGRAM

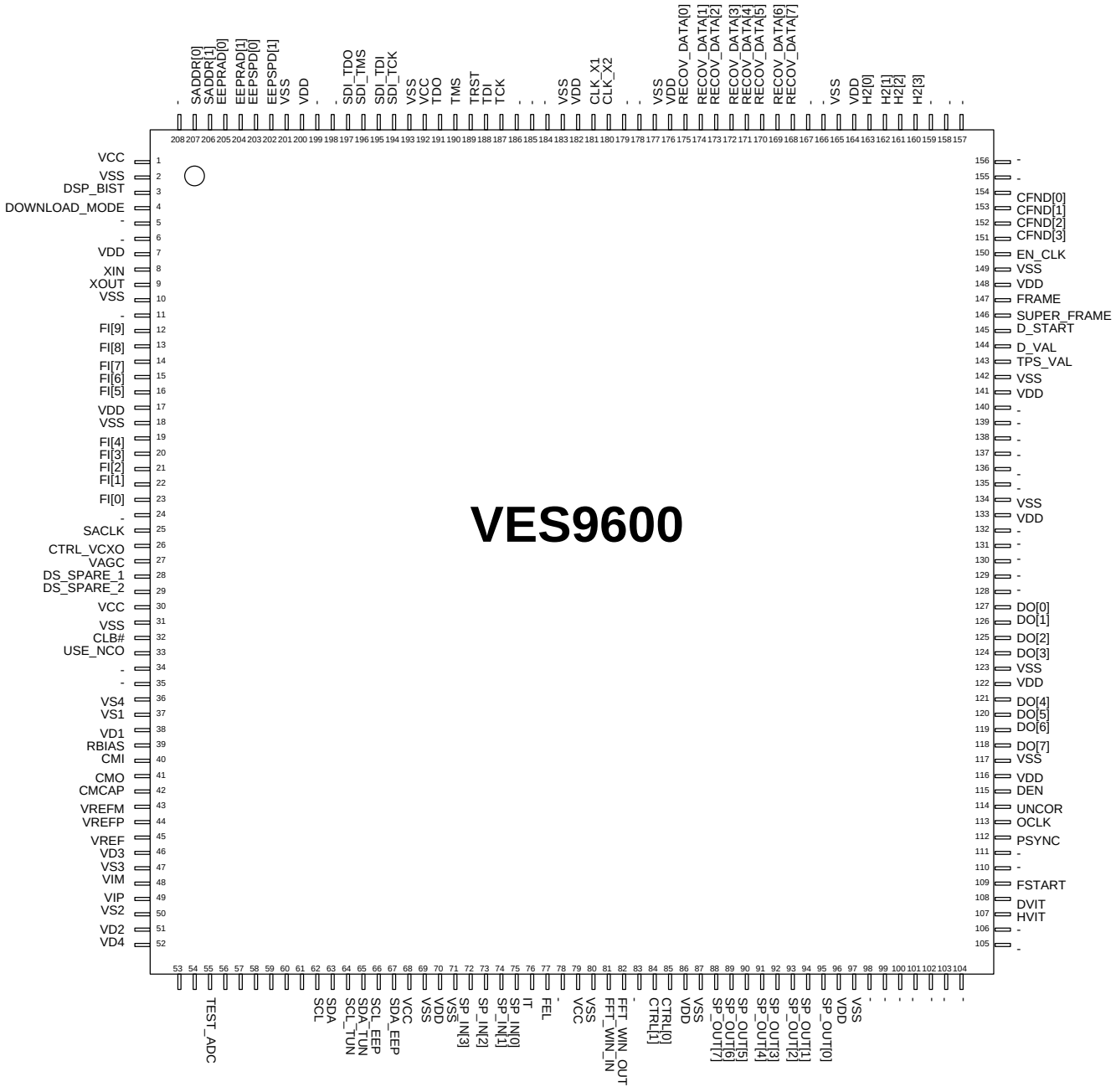


TABLE 1 : PIN DESCRIPTION

Pin	Pin Name	Direction
1	VCC	-
2	VSS	-
3	DSP_BIST	I
4	DWNLD_MODE	I
5	-	I^3
6	-	I^3
7	VCC	-
8	XIN	I
9	XOUT	O
10	VSS	-
11	-	I^3
12	FI[9]	I
13	FI[8]	I
14	FI[7]	I
15	FI[6]	I
16	FI[5]	I
17	VCC	-
18	VSS	-
19	FI[4]	I
20	FI[3]	I
21	FI[2]	I
22	FI[1]	I
23	FI[0]	I
24	-	I^3
25	SACLK	O
26	CTRL_VCXO	O
27	VAGC	O
28	DS_SPARE_1	O
29	DS_SPARE_2	O
30	VCC	-
31	VSS	-
32	CLR#	I
33	USE_NCO	I
34	-	I^3
35	-	I^3
36	VS4	-
37	VS1	-
38	VD1	-
39	RBIAS	I
40	CMI	O
41	CMO	O
42	CMCAP	I
43	VREFM	O
44	VREFP	O
45	VREF	O
46	VD3	-
47	VS3	-
48	VIM	I
49	VIP	I
50	VS2	-
51	VD2	-
52	VD4	-
53	-	-
54	-	-
55	TEST_ADC	I
56	-	I^3
57	-	O^3
58	-	O^3
59	-	O^3
60	-	O^3
61	-	O^3
62	SCL	I
63	SDA	I/O
64	SCL_TUN	OD
65	SDA_TUN	I/O
66	SCL_EEP	OD
67	SDA_EEP	I/O
68	VCC	-
69	VSS	-
70	VCC	-
71	VSS	-
72	SP_IN[3]	I
73	SP_IN[2]	I
74	SP_IN[1]	I
75	SP_IN[0]	I
76	IT	OD
77	FEL	OD
78	-	I^3
79	VCC	-
80	VSS	-
81	FFT_WIN_IN	I^1
82	FFT_WIN_OUT	O
83	-	I^3
84	CTRL[1]	O
85	CTRL[0]	O
86	VDD	-
87	VSS	-
88	SP_OUT[7]	O
89	SP_OUT[6]	O
90	SP_OUT[5]	O
91	SP_OUT[4]	O
92	SP_OUT[3]	O
93	SP_OUT[2]	O
94	SP_OUT[1]	O
95	SP_OUT[0]	O
96	VDD	-
97	VSS	-
98	-	I^3
99	-	I^3
100	-	I^3
101	-	I^3
102	-	I^3
103	-	I^3
104	-	I^3
105	-	I^3
106	-	I^3
107	HCORE	O
108	DCORE	O
109	FSTART	O
110	-	O^3
111	-	I^3
112	PSYNC	O
113	OCLK	O
114	UNCOR	O
115	DEN	O
116	VDD	-
117	VSS	-
118	DO[7]	O
119	DO[6]	O
120	DO[7]	O
121	DO[4]	O
122	VDD	-
123	VSS	-
124	DO[3]	O
125	DO[2]	O
126	DO[1]	O
127	DO[0]	O
128	-	I^3
129	-	I^3
130	-	I^3
131	-	I^3
132	-	O^3
133	VDD	-
134	VSS	-
135	-	O^3
136	-	O^3
137	-	I^3
138	-	I^3
139	-	I^3
140	-	I^3
141	VDD	-
142	VSS	-
143	TPS_VAL	O
144	D_VAL	O
145	D_START	O
146	SUPER_FRAME	O
147	FRAME	O
148	VDD	-
149	VSS	-
150	EN_CLK	O
151	CFND[3]	O
152	CFND[2]	O
153	CFND[1]	O
154	CFND[0]	O
155	-	I^3
156	-	-
157	-	I^3
158	-	I^3
159	-	I^3
160	H2[3]	O
161	H2[2]	O
162	H2[1]	O
163	H2[0]	O

164	VDD	-
165	VSS	-
166	-	O[3]
167	-	I[3]
168	RECOV_DATA[7]	O
169	RECOV_DATA[6]	O
170	RECOV_DATA[5]	O
171	RECOV_DATA[4]	O
172	RECOV_DATA[3]	O
173	RECOV_DATA[2]	O
174	RECOV_DATA[1]	O
175	RECOV_DATA[0]	O
176	VDD	-
177	VSS	-
178	-	O[3]
179	-	I[3]
180	CLK_X2	O

181	CLK_X1	O
182	VDD	-
183	VSS	-
184	-	-
185	-	O[3]
186	-	O[3]
187	TCK	I
188	TDI	I
189	TRST	I
190	TMS	I
191	TDO	OD
192	VCC	-
193	VSS	-
194	SDI_TCK	I
95	SDI_TDI	I
196	SDI_TMS	I
197	SDI_TDO	OD

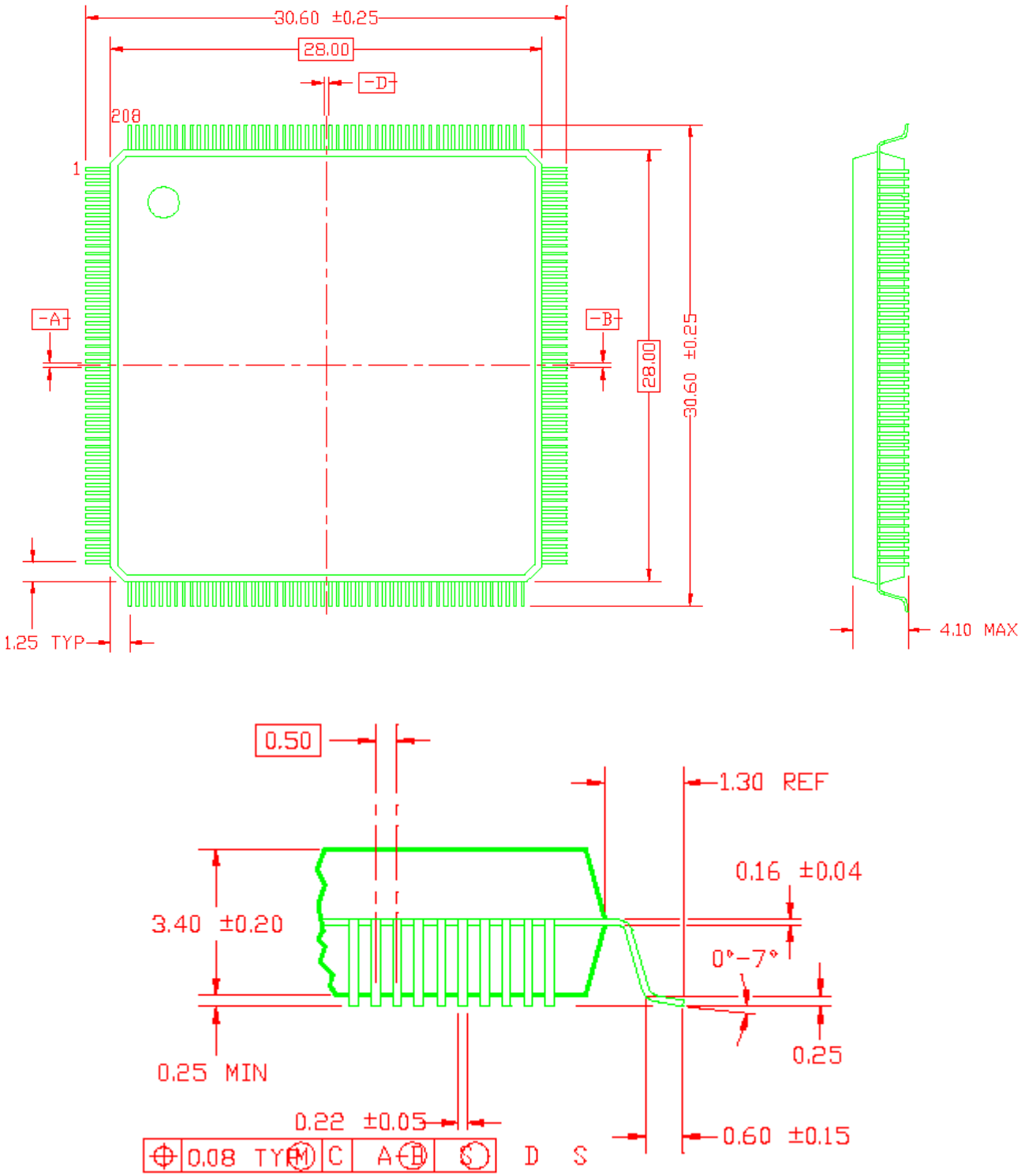
198	-	O[3]
199	-	O[3]
200	VCC	-
201	VSS	-
202	EEPSPD[1]	I
203	EEPSPD[0]	I
204	EEPRAD[1]	I
205	EEPRAD[0]	I
206	SADDR[1]	I
207	SADDR[0]	I
208	-	I[3]

Notes :
1.All inputs (I) are TTL, 5V tolerant inputs (excepted FFT_WIN_IN which is 3.3V only)

2.OD are Open Drain 5V outputs, so they must be connected to a pull-up resistor to either VDD or VCC

3. Test IO, inputs must be connected to GND.

PACKAGE INFORMATION



NOTE : Dimensions are in millimeters