CMOS 4-BIT MICROCONTROLLER

# TMP47C231AN

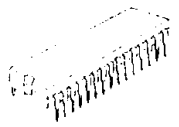
The 47C231A is the high speed and high performance 4-bit single chip microcomputer based on the TLCS-47 CMOS series, remote control signal preprocessor, A/D converter input for AFC signal or key input, 6-bit D/A converter (Pulse Width Modulation) output, and 8-bit serial interface on a chip. The 47C231A is suitable for application to the digital tuning systems for TV and VCR set.

| PART No. | ROM | RAM | PACKAGE | PIGGYBACK (adapter socket) |
|---|---|---|---|---|
| TMP47C231AN | 2048 × 8-bit | 128 × 4-bit | SDIP30 | TMP47C931AE (BM1103) |

## FEATURES

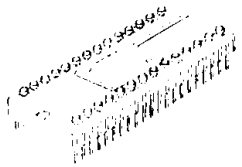
- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 1.9μs (at 4.2MHz)
- ◆90 basic instructions
- ◆Table look-up instructions
- ◆5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting : 15 levels max
- ◆6 interrupt sources (External : 2, Internal : 4)
  All source have independent latches each, and multiple interrupt control is available.
- ◆I/O port (24 pins)
  - Input 2 ports 5 pins
  - I/O 5 ports 19 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Serial Interface with 8-bit buffer
  - Simultaneous transmission and reception capability
  - External/internal clock, leading/trailing edge shift, 4/8-bit mode
- ◆4-bit A/D converter input 5 channels
  - Auto frequency control signal (S-shaped curve) detection
  - For key input
- ◆6-bit D/A converter (pulse width modulation) output
- ◆Remote control signal preprocessing capability
- ◆High current outputs
  LED direct drive capability (typ.20mA × 8 bits)
- ◆Hold function
  Battery/Capacitor back-up
- ◆Real Time Emulator : BM47213A

SDIP30



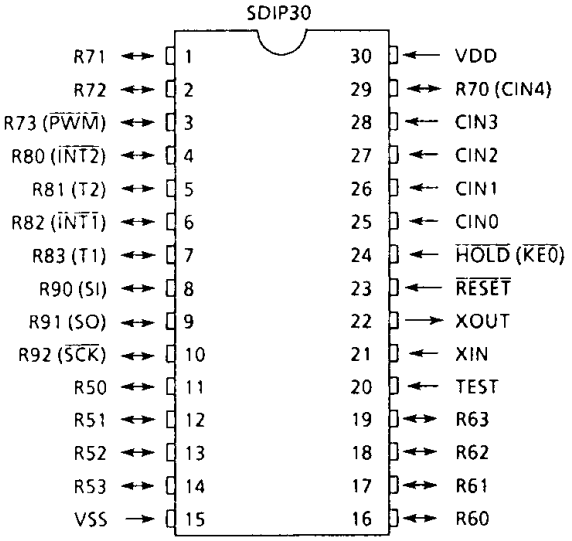
TMP47C231AN

SDIC42

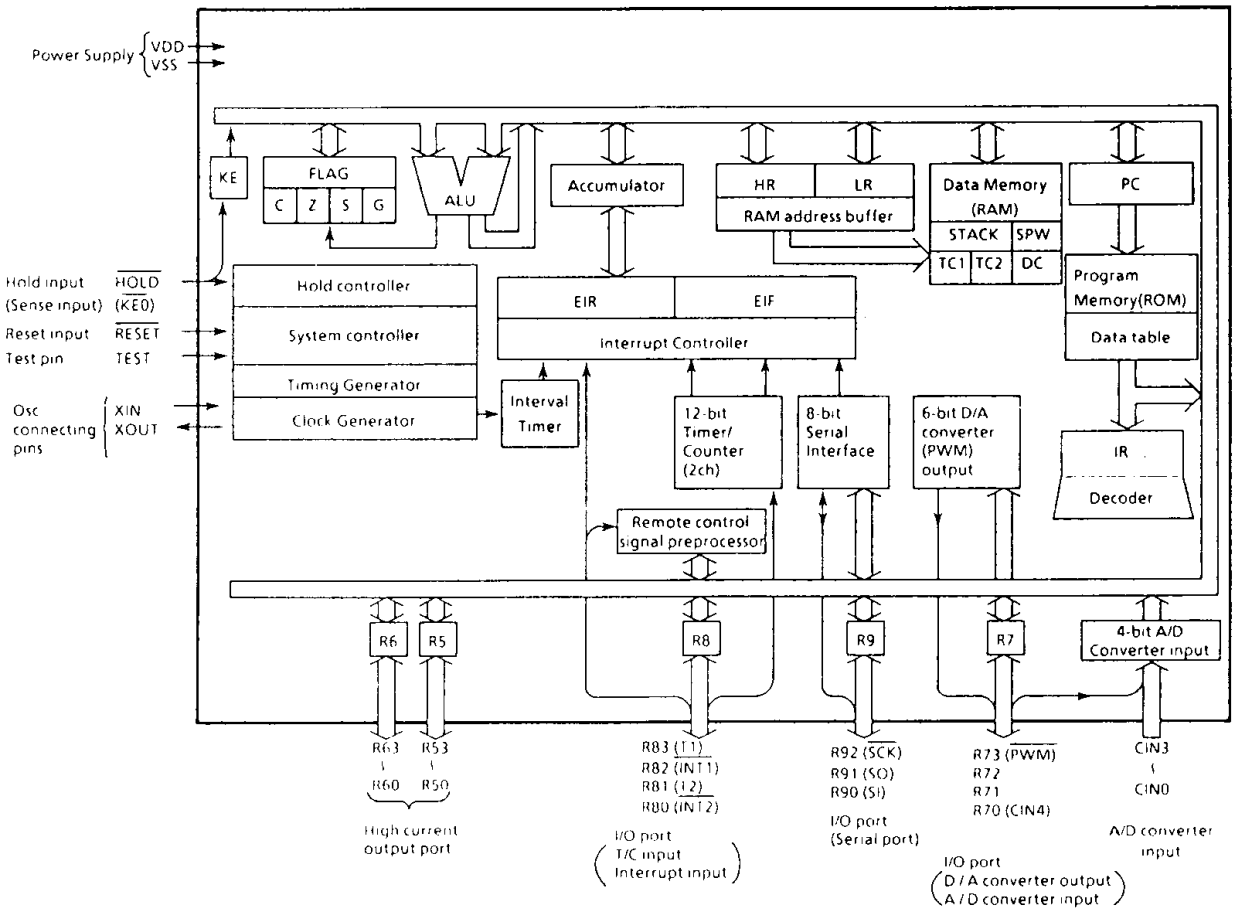


TMP47C931AE

## PIN ASSIGNMENT (TOP VIEW)




## BLOCK DIAGRAM



## PIN FUNCTION

| PIN NAME | Input/Output | FUNCTIONS | |
|---|---|---|---|
| CIN3 - CIN0 | Input | 4-bit A/D converter (comparator) input port | |
| R53 - R50<br>R63 - R60 | I/O | 4-bit I/O port with latch.<br>When using as input port, the latch must be set to "1".<br>8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL]. | |
| R73 ($\overline{PWM}$) | I/O (Output) | 4-bit I/O port with latch.<br>When used as input port, pulse width modulation output pin, comparator input pin, the latch must be set to "1". | 6-bit D/A converter output |
| R72, R71 | I/O | | |
| R70 (CIN4) | Output (Input) | | 4-bit A/D converter (comparator) input |
| R83 (T1) | I/O (Input) | 4-bit I/O port with latch.<br>When used as input port, external interrupt input pin, or Timer/Counter external input pin, the latch must be set to "1". | Timer/Couneter 1 external input |
| R82 ($\overline{INT1}$) | | | External interrupt 1 input |
| R81 (T2) | | | Timer/Counter 2 external input |
| R80 ($\overline{INT2}$) | | | External interrupt 2 input |
| R92 ($\overline{SCK}$) | I/O (I/O) | 3-bit I/O port with latch.<br>When used as input port or serial port, the latch must be set to "1". | Serial clock I/O |
| R91 (SO) | I/O (Output) | | Serial data output |
| R90 (SI) | I/O (Input) | | Serial data input |
| XIN | Input | Resonator connecting pin.<br>For inputting external clock, XIN is used and XOUT is opened. | |
| XOUT | Output | | |
| $\overline{RESET}$ | Input | Reset signal input | |
| $\overline{HOLD}$ ($\overline{KE0}$) | Input (Input) | Hold request/release signal input | Sense input |
| TEST | Input | Test pin for out-going test. Be opened or fixed to low level. | |
| VDD | Power Supply | + 5V | |
| VSS | | 0V (GND) | |

## OPERATIONAL DESCRIPTION

Concerning the 47C231A, the hardware configuration and operation are described. As the description include mainly differences from the 47C200A, refer to the technical data sheets for the 47C200A when checking the CMOS 4-bit single chip microcontroller.

### 1. SYSTEM CONFIGURATION

(1) I/O ports
(2) A / D converter (comparator) input
(3) D / A converter (pulse width modulation) output
(4) Remote control pre-decording circuit
(5) Serial interface

### 2. PERIPHERAL HARDWARE FUNCTION

#### 2.1 I/O ports

The 47C 231A has 7 ports (24 pins) each as follows :

| | | |
|---|---|---|
| ① CIN | ; | 4-bit comparator input |
| ② R5, R6 | ; | 4-bit input/output |
| ③ R7 | ; | 4-bit input/output (Shared by comparator input and pulse width modulation output) |
| ④ R8 | ; | 4-bit input/output (Shared by external interrupt input and Timer/Counter input) |
| ⑤ R9 | ; | 3-bit input/output (Shared by serial port) |
| ⑥ KE | ; | 1-bit sense input (Shared by hold request /release signal input) |

This section describes ports of ①, ② and ③, which are changed from the 47C200A. The 47C231A has no K0, P1 and P2.

Table 2-1. lists the port address assigments and the I/O instructions that can access the ports.

(1) Ports R5 (R53-R50), R6 (R63-R60)

The 4-bit I/O ports with a latch. When used as an input port, the latch should be set to "1". These 2 ports can be accessed separately at port address OP05/IP05. Additionally, 8-bit data can be set to these ports by using the 5-bit to 8-bit data conversion instruction [OUTB @HL].

The latch is initialized to "1" during reset.

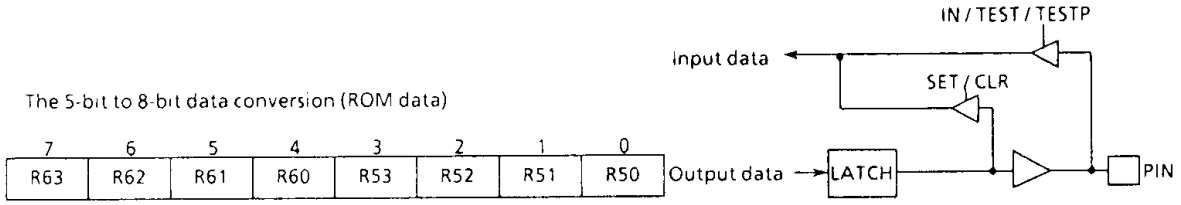



Figure 2-1. Ports R5 and R6

(2) Ports CIN (CIN3-CIN0), R7 (R73-R70)

The CIN ports and R70 pin is 4-bit A/D converter (Comparator) input. The R73 pin shared by pulse width modulatoin output. The R71, R72 pin is I/O pin as usual. When used as an input port, the latch should be set to "1". The latch is initialized to "1" during reset.

| Port Address (••) | Port | | Input/Output instruction | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Input (IP••) | Output (OP••) | IN %p, A<br>IN %p, @HL | OUT A,%p<br>OUT @HL,%p | OUT #k, %p | OUTB @HL | SET %p, b<br>CLR %p, b | TEST %p, b<br>TESTP %p,b | SET @L<br>CLR @L<br>TEST @L |
| $00_H$ | CIN port | —— | – | – | – | – | – | ○ | – |
| 01 | —— | —— | – | – | – | – | – | – | – |
| 02 | —— | —— | – | – | – | – | – | – | – |
| 03 | —— | —— | – | – | – | – | – | – | – |
| 04 | —— | —— | – | – | – | – | – | – | – |
| 05 | R5 input port | R5 output port | ○ | ○ | ○ | ○ (Note 2) | ○ | ○ | ○ |
| 06 | R6 input port | R6 output port | ○ | ○ | ○ | ○ (Note 2) | ○ | ○ | ○ |
| 07 | R7 input port | R7 output port | ○ | ○ | ○ | – | ○ | ○ | ○ |
| 08 | R8 input port | R8 output port | ○ | ○ | ○ | – | ○ | ○ | – |
| 09 | R9 input port | R9 output port | ○ | ○ | ○ | – | ○ | ○ | – |
| 0A | Remote control count register | Remote control offset register | ○ | ○ | ○ | – | – | – | – |
| 0B | —— | —— | – | – | – | – | – | – | – |
| 0C | —— | —— | – | – | – | – | – | – | – |
| 0D | —— | —— | – | – | – | – | – | – | – |
| 0E | SIO Hold status | —— | ○ | – | – | – | – | – | – |
| 0F | Serial receive buffer | Serial transmit buffer | ○ | ○ | ○ | – | – | – | – |
| $10_H$ | Undefined | Hold operating mode control | – | ○ | – | – | – | – | – |
| 11 | Undefined | —— | – | – | – | – | – | – | – |
| 12 | Undefined | Comparator input control | – | ○ | – | – | – | – | – |
| 13 | Undefined | —— | – | – | – | – | – | – | – |
| 14 | Undefined | Remote control single preprocess or control | – | ○ | – | – | – | – | – |
| 15 | Undefined | —— | – | – | – | – | – | – | – |
| 16 | Undefined | —— | – | – | – | – | – | – | – |
| 17 | Undefined | PWM buffer selector | – | ○ | – | – | – | – | – |
| 18 | Undefined | PWM data transfer buffer | – | ○ | – | – | – | – | – |
| 19 | Undefined | Interval Timer interrupt control | – | ○ | – | – | – | – | – |
| 1A | Undefined | —— | – | – | – | – | – | – | – |
| 1B | Undefined | —— | – | – | – | – | – | – | – |
| 1C | Undefined | Timer/Counter 1 control | – | ○ | – | – | – | – | – |
| 1D | Undefined | Timer/Counter 2 control | – | ○ | – | – | – | – | – |
| 1E | Undefined | SIO control 1 | – | ○ | – | – | – | – | – |
| 1F | Undefined | SIO control 2 | – | ○ | – | – | – | – | – |

*Note 1.* *"____" means the reserved state. Unavailable for the user programs.*

*Note 2.* *The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports R5 and R6.*

Table 2-1. Port Address Assignments and Available I/O Instructions

## 2.2 4-bit A/D converter (Comparator) input

The comparator input is analog input to discriminate key input or AFC (Auto Frequency Control) signal. It's composed of 4-bit D/A converter, comparator and control circuit. Analog input level (CIN0-CIN3) can be detected as 16-stage by setting reference voltage.

The comparator input can also be used as K0 port (digital input).

### 2.2.1 Circuit configuration of Comparator input

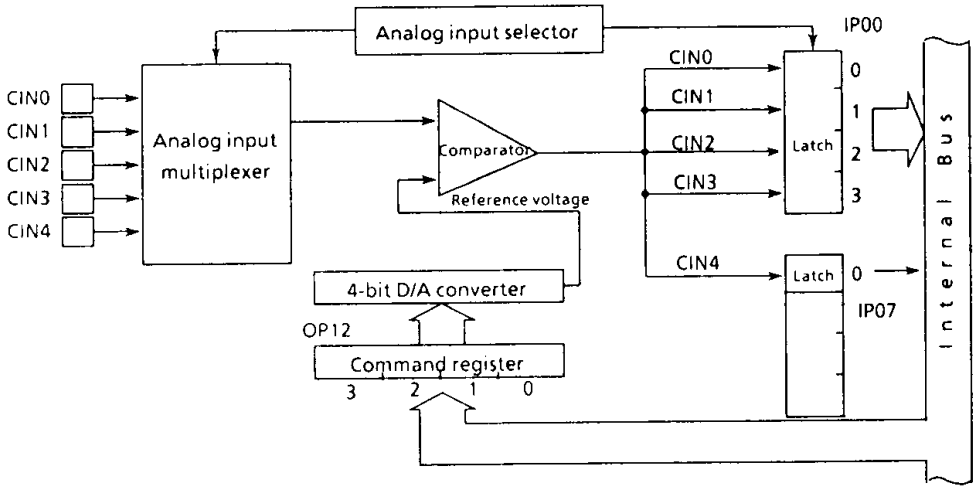



Figure 2-2. Comparator input circuit

### 2.2.2 Control of comparator input

Reference voltage ($V_{REF}$) is set by command register (port address OP12), and it is determined by the following form.

$$V_{REF} = V_{DD} \times (n + 1) / 16 \ [V] \quad (n = 0 \text{ to } 15)$$

After initialization sequence, 5-channel comparator inputs continue comparison operation successively.

Since 2-instruction cycles are required to complete comparison of 1-channel, it is necessary to wait for 10-instruction cycles after setting a reference voltage to read data form the comparator.

When analog input voltage is higher than reference voltage, comparator data latch is set to "1".

At the initialization sequence, OP12 is set to "0".

```
LD      A,#0111B  ; Setting a reference voltage
OUT     A,%OP12
IN      %IP00,A   ; reading a refernce effect
  :               ] 10 instruction cycles
```

| OP12 3 | 2 | 1 | 0 | $V_{REF}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0.31 |
| 0 | 0 | 0 | 1 | 0.62 |
| 0 | 0 | 1 | 0 | 0.94 |
| 0 | 0 | 1 | 1 | 1.25 |
| 0 | 1 | 0 | 0 | 1.56 |
| 0 | 1 | 0 | 1 | 1.87 |
| 0 | 1 | 1 | 0 | 2.19 |
| 0 | 1 | 1 | 1 | 2.50 |
| 1 | 0 | 0 | 0 | 2.81 |
| 1 | 0 | 0 | 1 | 3.12 |
| 1 | 0 | 1 | 0 | 3.44 |
| 1 | 0 | 1 | 1 | 3.75 |
| 1 | 1 | 0 | 0 | 4.06 |
| 1 | 1 | 0 | 1 | 4.37 |
| 1 | 1 | 1 | 0 | 4.69 |
| 1 | 1 | 1 | 1 | 5.00 |

Table 2-2. Reference Voltage at $V_{DD}$ = 5V

## 2.3 D/A converter (PWM) output

The 47C231A have one channels of built-in pulse width modulation ($\overline{PWM}$) outputs. D/A converter output can easily be obtained by connecting an external low pass filter. $\overline{PWM}$ outputs data are multiplex to the R73 pin. It is R73 pin common to $\overline{PWM}$ output and R73 output. The R73 output latch should be set to "1" when $\overline{PWM}$ is used as an output port. $\overline{PWM}$ output is controlled by the buffer selector (OP17) and the data transfer buffer (OP18).

### 2.3.1 Configuration of circuit

Configuration of pulse width modulation circuit shown is Figure 2-3.

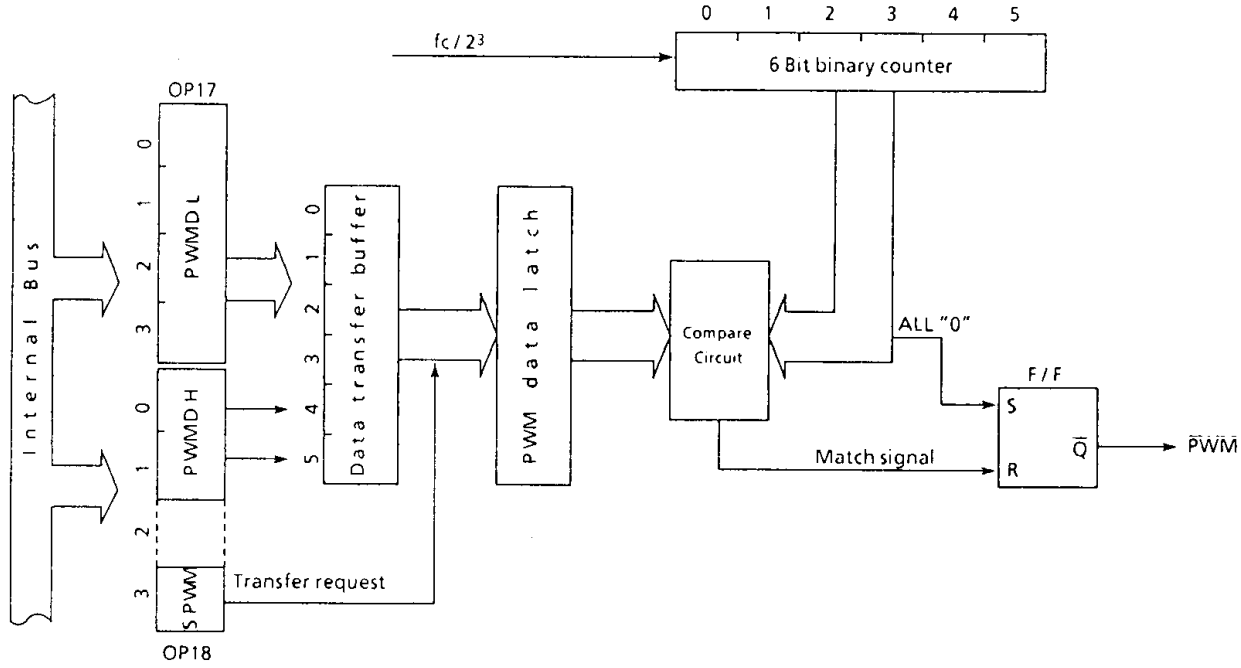



Figure 2-3. PWM output circuit

### 2.3.2 Output waveform of PWM circuit

It is a PWM output controled by 6 bits data. The period of them is $T_N = 2^9/fc$ or 128μs at 4 MHz clock.

The 6 bits of transfer PWM data latch are used to control the pulse width of the pulse output with the period of $T_N$.

When the 6 bits data are decimal n ($0<n<63$), the low level pulse width becomes n x to (to $= 2^3/fc$)

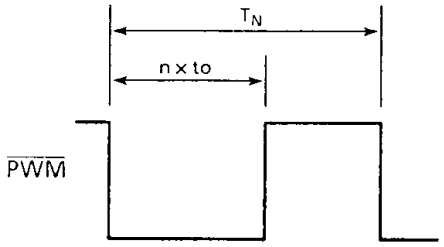



Figure 2-4. $\overline{PWM}$ output waveform

### 2.3.3 Control of PWM output circuit

PWM data are loaded to the data transfer buffers (the lower 2 bits of OP17 and OP18). By loading to SPWM (bit 3 of OP18), these PWM data can be transferred to the PWM data latch for switching to $\overline{PWM}$ output.

SPWM is automatically cleared when the data are transferred. A maximum of $2^9/fc$ [sec] is required from SPWM loading to $\overline{PWM}$ output. The PWM data latch holds these data until another transfer request is received.

Also, the OP17, OP18 and the PWM data latch are cleared to "0" during reset and hold ($\overline{PWM}$ output is "H" level).

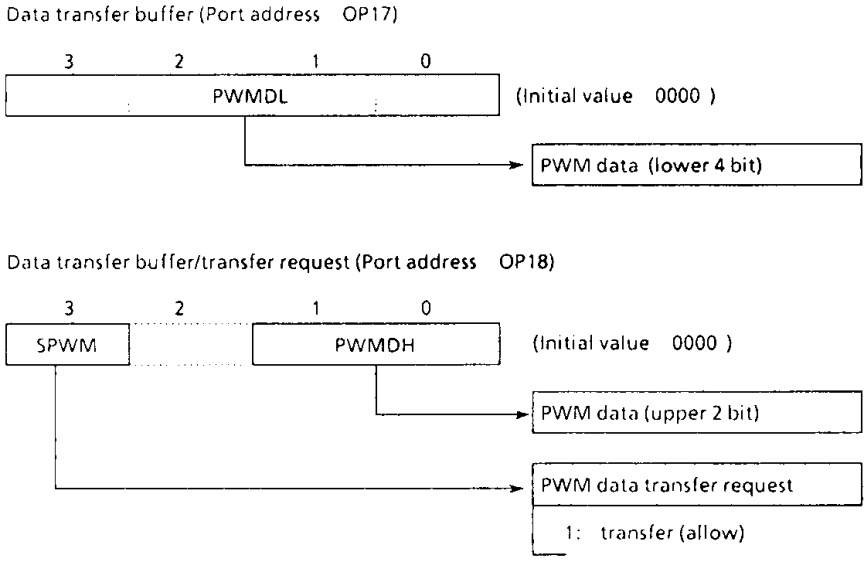



Figure 2-5. Command Register

Example: Sets the PWM data latch (OP17←RAM [$10_H$, $11_H$] )

```
LD      HL, #10H      ; OP17←RAM [10H] (Sets lower 4-bit data of PWM data)
OUT     @HL, %OP17
INC     L
LD      A, @HL
OR      A, #1000B     ; SPWM←1
OUT     A, %OP18      ; OP18←Acc (Sets upper 2-bit data of PWM data)
```

## 2.4 Remote Control Pre-processor

The remote control pre-processor counts the edge-to-edge time of the input pulse and generates an interrupt request each time that the switching edge of an input pulse is detected. Remote control signal waveform which has been rectified by the receiver is inputed to the R80 ($\overline{INT2}$) pin.

### 2.4.1 Circuit Configuration

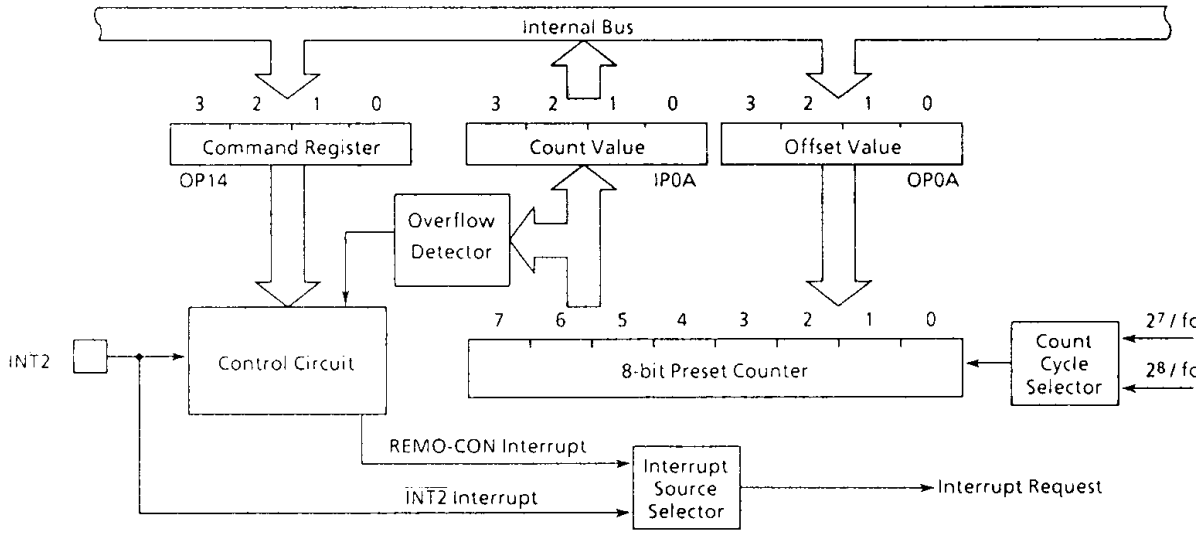



Figure 2-6. Remote Control Pre-processor

## 2.4.2 Control of Remote Control Pre-processor

The remote control pre-processor is controlled by the command register (OP0E). Also, external interrupt 2 is used to interrupt source. At reset, $\overline{INT2}$ is selected, so a remote control discrimination (REMO-CON) interrupt is selected by command. Interrupt enable master F/F (EIF) and interrupt enable register (EIR) are used to enable/disable remote control discrimination interrupt. The interrupt priority is the same as for external interrupt 2.

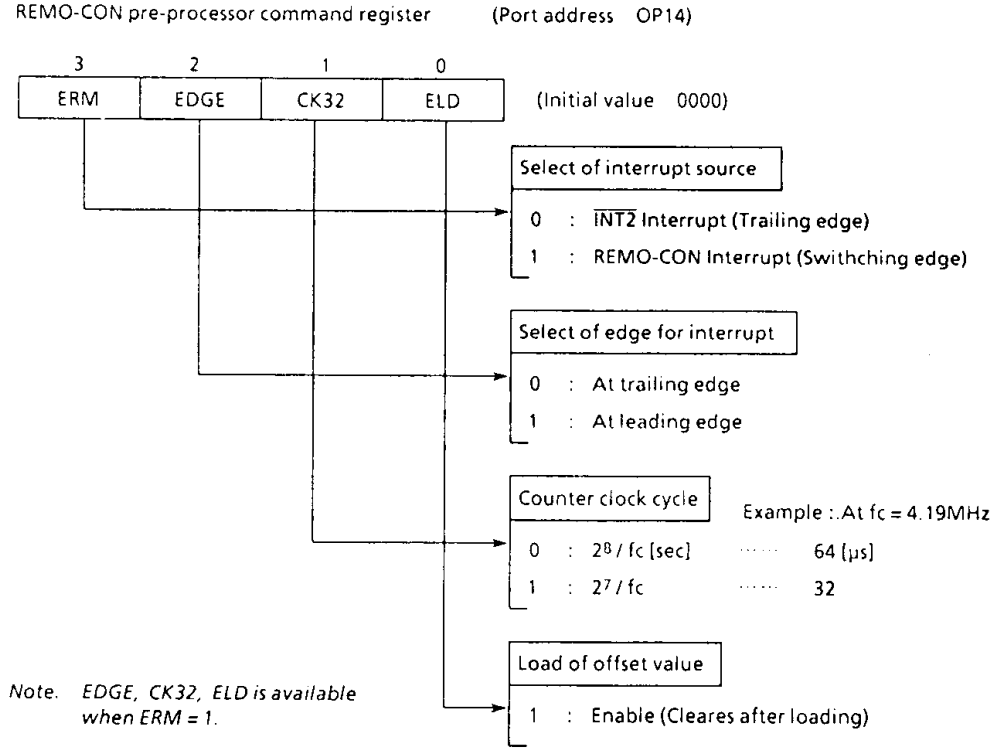



Figure 2-7. Command Register

(1) 8-bit preset counter

This is a binary counter which counts the time from edge to next edge. A value of offset value register (OP0A) are loaded to the lower 4 bits and the value of the upper 4 bits are stored to the count value register (IP0A).

Offset value is loaded in the following cases :

① When ELD (bit 0 of the OP14) is set to "1".
② When there is an overflow of the lower 4 bits.
③ When an edge is detected.

Count value is stored in the following cases :

① When the upper 4 bits are all "1".
② When an edge is detected.

(2) Reference time and detection time

The reference time must be created before measuring the pulse width of the remote control signal waveform. Reference time is set the value shown in Table 2-3 by the count cycle of the preset counter selected with the OP14 and the offset value set to the OP0A. Therefore, the product of the reference time and the count value read from the IP0A becomes the detecion time.
However, the worst error of the detection time is equivalent to reference time.

| Count clock cycle | Offset value (HEX) | Reference time (n = 0 - 15) |
|---|---|---|
| $2^7$ / fc [sec] | 0 to F | $(2^{11} - n \times 2^7)$ / fc [sec] |
| $2^8$ / fc [sec] | 0 to F | $(2^{12} - n \times 2^8)$ / fc [sec] |

Table 2-3. Set value of reference time

(3) Remote control pre-processing operation

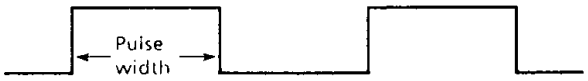
First, set the offset value for creating the reference time to the OP0A. The offset value is loaded to the lower 4 bits of preset counter by setting ELD to "1". ERM can also be set to "1" at the same time. Setting ERM starts counting. ELD is cleared after loading but it is automatically loaded during the count by an overflow of the lower 4 bits.

After storing the count value in the IP0A by detecting the switching edge (leading/trailing) of the input pulse, the preset counter again loads the offset value to the lower 4 bits, clears to "0" the upper 4 bits and restarts counting. An interrupt request is genarated at this time. Therefore, read the count value in the interrupt service routine. The next interrupt is disabled until the stored count value is read. Switching edges can select in one by one using EDGE.

If the upper 4 bits of counter becomes "$1111_B$" before the next edge is accepted, it is judged to be an overflow and the interrupt is generated. In this case, IP0A is set to "$F_H$" and it can be identified to be the overflow interruption. The input pulse width of both "H" and "L" levels must be more than 192/fc [sec]. If any shorter pulse than 192/fc [sec] may be expected, put the dummy instruction [IN %IP0A, A] reading out from count value register in the main routine.

Even if ERM is "0", when an INT2 interrupt sourse is enabled (determined by EIF,EIR), an interrupt request is generated by a falling edge of input pulse. Figure 2-8 shows the operation timing.

Example: To store a count value to RAM [$10_H$] that pulse width of input pulse is measured.




```
Main routine
        OUT     #5, %OP0A       ; Offset value register set to "5".
        LD      A, 1111B        ; Interrupt enable with setting count cycle to 32 µsec,
        OUT     A, %OP14          leading edge detection mode.
        CLR     0, 0            ; Clear to RAM [00H]0 as interrupt status flog.
        LD      A, #0001B       ; Interrupt enable
        XCH     A, EIR
        EICLR   IL, #111110B
        :
INT2 service routine
        TEST    0, 0            ; Skip, if interrupt status flag is "0".
        B       ST0
        LD      HL, #10H        ; HL ← 10H
        IN      %IP0A, @HL      ; RAM [10H] ← Count value
        CLR     0, 0            ; Clearing interrupt status flag.
        LD      A, 1110B
        OUT     A, %OP14        ; Set to leading edge detection mode.
        B       SEND
ST0:    SET     0, 0            ; Setting interrupt status flag.
        LD      A, 1010B
        OUT     A, %OP14        ; Set to trailing edge detection mode.
        IN      %IP0A, A        ; Dummy
SEND:
```

※ Calculation of pulse width with the avobe program when the count value stored to the RAM [$10_H$] is "9". When the clock frequency is 32μs (fc = 4.19MHz) and the offset value is "5", the reference time will be as follows :

$$(2^{11} - 5 \times 2^4) / fc = 336\ [\mu s]$$

Thus, the detection time (pulse width) will be 336 x 9 = 3.02[ms] (including an error of 336μs max.)

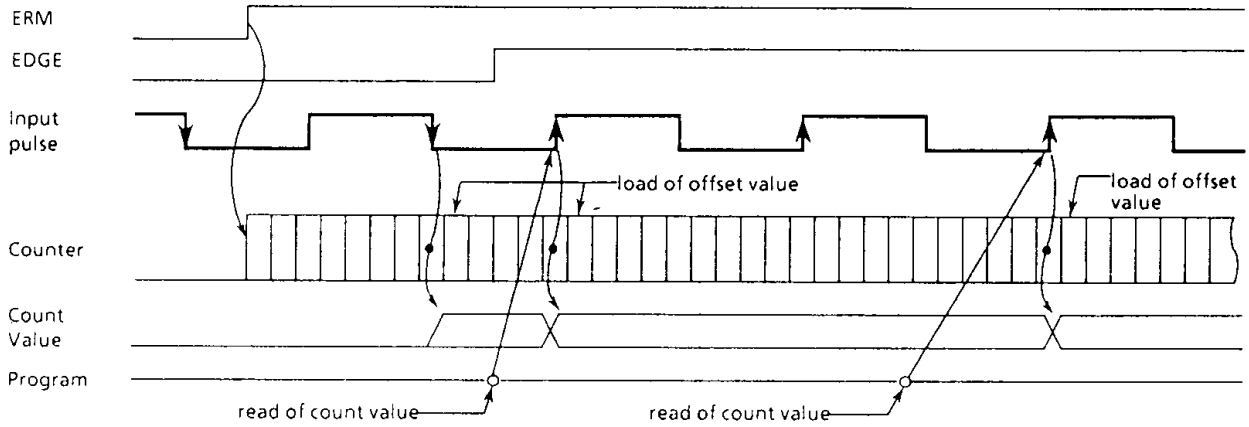



Figure 2-8. · Timing chart

## 2.5 Serial Interface (SIO)

The 47C231A contains a serial interface with an 8-bit buffer. The serial interface is connected to the exterenal device via 3 pins (the serial port): R92 ($\overline{SCK}$), R91 (SO), and R90 (SI). The serial port is shared by port R9. For the serial port, the output latch of port R9 must be set to "1". In the transmit mode, R90 pin provides the I/O port; in the receive mode, R91 pin provides the I/O port.

### 2.5.1 Configuration of Serial Interface

Figure 2-9 shows configuration of serial interface.

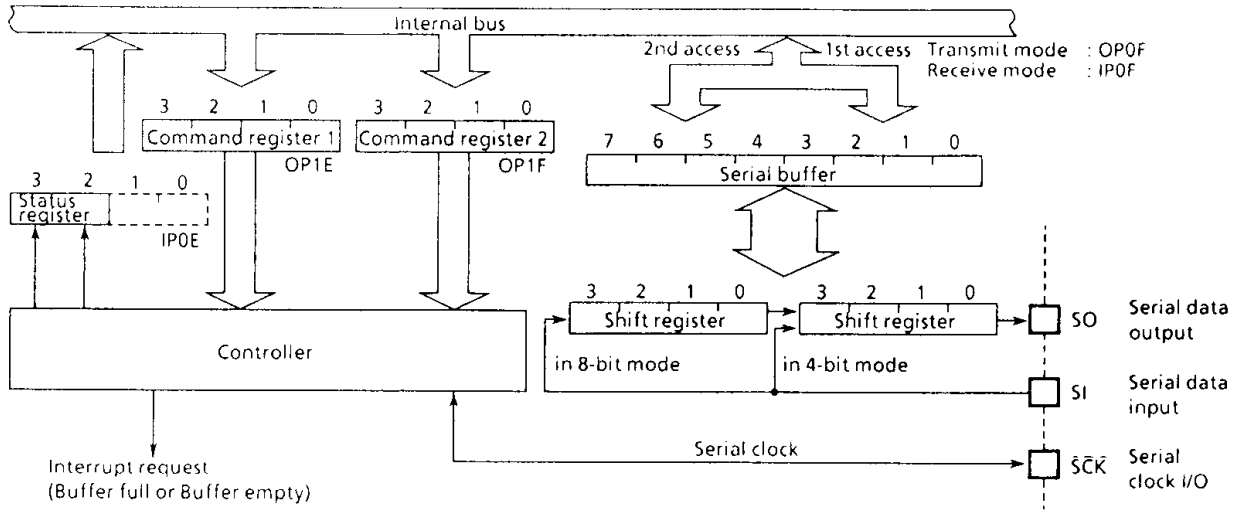



Figure 2-9. Configuration of Serial Interface

## 2.5.2 Control of Serial Interface

The serial interface is controlled by command registers (OP1E, OP1F). The operating states of the serial interface can monitor by the status register (IP0E).

The command register 1 is initialized to "1" and the command register 2 is initialized to "0" during reset.

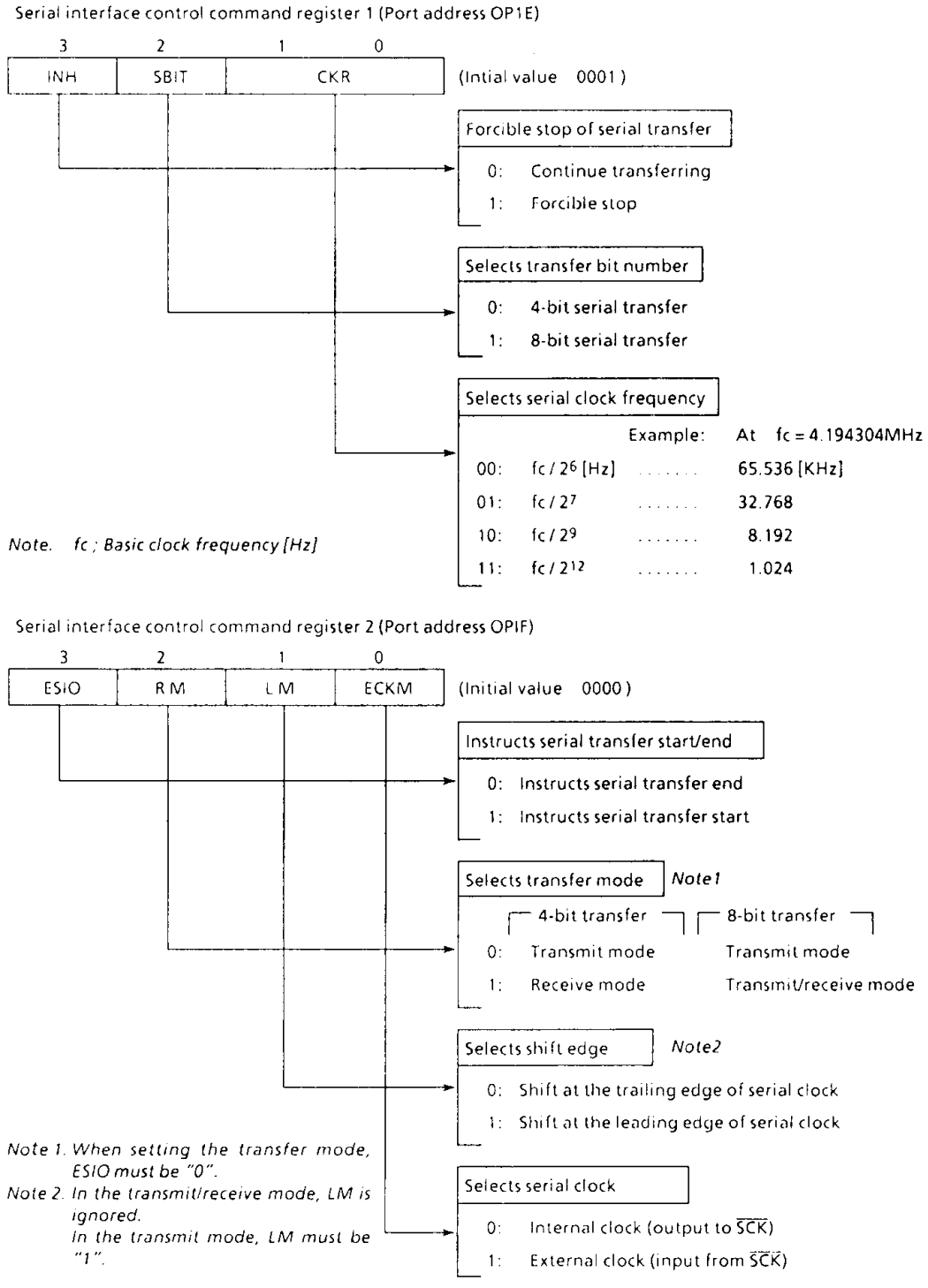



Figure 2-10. Serial Interface Control Command Register

Serial Interface Status Register (port address IP0E)

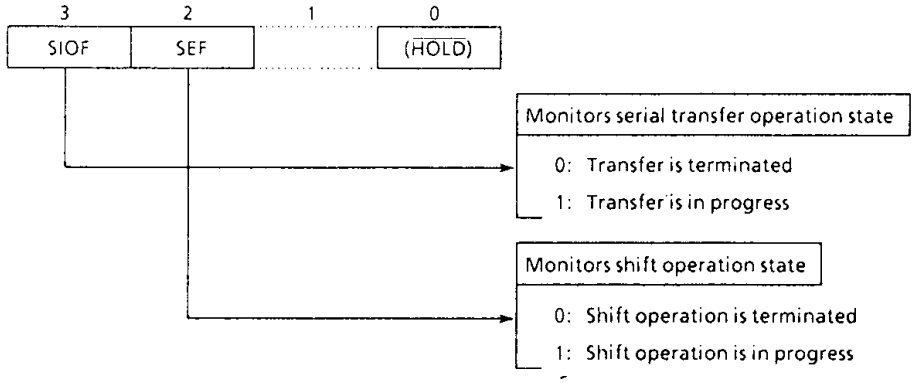



Figure 2-11. Serial Interface Status Register

(1) Serial clock

For the serial clock, one of the following can be selected according to the contents of the command register:

a. Clock source selection

① Internal clock

The serial clock frequency is selected by command register. The serial clock is output on the $\overline{SCK}$ pin. This device provides the wait function in which the shift is not occurred until these processings are completed.

The highest transfer rate based on the internal clock is 62500 bits/second (at fc = 4 MHz).

② External clock

The signal obtained by the clock supplied to the $\overline{SCK}$ pin from the outside is used for the serial clock. In this case, the output latch of R92 ($\overline{SCK}$) must be set to "1" beforehand. For the shift operation to be performed correctly, each of the serial clock's high and low levels needs 2 instruction cycles or more to be completed.

b. Shift edge selection

① Leading edge

Date is shifted at the leading edge (the falling edge of $\overline{SCK}$ pin input) of the serial clock.

② Trailing edge

Data is shifted at the trailing edge (the rising edge of $\overline{SCK}$ pin input) of the serial clock. However, in the transmit mode, the trailing-edge shift is not supported.

(2) Transfer bit number

SBIT (bit 2 of the command register 1) can select 4-bit/8-bit serial transfer.

a. 4-bit serial transfer

In this mode, transmission/reception is performed on 4-bit basis. ISIO interrupt is generated every 4-bit transfer. Transmit/receive data is written/read by accessing the buffer register (OP0F/IP0F).

b. 8-bit serial transfer

In this mode, transmission/reception is performed on 8-bit basis. ISIO interrupt is generated every 8-bit transfer.

Transmit/receive data is written/read by accessing the buffer register (OP0F/IP0F) twice. At the first access after setting transfer mode or generating the interrupt request, the write/read operation of lower 4-bit is performed to from the buffer register. At the second access, that of upper 4-bit is performed.

(3) Transfer modes

Selection between the transmit mode, the receive mode and the transmit/receive mode is performed by RM (bit 2 of the command register).

This section describes about the 8-bit transfer mode.

a. 8-bit transmit mode

The transmit mode is set to the command register then writes the first transmit data (4 bits or 8 bits) to the buffer register (OP0F). If the transmit mode is not set, the data is not written to the buffer register.

In the 8-bit transfer mode, the 8-bit data is written by accessing the buffer register (OP0F) twice. The transmit data is written after the 8-bit transfer mode is set or an interrupt request occurs: the lower 4 bits are written by the first access and the upper 4 bits by the next access.

Then, setting ESIO to "1" starts transmission. The transmit data is output to the SO pin in synchronization with the serial clock from the LSB side sequentially. When the LSB is output, the transmit data is moved from the buffer register to the shift register. When the buffer register becomes empty,the buffer empty interrupt (ISIO) to request for the next transmit data is generated. In the interrupt service program, when the next transmit data is written to the buffer register, the interrupt request is reset.

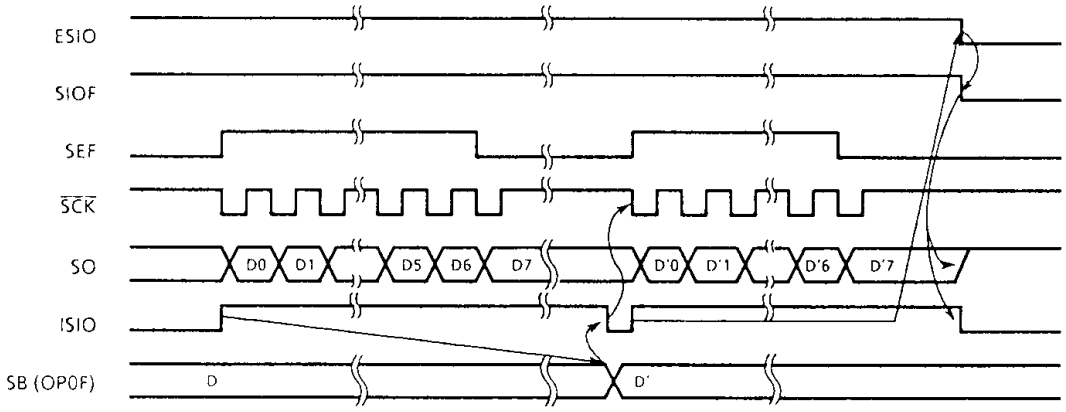
In the operation based on the internal clock, if no more data is set after the transmission of the 8-bit data, the serial clock is stopped and the wait state sets in. In the operation based on the external clock, the data must be set in the buffer register by the time the next data shift operation starts.

Therefore, the transfer rate is determined by the maximum delay time between the occurrence of the interrupt request and the writing of data to the buffer register by the interrupt serviced program.

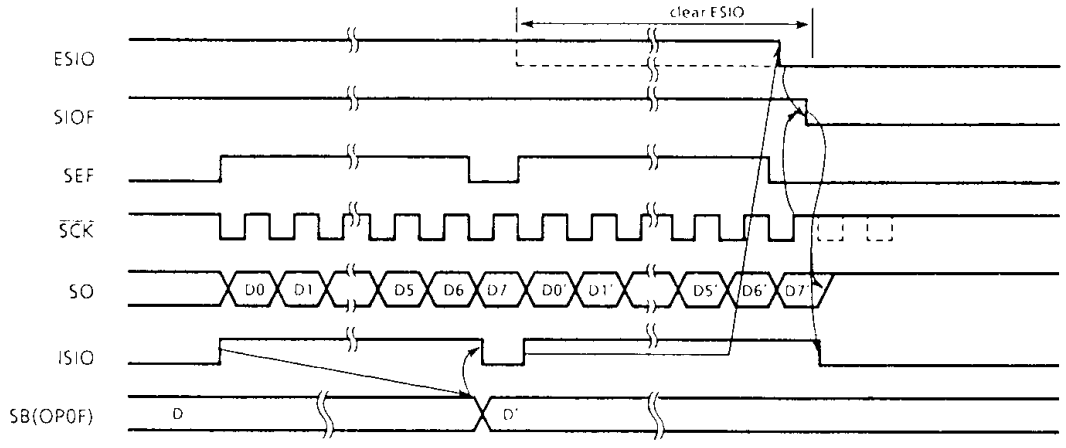
To end transmission, ESIO is cleared to "0" instead of writing the next transmit data by the buffer empty interrupt service program. When ESIO is cleared,transmission stops upon termination of the currently shifted-out data.

The transmission end can be known by the SIOF state (SIOF goes "0" upon transmission end). In the operation based on the external clock, ESIO must be cleared to "0" before the next data is shifted out. If ESIO is not cleared before, the transmission stops upon sending the next 8-bit data (dummy).

```
Example :   8-bit transmit mode set up (on the internal clock)
    LD      A, #0100B       ;  OP1E←0100B
    OUT     A, %OP1E           (Sets the 8-bit transfer and serial clock frequency)
    LD      A, #0010B       ;  OP1F←0010B (Sets the transmit mode)
    OUT     A, %OP1F
    LD      HL, #SODAT
    OUT     @HL, %OP0F      ;  OP0F←RAM [HL] (Writes lower 4-bit data to be transmitted)
    INC     L
    OUT     @HL, %OP0F      ;  OP0F←RAM [HL] (Writes Upper 4-bit data to be transmitted)
    LD      A, #1010B       ;  ESIO←1 (Instructs serial transfer start)
    OUT     A, %OP1F
     :
```




(a) Internal-clock-based operation with wait




(b) External-clock-based operation

Figure 2-12. 8-bit transmit mode

b. 8-bit simultaneous transmit/receive mode

After the command register is set to the simultaneous transmit/receive mode, the first data to be transmited written to the buffer register. After that, simultaneous transmit/receive mode is enabled by setting ESIO to "1". The data being transmitted are output from the SO pin on the leading edge of the serial clock and the data being received are input at the SI pin on the trailing edge. The 8-bit data received are transferred from the shift register to the buffer register (IP0F) and an ISIO (buffer full) interrupt is generated requesting readout of the data. The interrupt service program reads the data from the buffer register and then writes data to be transmitted. The lower 4-bits are accessed the first time the buffer register is read/written after an interrupt request is generated or the transmit/receive mode is set; the next time the buffer register is read or written, the upper 4-bits are accessed.

In the operation based on the internal clock, SIO becomes the wait state until the received data are read out and the next data to be transmitted are written.

In the operation based on the external clock, the shift operation is synchronized with the external clock; therefore, it is necessary to read the data received and to write data to be sent next before starting the next shift operation.

The maximum transfer rate using an external clock is determined by the maximum delay time between the generation of the interrupt request and the writing of the data to be transmitted after the reading of the received data.

Also, the buffer register is used for both transmission and reception; therefore, the data being transmitted must be written after reading 8-bits of received data.

This operation is ended by clearing ESIO to "0". When ESIO is cleared, this operation is ended after transfer of the current 8-bits of data to the buffer register is completed. Programs can confirm that the operation has been completed by sensing SIOF (bit 3 of the status register) because SIOF is cleared to "0" when the operation is completed.

Example : 8-bit simultaneous transmit/receive mode set up (on the external clock)

```
LD      A, #0100B       ; OP1E←0100B
OUT     A, %OP1E          (Sets the 8-bit transmit/receive and serial clock
                          frequency)
LD      A, #0111B       ; OP1F←01*1B (Sets the transmit/receive mode of
                          external clock operation)
OUT     A, %OP1F
LD      HL, #SODAT      ; OP0F←RAM [HL] (Writes lower 4-bit data to be
                          transmitted)
OUT     @HL, %OP0F
INC     L               ; OP0F←RAM [HL] (Writes Upper 4-bit data to be
                          transmitted)
OUT     @HL, %OP0F
LD      A, #1111B       ; ESIO←1 (Instructs serial transfer start)
OUT     A, %OP1F
```

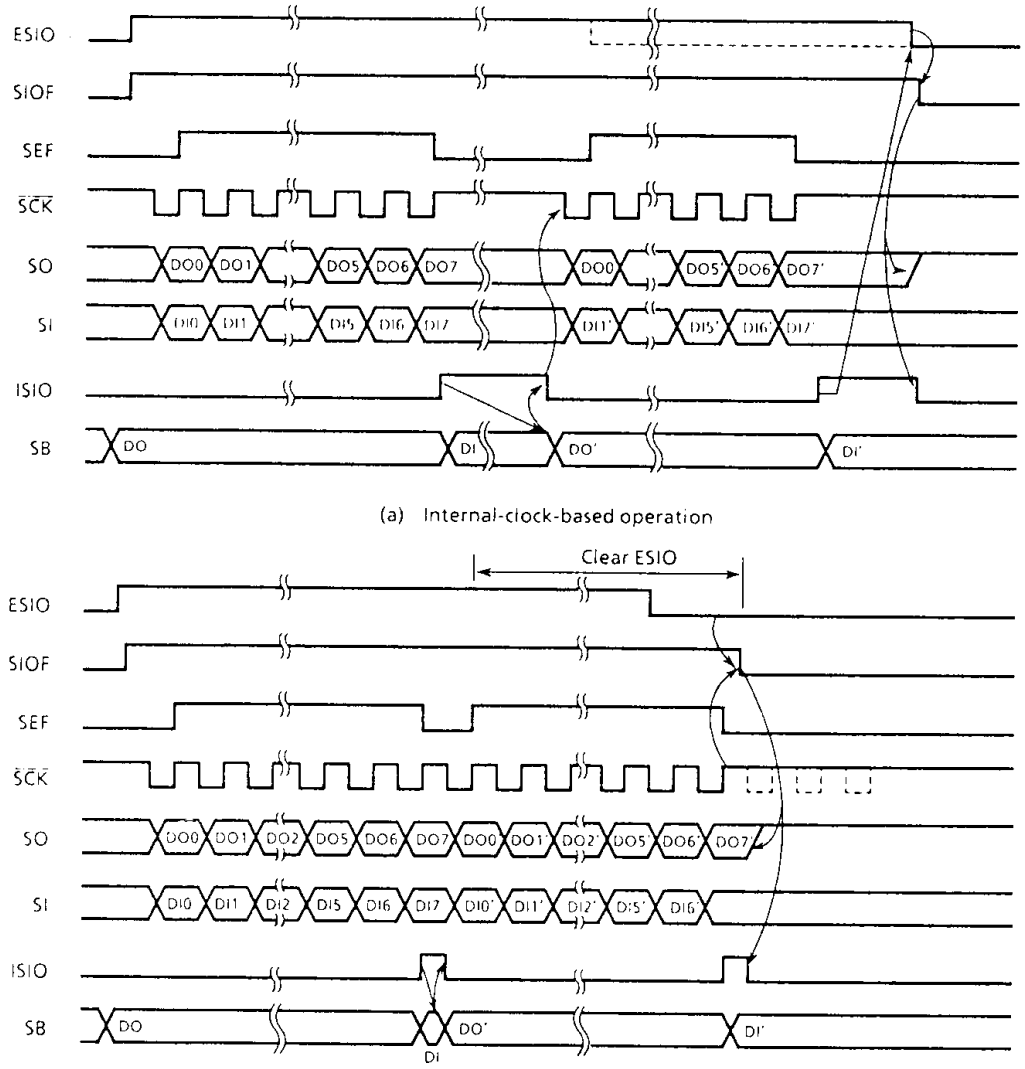



Figure 2-13. 8-bit Transmit / Receive Mode

(3) Stopping serial transfer

A serial transfer operation can be stopped forcibly.

It is stopped by setting INH (bit 3 of command register 1) to "1", clearing the shift counter and ESIO. When the serial transfer is over, INH is automatically cleared to "0" with no other bits of command register affected.

In the transmit mode of this case, SO output is initialized to "H" level whereas the shift register is not cleared. Therefore, after the resumption of transmit, SO holds the data just before forcible stop via the shift register until the 1st shift data comes to SO.

## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS ($V_{SS}$ = 0V)

| PARAMETER | SYMBOL | PINS | RATING | UNIT |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | − 0.3 to 7 | V |
| Input Voltage | $V_{IN}$ | | − 0.3 to $V_{DD}$ + 0.3 | V |
| Output Voltage | $V_{OUT1}$ | Except sink open drain pin, but include R70 pin | − 0.3 to $V_{DD}$ + 0.3 | V |
| | $V_{OUT2}$ | Sink open drain pin except R70 pin | − 0.3 to 10 | |
| Outpur Current (Per 1 pin) | $I_{OUT1}$ | Ports R5, R6 | 30 | mA |
| | $I_{OUT2}$ | Ports R7, R8, R9 | 3.2 | |
| Output Current (Total) | $\Sigma I_{OUT1}$ | Ports R5, R6 | 120 | mA |
| Power Dissipation [$T_{opr}$ = 70°C] | PD | | 600 | mW |
| Soldering Temperature (time) | $T_{sld}$ | | 260 (10sec) | °C |
| Storage Temperature | $T_{stg}$ | | − 55 to 125 | °C |
| Operating Temperature | $T_{opr}$ | | − 30 to 70 | °C |

### RECOMMENDED OPERATING CONDITIONS ($V_{SS}$ = 0V, $T_{opr}$ = − 30 to 70°C)

| PARAMETER | SYMBOL | PINS | CONDITION | Min. | Max. | UNIT |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | in the Normal mode | 4.5 | 6.0 | V |
| | | | in the HOLD mode | 2.0 | | |
| Input High Voltage | $V_{IH1}$ | Except Hysteresis Input | $V_{DD} \geqq 4.5V$ | $V_{DD} \times 0.7$ | $V_{DD}$ | V |
| | $V_{IH2}$ | Hysteresis Input | | $V_{DD} \times 0.75$ | | |
| | $V_{IH3}$ | | $V_{DD} < 4.5V$ | $V_{DD} \times 0.9$ | | |
| Input Low Voltage | $V_{IL1}$ | Except Hysteresis Input | $V_{DD} \geqq 4.5V$ | 0 | $V_{DD} \times 0.3$ | V |
| | $V_{IL2}$ | Hysteresis Input | | | $V_{DD} \times 0.25$ | |
| | $V_{IL3}$ | | $V_{DD} < 4.5V$ | | $V_{DD} \times 0.1$ | |
| Clock Frequency | fc | | | 0.4 | 4.2 | MHz |

*Note . Input Voltage $V_{IH3}$, $V_{IL3}$ : In the HOLD mode.*

## D.C. CHARACTERISTICS

($V_{SS}$ = 0V, $T_{opr}$ = − 30 to 70°C)

| PARAMETER | SYMBOL | PINS | CONDITIONS | Min. | Typ. | Max. | UNIT |
|---|---|---|---|---|---|---|---|
| Hysteresis Voltage | $V_{HS}$ | Hysteresis Input | | − | 0.7 | − | V |
| Input Current | $I_{IN1}$ | Port CIN, TEST, $\overline{RESET}$, $\overline{HOLD}$ | $V_{DD}$ = 5.5V, $V_{IN}$ = 5.5V / 0V | − | − | ± 2 | μA |
| | $I_{IN2}$ | Port R (open drain) | | | | | |
| Input Low Current | $I_{IL}$ | Port R (push-pull) | $V_{DD}$ = 5.5V, $V_{IN}$ = 0.4V | − | − | − 2 | mA |
| Input Resistance | $R_{IN1}$ | Port CIN with pull up/pull down | | 30 | 70 | 150 | KΩ |
| | $R_{IN2}$ | $\overline{RESET}$ | | 100 | 220 | 450 | |
| Output Leakage Current | $I_{LO}$ | Port R (open drain) | $V_{DD}$ = 5.5V, $V_{OUT}$ = 5.5V | − | − | 2 | μA |
| Output High Voltage | $V_{OH}$ | Port R (push-pull) | $V_{DD}$ = 4.5V, $I_{OH}$ = − 200μA | 2.4 | − | − | V |
| Output Low Voltage | $V_{OL2}$ | XOUT, Port R (except ports R5, R6) | $V_{DD}$ = 4.5V, $I_{OL}$ = 1.6mA | − | − | 0.4 | V |
| Output Low Current | $I_{OL1}$ | Ports R5, R6 | $V_{DD}$ = 4.5V, $V_{OL}$ = 1.0V | − | 20 | − | mA |
| Supply Current (in the Normal mode) | $I_{DD}$ | | VDD = 5.5V, fc = 4MHz | − | 3 | 6 | mA |
| Supply Current (in the HOLD mode) | $I_{DDH}$ | | $V_{DD}$ = 5.5V | − | 0.5 | 10 | μA |

*Note 1. Typ. values show those at $T_{opr}$ = 25°C, $V_{DD}$ = 5V.*

*Note 2. Input Current $I_{IN1}$ : The current through resistor is not included, when the pull-up/pull-down resistor is contained.*

*Note 3. Supply Current : $V_{IN}$ = 5.3V / 0.2V*
*The CIN port is open when the pull-up/pull-down resistor is contained.*
*The voltage applied to the R port is within the valid range $V_{IL}$ or $V_{IH}$.*

## A / D CONVERTER CHARACTERISTICS

($V_{SS}$ = 0V, $V_{DD}$ = 4.5 to 6.0V, $T_{opr}$ = − 30 to 70°C)

| PARAMETER | SYMBOL | CONDITION | Min. | Typ. | Max. | UNIT |
|---|---|---|---|---|---|---|
| Analog input voltage | $V_{AIN}$ | CIN4 to CIN0 | $V_{SS}$ | − | $V_{DD}$ | V |
| A/D conversion error | − | | − | − | $\pm\frac{1}{2}$ | LSB |

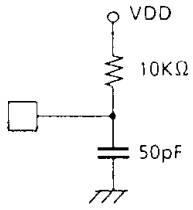
## A.C. CHARACTERISTICS

($V_{SS}$ = 0V, $V_{DD}$ = 4.5 to 6.0V, $T_{opr}$ = – 30 to 70°C)

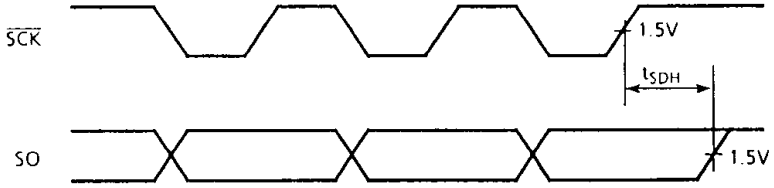
| PARAMETER | SYMBOL | CONDITIONS | Min. | Typ. | Max. | UNIT |
|---|---|---|---|---|---|---|
| Instruction Cycle Time | $t_{cy}$ | | 1.9 | – | 20 | μs |
| High Level Clock Pulse Width | $t_{WCH}$ | For external clock operation | 80 | – | – | ns |
| Low Level Clock Pulse Width | $t_{WCL}$ | | | | | |
| Shift data Hold Time | $t_{SDH}$ | | $0.5t_{cy}$ – 300 | – | – | ns |

*Note . Shift data Hold Time:*

External circuit fot $\overline{SCK}$ pin and SO pin




Serial port (Completion of transmission)




## RECOMMENDED OSCILLATING CONDITIONS

($V_{SS}$ = 0V, $V_{DD}$ = 4.5 to 6.0V, $T_{opr}$ = – 30 to 70°C)

(1) 4MHz

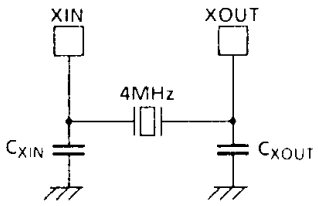
Ceramic Resonator

CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF

KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF

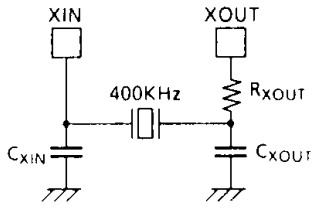



(2) 400KHz

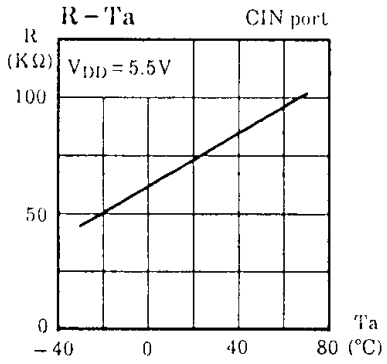
Ceramic Resonator

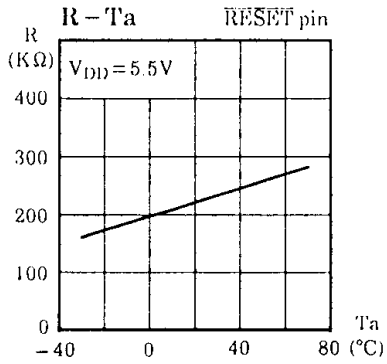
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, $R_{XOUT}$ = 6.8KΩ

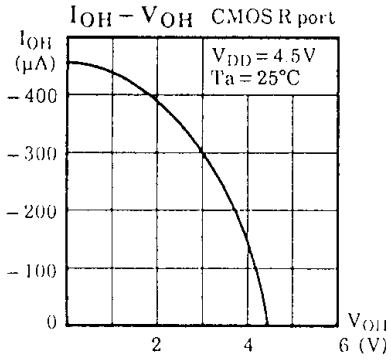
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, $R_{XOUT}$ = 10KΩ

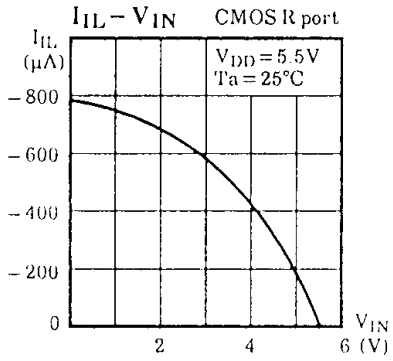


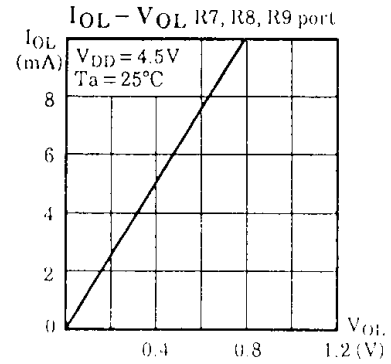
## TYPICAL CHARACTERISTICS

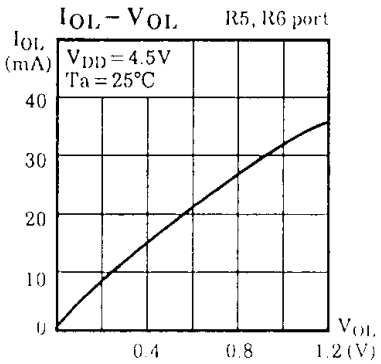


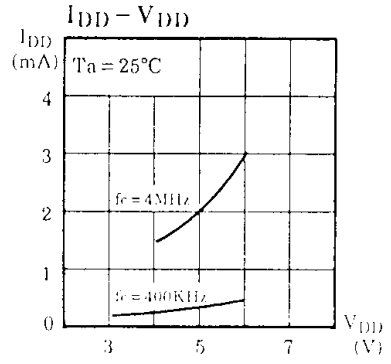



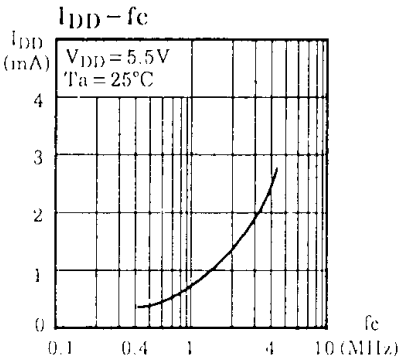



## INPUT/OUTPUT CIRCUITRY

(1) Control pins

Input/Output circuitries of the 47C231A control pins are similar to those of the 47C200A.

(2) I/O ports

The input/output circuitries of the 47C231A I/O ports are shown as belows, any one of the circuitries can be chosen by a code (PD to PF, PL) as a mask option.

| PORT | I/O | INPUT/OUTPUT CIRCUITRY and CODE | REMARK |
|---|---|---|---|
| K0 | Input | PD: R, $V_{REF}$ / PE: VDD, $R_{IN}$, R, $V_{REF}$ / PF, PL: R, $R_{IN}$, $V_{REF}$ | Comparator input<br>Pull-up or pull-down resistor<br>$R_{IN}$ = 70KΩ (typ.)<br>R = 1KΩ (typ.) |
| R5<br>R6 | I/O | PD, PE, PF: Initial "Hi-Z", R / PL: Initial "Low", $V_{DD}$, R | Sink open drain<br>or<br>Push-pull output<br>R = 1KΩ (typ.) |
| R7 | I/O | R70: R, $V_{REF}$ / R71-R73: R | Sink open drain<br>Initial "Hi-Z"<br>Comparator input (R70)<br>R = 1KΩ (typ.) |
| R8 | I/O | R | Sink open drain<br>Initial "Hi-Z"<br>Hysteresis input<br>R = 1KΩ (typ.) |
| R9 | I/O | PD, PE, PF: Initial "Hi-Z", R / PL: Initial "High", VDD, R | Sink open drain<br>or<br>Push-pull output<br>Hysteresis input<br>R = 1KΩ (typ.) |

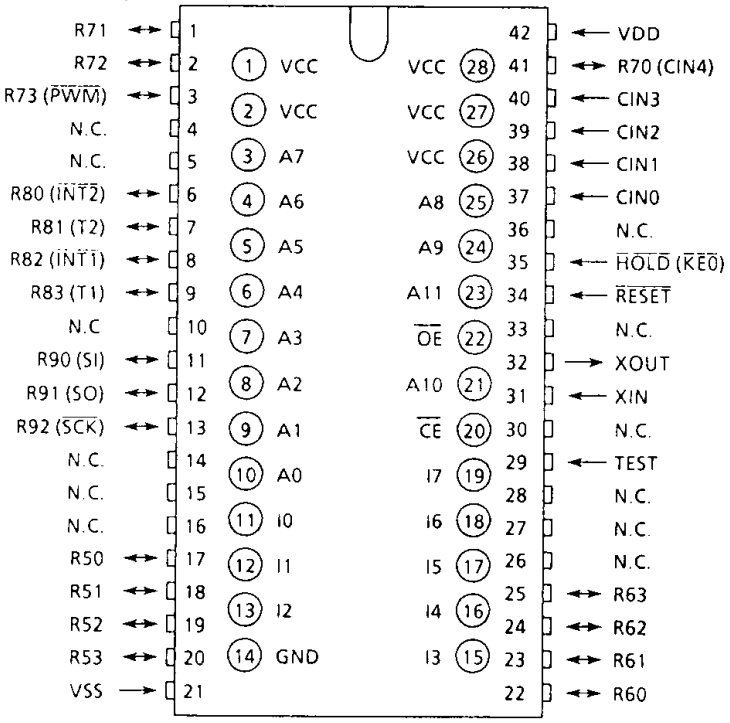
CMOS 4-BIT MICROCONTROLLER

# TMP47C931AE

The 47C931A, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C231A application systems (programs).
The 47C931A has a 42-pin package and can be made pin compatible with the mask ROM 47C231A by using the 42-to -30 pin conversion adapter (BM1103).

## PIN ASSIGNMENT (TOP VIEW)

SDIC42




## PIN FUNCTION (Top of the package)

| PIN NAME | Input / Output | FUNCTIONS |
|---|---|---|
| A11 ~ A0 | Output | Program memory address output |
| I7 ~ I0 | Input | Program memory data input |
| $\overline{CE}$ | Output | Chip enable signal output |
| $\overline{OE}$ | | Output enable signal output |
| VCC | Power supply | + 5V (connected with VDD) |
| GND | | 0V (connected with VSS) |

## A.C. CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | Min. | Typ. | Max. | UNIT |
|---|---|---|---|---|---|---|
| Address Delay Time | $t_{AD}$ | $V_{SS}$ = 0V, $V_{DD}$ = 4.5 to 6.0V | – | – | 150 | ns |
| Data Setup Time | $t_{IS}$ | $C_L$ = 100pF | 150 | – | – | ns |
| Data Hold Time | $t_{IH}$ | Topr = – 30 to 70°C | 50 | – | – | ns |

## NOTES FOR USE

(1) Program memory

The program area depends on the capacity of EPROM. See Figure 1.

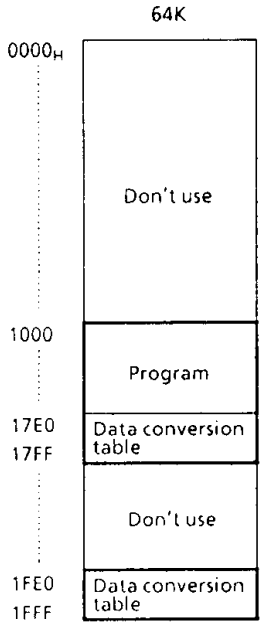



Figure 1. Program area

(2) Data memory

The 47C931A contains 128 x 4-bit data memory.

(3) I/O ports

Input/Output circuitries of I/O ports in the 47C931A are similar to the code PD of the 47C231A. When this chip is used as evaluator with other I/O code, it is necessary to provide the external resistors.


(a) Code : PE (b) Code : PF

Figure 2. I/O code and external circuitry

*Note. Caution is required when using the 47C931A as a code PL evaluator. The following ports of the 47C931A differ from those of the 47C231A (code PL).*

*(1) Ports R5 and R6 are not push-pull output (initial "Low").*

*(2) Port R9 is not push-pull output (initial "High").*