CMOS 4-BIT MICROCONTROLLER

TMP47C200AN, TMP47C400AN
TMP47C200AF, TMP47C400AF

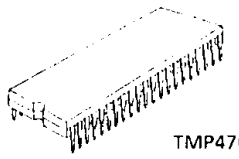
The 47C200A/400A are high speed and high performance 4-bit single chip microcomputers, integrating ROM, RAM, input/output ports, timer/counters, and a serial interface on a chip. The 47C200A/400A are the standard type devices in the TLCS-47 CMOS series, and provides high current output capability for LED direct drive.

PART No.	ROM	RAM	PACKAGE	PIGGYBACK
TMP47C200AN	2048 × 8-bit	128 × 4-bit	SDIP42	TMP47C990E
TMP47C200AF			QFP44	TMP47C990G
TMP47C400AN	4096 × 8-bit	256 × 4-bit	SDIP42	TMP47C990E
TMP47C400AF			QFP44	TMP47C990G

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction execution time: 1.9μs (at 4.2MHz)
- ◆90 basic instructions
- ◆Table look-up instructions
- ◆5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting: 15 levels max.
- ◆6 interrupt sources (External: 2, Internal: 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (36 pins)
  - Input 2ports 5pins
  - Output 2ports 8pins
  - I/O 6ports 23pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Serial Interface with a 4-bit buffer
  External/internal clock, and leading/trailing edge shift mode
- ◆High current outputs
  LED direct drive capability (typ. 20mA × 8 bits)
- ◆Hold function
  Battery/Capacitor back-up
- ◆Real Time Emulator : BM4721A

SDIP42

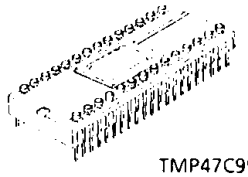


TMP47C200AN
TMP47C400AN

QFP44

TMP47C200AF
TMP47C400AF

SDIC42



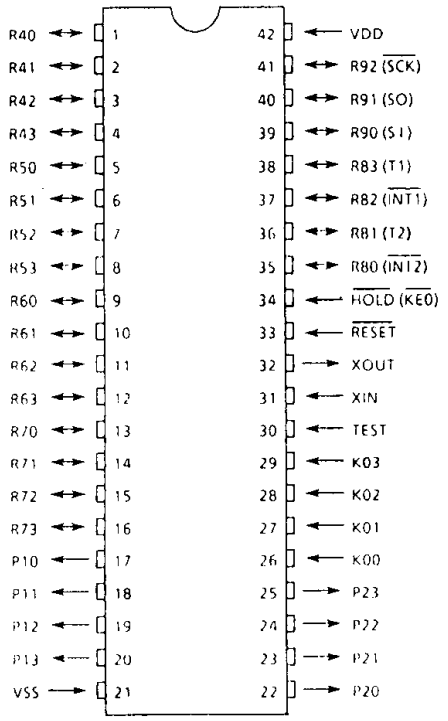
TMP47C990E

QFC44

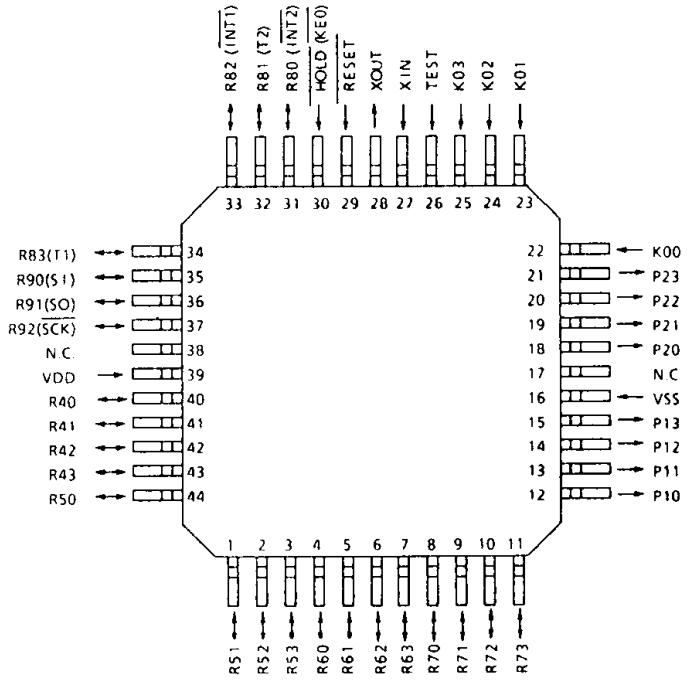
TMP47C990G

PIN ASSIGNMENTS (TOP VIEW)

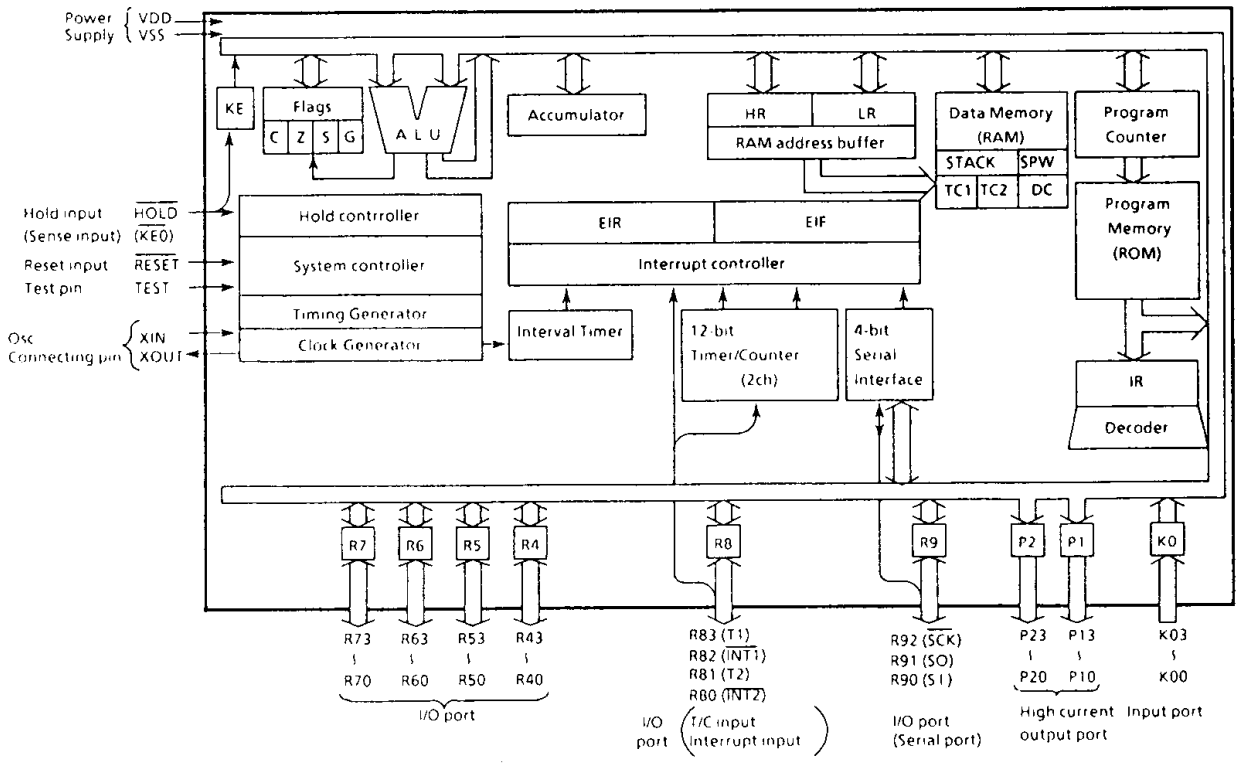
(1) 42-SDIP



(2) 44-QFP



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	Input	4-bit input port	
P13 - P10	Output	4-bit output port with latch. 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @HL].	
P23 - P20			
R43 - R40	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1". Every bit data is possible to be set, cleared and tested by the bit manipulation instruction of the L-register indirect addressing.	
R53 - R50			
R63 - R60			
R73 - R70			
R83 (T1)	I/O(Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 1 input
R92 ($\overline{SCK}$)	I/O(I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O(Output)		Serial data output
R90 (SI)	I/O(Input)		Serial data input
XIN	Input	Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KEO}$)	Input(Input)	Hold request/release signal input	Sense input
TEST	Input	Test pin for shipping. Be opened or fixed to low level.	
VDD	Power Supply	+ 5V	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

1. SYSTEM CONFIGURATION

(1) Program Counter (PC)
(2) Program Memory (ROM)
(3) H Register, L Register
(4) Data Memory (RAM)
  a. Stack
  b. Stack Pointer Word (SPW)
  c. Data Counter (DC)
(5) ALU, Accumulator
(6) Flags
(7) Clock Generator, Timing Generator
(8) I/O Ports
(9) Interval Timer
(10) Timer/Counters (TC1, TC2)
(11) Serial Interface
(12) Interrupt Controller
(13) Hold Controller
(14) Reset Circuit

Concerning the above component parts, the configuration and functions of hardwares are described.

2. INTERNAL CPU FUNCTION

2.1 Program Counter (PC)

The program counter is a 12-bit binary counter which indicates the address of the program memory storing the next instruction to be executed. Normally, the PC is incremented by the number of bytes of the instruction every time it is fetched. When a branch instruction or a subroutine instruction has been executed or an interrupt has been accepted, the specified values listed in Table 2-1 are set to the PC. The PC is initialized to "0" during reset.

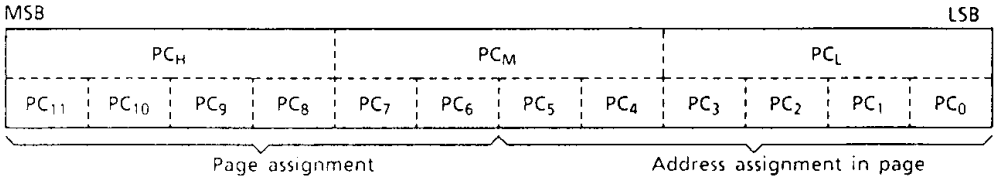


Figure 2-1. Configuration of Program Counter

The PC can directly address a 4096-byte address space. However, with the short branch and subroutine call instructions, the following points must be considered :

(1) Short branch instruction [BSS a]
In [BSS a] instruction execution, when the branch condition is satisfied, the value specified in the instruction is set to the lower 6 bits of the PC. That is, [BSS a] becomes the in-page branch instruction. When [BSS a] is stored at the last address of the page, the upper 6 bits of the PC point the next page, so that branch is made to the next page.

(2) Subroutine call instruction [CALL a]
In [CALL a] instruction execution, the contents of the PC are saved to the stack then the value specified in the instruction is set to the PC. The address which can be specified by the instruction consists of 11 bits and the most significant bit of the PC is always "0". Therefore, the entry address of the subroutine should be within an addrress range of 000_H through $7FF_H$.