

TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TD62783AP, TD62783F, TD62783AF
TD62784AP, TD62784F, TD62784AF**

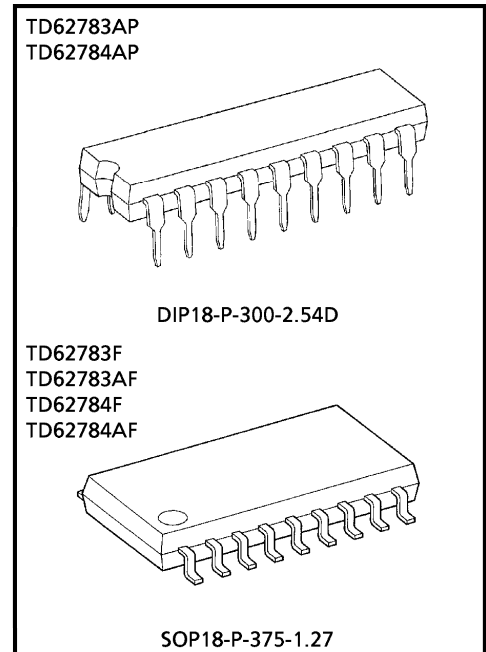
8CH HIGH-VOLTAGE SOURCE DRIVER

The TD62783AP/F/AF Series are comprised of eight source current Transistor Array.
These drivers are specifically designed for fluorescent display applications.
Applications include relay, hammer and lamp drivers.

FEATURES

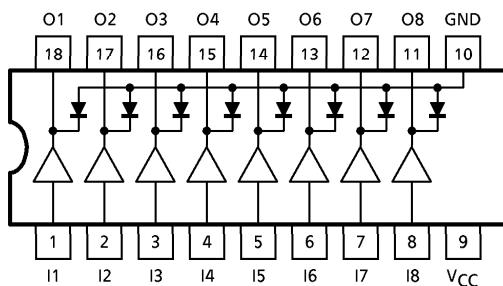
- High output voltage Type-AP, AF : $V_{CC} = 50V$ MIN.
Type-F : $V_{CC} = 35V$ MIN.
- Output current (single output) $I_{OUT} = -500mA$ MIN.
- Output clamp diodes
- Single supply voltage
- Input compatible with various types of logic
- Package Type-AP : DIP-18pin
- Package Type-F, AF : SOP-18pin

TYPE	DESIGNATION
TD62783AP/F/AF	TTL, 5V CMOS
TD62784AP/F/AF	6~15V PMOS, CMOS

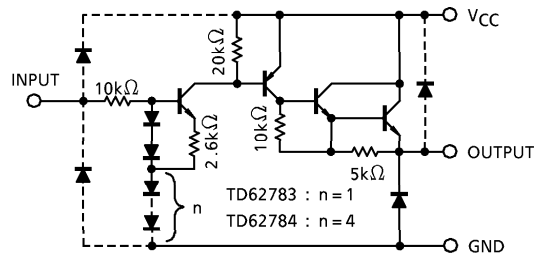


Weight
DIP18-P-300-2.54D : 1.47g (Typ.)
SOP18-P-375-1.27 : 0.41g (Typ.)

PIN CONNECTION (TOP VIEW)



SCHEMATICS (EACH DRIVER)



(Note) The input and output parasitic diodes cannot be used as clamp diodes.

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MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage	AP, AF	V _{CC}	50	V
	F		35	
Output Current		I _{OUT}	- 500	mA / ch
Input Voltage		V _{IN} (Note 1)	15	V
		V _{IN} (Note 2)	30	
Clamp Diode Reverse Voltage	AP, AF	V _R	50	V
	F		35	
Clamp Diode Forward Current		I _F	500	mA
Power Dissipation	AP	P _D (Note 3)	1.47	W
	F, AF		0.96	
Operating Temperature		T _{opr}	- 40~85	°C
Storage Temperature		T _{stg}	- 55~150	°C

(Note 1) Only TD62783AP / F / AF

(Note 2) Only TD62784AP / F / AF

(Note 3) Delated above 25°C in the proportion of 11.7W/°C (AP Type), 7.7W/°C (F, AF Type).

RECOMMENDED OPERATING CONDITIONS (Ta = - 40~85°C)

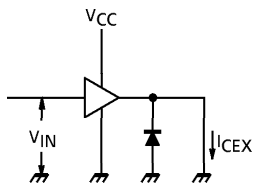
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Supply Voltage	AP, AF	V _{CC}	—	—	—	50	V	
	F		—	—	—	35		
Output Current		I _{OUT}	Ta = 85°C Tj = 120°C T _{pw} = 25ms	Duty = 10% 8 Circuits	—	—	- 260	mA / ch
				Duty = 50% 8 Circuits	—	—	- 59	
	Duty = 10% 8 Circuits			—	—	- 180		
	Duty = 50% 8 Circuits			—	—	- 38		
Input Voltage	TD62783AP / F / AF		V _{IN}	—	—	12	V	
	TD62784AP / F / AF			—	—	24		
Input Voltage	Output On	TD62783AP / F / AF		V _{IN} (ON)	—	2.0	5.0	V
		TD62784AP / F / AF			—	4.5	12.0	
	Output Off	TD62783AP / F / AF		V _{IN} (OFF)	—	0	—	V
		TD62784AP / F / AF			—	0	—	
Clamp Diode Reverse Voltage	AP	V _R	—	—	—	50	V	
	F, AF		—	—	—	35		
Clamp Diode Forward Current		I _F	—	—	—	400	mA	
Power Dissipation	AP	P _D	—	—	—	0.52	W	
	F, AF		—	—	—	0.35		

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

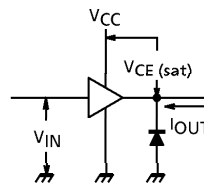
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leakage Current		I _{CEX}	1	V _{CC} = V _{CC} MAX. V _{IN} = 0.4V Ta = 25°C	—	—	100	μA
Output Saturation Voltage		V _{CE} (sat)	2	V _{IN} = V _{IN} (ON), I _{OUT} = - 350mA	—	—	2.0	V
				V _{IN} = V _{IN} (ON), I _{OUT} = - 225mA	—	—	1.9	
				V _{IN} = V _{IN} (ON), I _{OUT} = - 100mA	—	—	1.8	
Input Current	TD62783AP / F / AF	I _{IN} (ON)	3	V _{IN} = 2.4V	—	36	52	μA
				V _{IN} = 3.85V	—	180	260	
	TD62784AP / F / AF			V _{IN} = 5V	—	92	130	
				V _{IN} = 12V	—	790	1130	
Input Voltage	TD62783AP / F / AF	V _{IN} (ON)	4	V _{CE} = 2.0V	—	—	2.0	V
	TD62784AP / F / AF			I _{OUT} = - 350mA	—	—	4.5	
	TD62783AP / F / AF	V _{IN} (OFF)		I _{OUT} = - 500μA	0.8	—	—	
	TD62784AP / F / AF				2.0	—	—	
Supply Current		I _{CC} (ON)	3	V _{IN} = V _{IN} (ON), V _{CC} = 50V	—	—	2.5	mA / ch
Clamp Diode Reverse Current	AP, AF	I _R	5	V _R = 50V	—	—	50	μA
	F			V _R = 35V	—	—	50	
Clamp Diode Forward Voltage		V _F	6	I _F = 350mA	—	—	2.0	V
Turn-On Delay		t _{ON}	7	V _{CC} = V _{CC} MAX. R _L = 125Ω C _L = 15pF, R _L = 88Ω (F)	—	0.15	—	μs
Turn-Off Delay		t _{OFF}			—	1.8	—	

TEST CIRCUIT

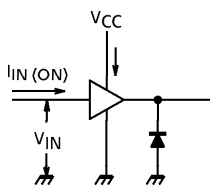
1. I_{CEX}



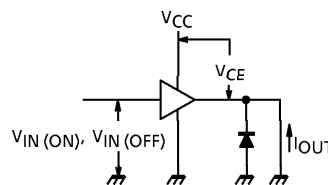
2. $V_{CE(sat)}$



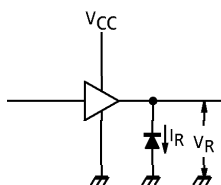
3. $I_{IN(ON)}, I_{CC}$



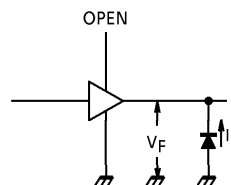
4. $V_{IN(ON)}, V_{IN(OFF)}$



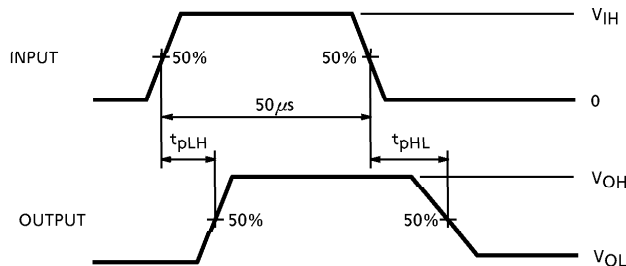
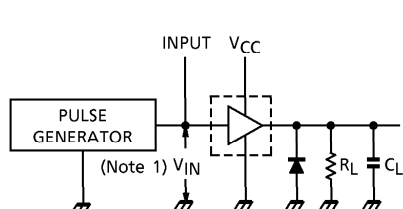
5. I_R



6. V_F



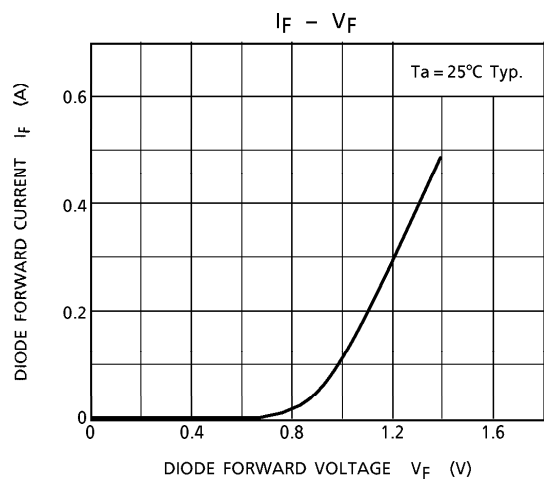
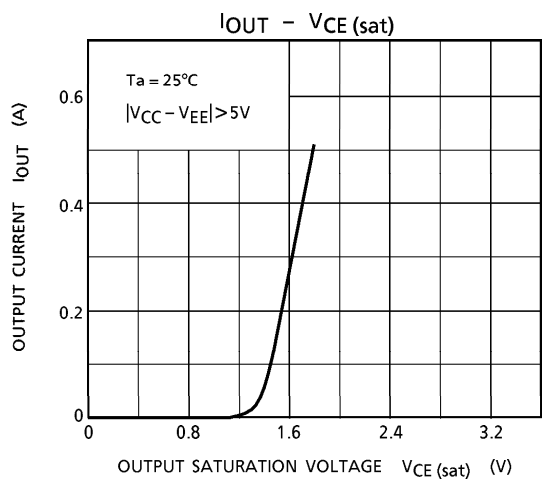
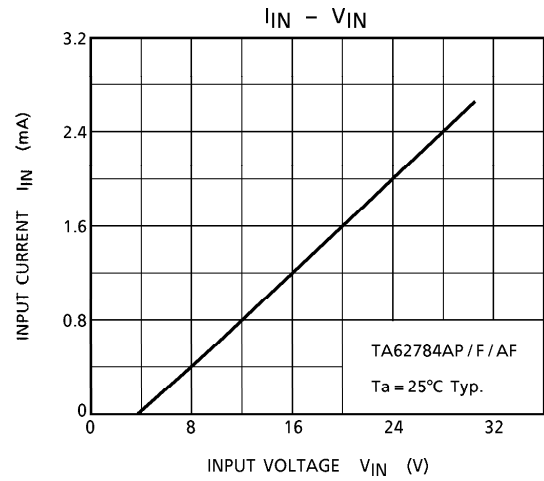
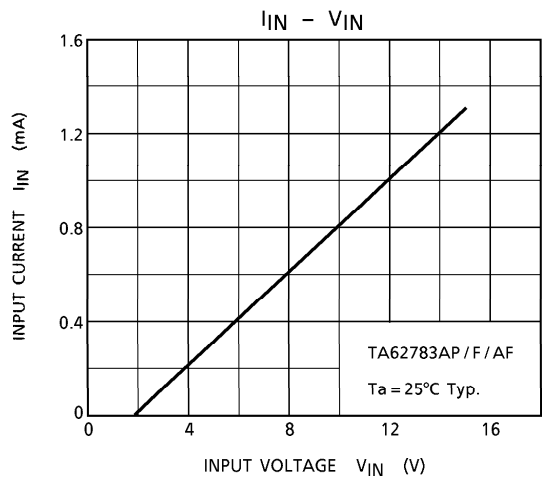
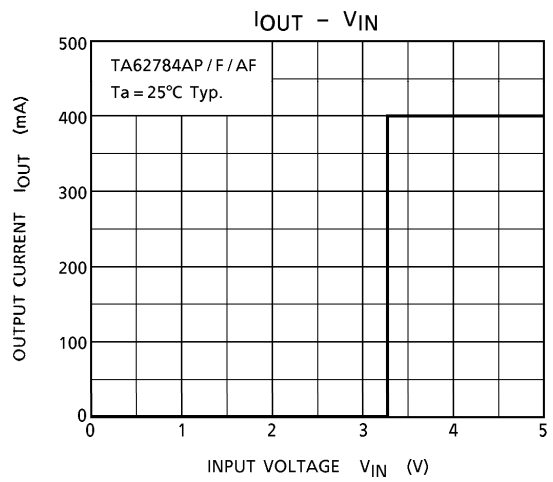
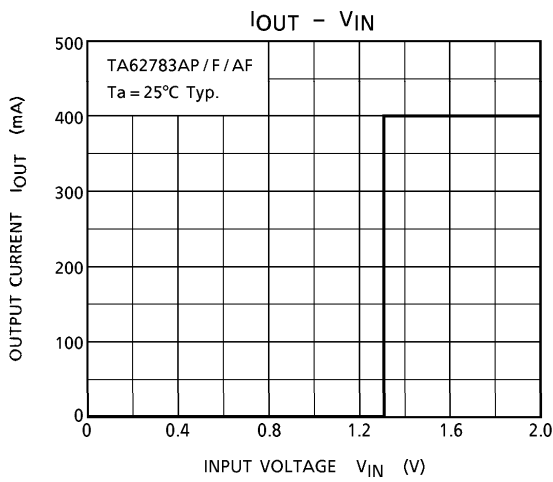
7. t_{ON}, t_{OFF}

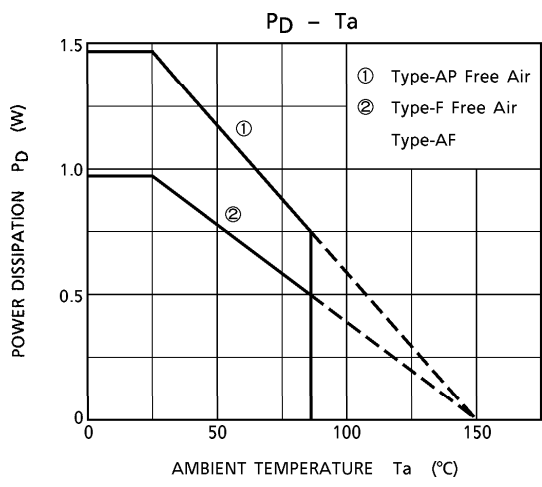


- (Note 1) Pulse width $50\mu s$, duty cycle 10%
Output impedance 50Ω , $t_r \leq 5ns$, $t_f \leq 10ns$
- (Note 2) C_L includes probe and jig capacitance

PRECAUTIONS for USING

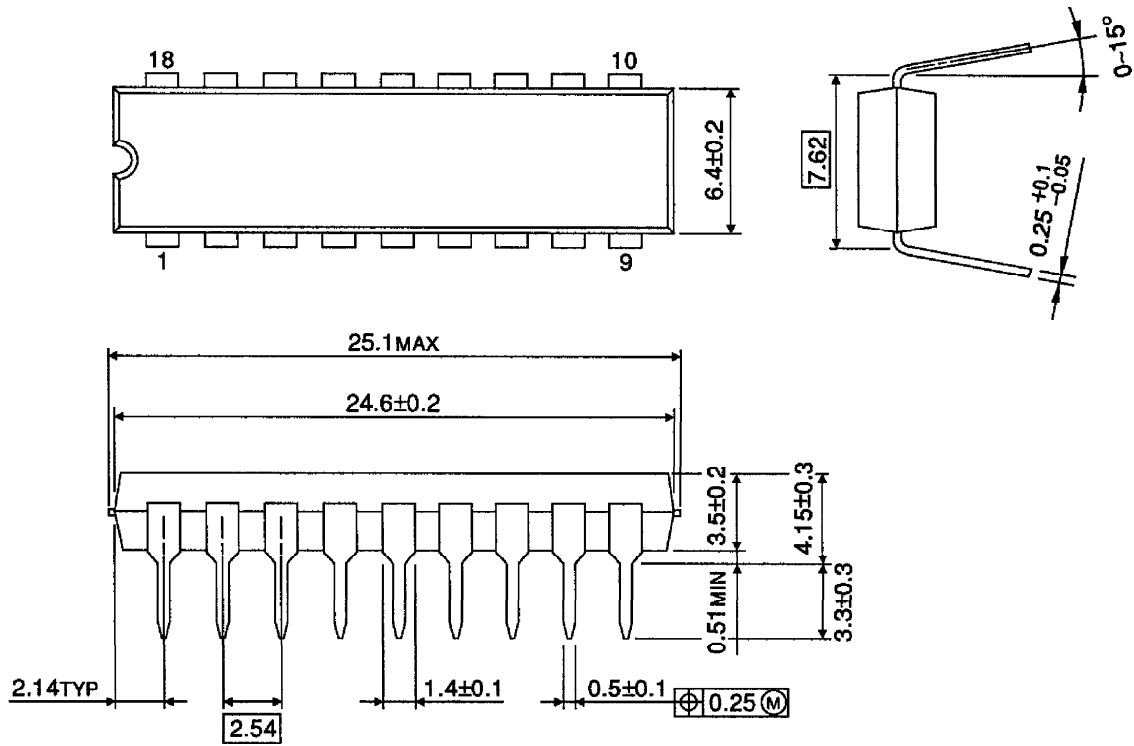
Utmost care is necessary in the design of the output line, V_{CC} and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.





OUTLINE DRAWING
DIP18-P-300-2.54D

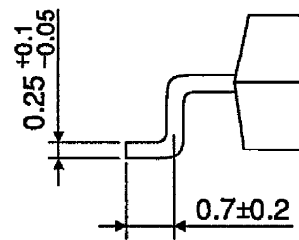
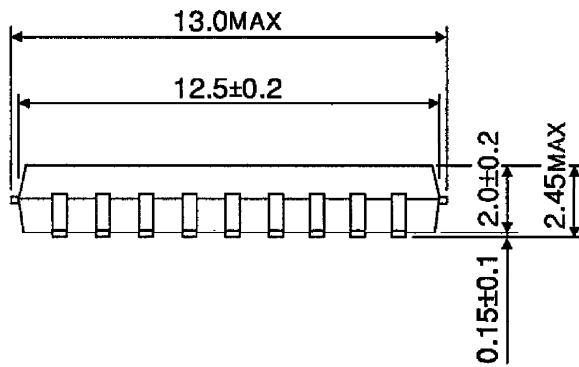
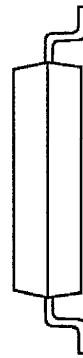
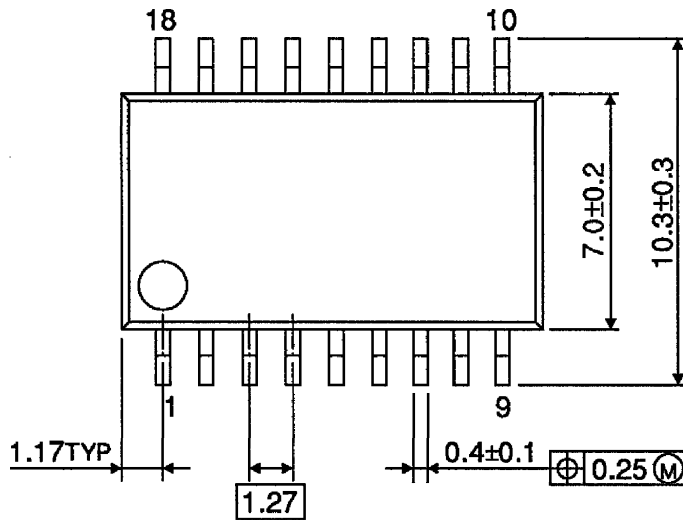
Unit : mm



Weight : 1.47g (Typ.)

OUTLINE DRAWING
SOP18-P-375-1.27

Unit : mm



Weight : 0.41g (Typ.)