# HIP7020

## J1850 Bus Transceiver For Multiplex Wiring Systems

June 1998

### Features

- **J1850 Bus Transceiver for MX Wiring**
- **5V CMOS/TTL Logic Interface**
- **Current Controlled Transmitter Driver**
- **Controlled Rise/Fall Time of Bus Drive for Both Voltage and Current**
- **Bus Drive Capability to Less Than 500Ω with a 5μs Load RC Time Constant**
- **Filtered Bus Input Receiver**
- **Ground Fault Tolerant for Bus Isolation**
- **Short Circuit and Over Temperature Protection**
- **Protection for Reverse Battery, Load Dump and Latch-Up**
- **±9kV ESD Protection BUS OUT and BATTERY Pins**
- **-40°C to 125°C Operating Range**
- **Loop-Back Fault Detection Mode**
- **4x (41.6kHz) Receive Speed**

### Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| HIP7020AB | -40 to 125 | 8 Ld SOIC | M8.15 |
| HIP7020AP | -40 to 125 | 8 Ld PDIP | E8.3 |

### Description

The HIP7020 IC is an Integrated I/O Bus Transceiver designed for the SAE Standard **J1850 Class B Data Communication Network Interface**. The Bus transmits and receives data on a single wire using a 10.4kHz VPWM (Variable Pulse Width Modulated) signal. The HIP7020 serves as an I/O buffer interfacing to 5V CMOS logic. It is designed to operate directly from the 12V battery line of an automobile. The normal Bus voltage swing capability is from 0V to 7.75V at currents greater than 20mA.

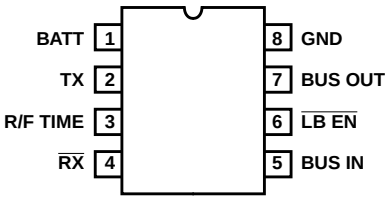
As shown in the Block Diagram, the Transmitter TX Input and the Receiver $\overline{RX}$ Output of the Bus Transceiver Circuit interface to the control logic. The TX input signal is wave shaped for rise time, fall time and amplitude before it is converted from voltage to current. The Wave Shaper with an external programming resistor, $R_S$ controls the rise and fall time of the BUS OUT output signal. The current source drive to the Bus is voltage controlled by the Wave Shaped Voltage Reference to a maximum limit as specified for the J1850 Bus and includes short-circuit current limiting.

The HIP7020 Receiver input, BUS IN is connected to the J1850 Bus through an external resistor, $R_F$ and has a trip point at one-half of the nominal Bus signal voltage which is 3.875V. The Receiver input is filtered to remove high frequency Bus noise by the external resistor and an internal capacitor. The Receiver Bus signal, after processing, is output at the $\overline{RX}$ pin by the $\overline{RX}$ Buffer's open collector driver. The $\overline{RX}$ output is active low and requires an external pull-up resistor returned to the control logic $V_{CC}$ supply. This prevents power-up of the control logic by the transceiver if $V_{CC}$ supply voltage is removed.

The HIP7020 has a Loop-Back Enable Mode Switch to return diagnostic information for the Bus Transceiver node. For an active low or an open $\overline{LB\ EN}$ input, the Transmit/Receive signals are internally "Looped-Back" to provide a TX to $\overline{RX}$ return signal path independent of signals on the Bus. A return path validation indicates proper action of the Bus Transceiver apart from the J1850 Bus.

### Pinout

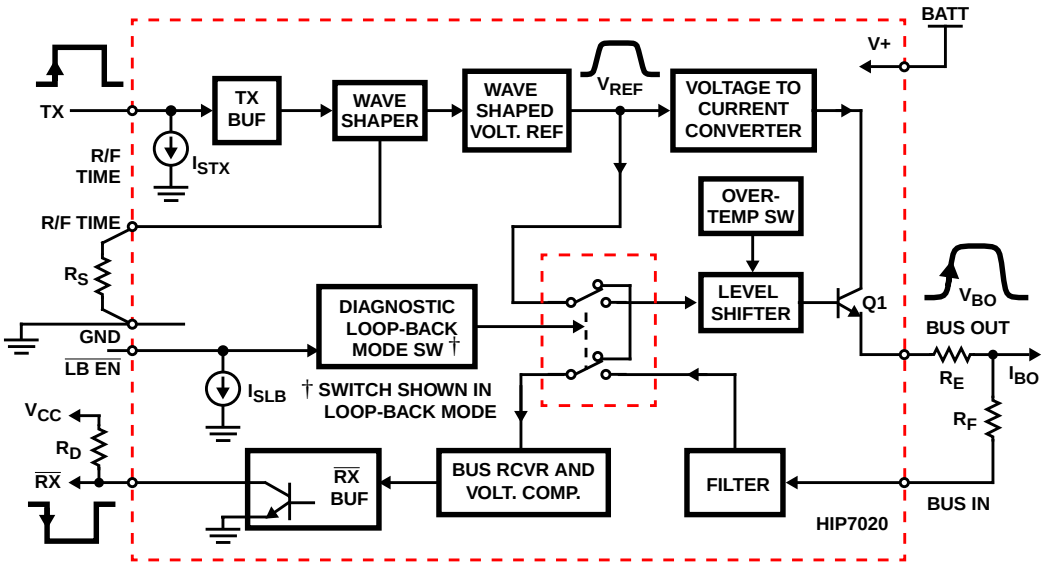
**HIP7020**
**(PDIP, SOIC)**
TOP VIEW





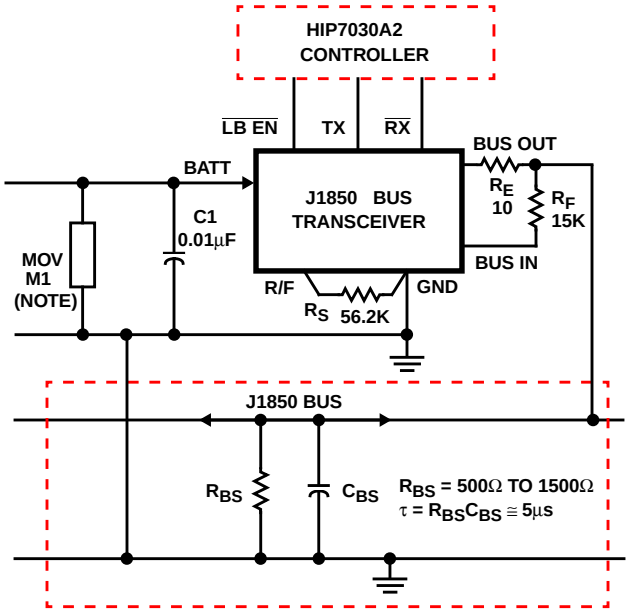

File Number **3642.3**

## Block Diagram




## Applications

The circuit of Figure 1 illustrates the essential elements of the J1850 Bus Transceiver in a normal application. For normal J1850 applications, a Bus Transceiver is used at each system node. The Electrical Specifications Table also refers to the peripheral components shown in Figure 1 and the Block Diagram for the HIP7020 Bus Transceiver.




NOTE: MOV, M1 represents central protection, normally on the alternator and with a typical value in the range of 27V to 40V.

**FIGURE 1. TYPICAL APPLICATION CIRCUIT DIAGRAM**

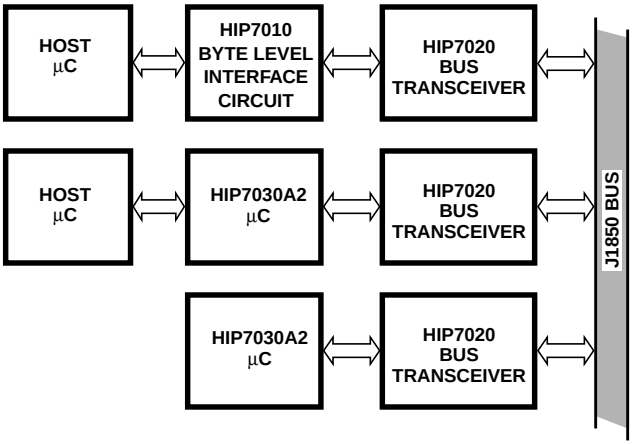



**FIGURE 2. TYPICAL J1850 SYSTEM CONFIGURATIONS**

**NOTE: The R/F bias resistor, $R_S$, should be located as close as possible to the IC to minimize noise coupling to the R/F pin. The ground connection of $R_S$ must be made directly to the GND pin of the IC with no other current flowing in the connecting line to prevent system ground currents from affecting the rise/fall time control of the Wave Shaper. The $R_S$ resistor value is typically specified as 1% tolerance. If an R/F bypass capacitor is used to filter noise, the value should be 100pF or less. For effective noise filtering, the R/F bypass capacitor should be connected direct from the R/F pin to the GND pin and should not carry current from other sources.**

Figure 2 illustrates some of the typical J1850 System Configurations that utilize the HIP7020 Bus Transceiver. Refer to the HIP7010 and HIP7030A2 Data Sheets for further information on J1850 System Configuration detail.

## Absolute Maximum Ratings

Supply Voltage, $V_{BATT}$ . . . . . -20V to +24V
Short Term Supply Voltage, $V_{BATT}$, 1s Max. (Note 2) . . . . . +35V
J1850 Bus Input Voltage, $V_{BUS\ IN}$ . . . . . ±20V
J1850 Bus Load Current, $I_{BO}$ . . . . . .Self-Limiting
TX Logic Input Voltage . . . . . GND -0.3V to 7V
$\overline{RX}$ Logic Output Current . . . . . 5mA
Load Dump (Note 2) . . . . . 40V
BUS Transient Susceptibility . . . . . (Note 3)
ESD: BUS OUT, BATTERY Pins, (Air Gap, Note 4) . . . . . ±9kV
BUS OUT, BATTERY Pins, (Direct, Note 4) . . . . . ±4.5kV
All Other Pins (Direct, Note 4) . . . . . ±2kV

## Operating Conditions

Temperature Range . . . . . $-40^oC$ to $125^oC$

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ ($^oC/W$) |
|---|---|
| PDIP Package | 120 |
| SOIC Package | 160 |

Maximum Junction Temperature . . . . . $150^oC$
Maximum Storage Temperature Range . . . . . $-40^oC$ to $150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^oC$
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.
2. Fault capability of the J1850 Bus Transceiver includes reverse battery, load dump and latch-up tolerance to ±200mA on any terminal. The Short Term Power Supply Voltage capability is 35V for a maximum of 1s. Continued operation at this voltage may cause thermal shutdown.
3. Transient Susceptibility Bus and Battery Pins Per SAE J1113, Aug 1987, Figures 7 Test Pulses 1, 2, 3A and 3B at -50V, +100V and ±200V respectively.
4. ESD Conditions - SAE J1113; Aug 1987. BUS OUT & BATTERY Pins: Air Gap and Direct Contact Discharge; R = 2kΩ, C = 150pF
All Other Pins: Direct Contact Discharge; R = 1.5kΩ, C = 100pF

## Electrical Specifications

$9.0V \le V_{BATT} \le 16V$; $R_S = 56.2k\Omega$ ±1%; except as noted, $R_{BS} = 500\Omega$ to $1500\Omega$ and $\tau = R_{BS}C_{BS} = 5\mu s$. All voltages are measured with respect to ground and the $T_A$ Range of $-40^oC$ to $125^oC$ shall not be exceeded during test unless otherwise specified. For test detail, refer to the Block Diagram, Figures 3 and 4 Test Circuits and Figures 5 and 6 Waveforms.

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Idle Supply Current | $I_{BATT}$ | BUS OUT Open; No Bus Signal; $V_{BATT}$ = 12.6V; $V_{TX}$ Low | | 90 | 200 | 350 | µA |
| Operating Voltage Range | $V_{BATT}$ | (Note 5) | | 6 | - | 24 | V |
| Supply Current, BUS OUT Short to GND | $I_{BATT(SG)}$ | BUS OUT Short to GND, $V_{TX}$ High | | 20 | - | 50 | mA |
| Supply Current, BUS OUT Short to BATT | $I_{BATT(SB)}$ | BUS OUT to $V_{BATT}$; $I_{BO}$ = 0 mA | $V_{TX}$ High | 2 | - | 8 | mA |
| | | | $V_{TX}$ Low | 90 | - | 350 | µA |
| Thermal Shutdown Temperature | $T_{SD}$ | (Note 6) | | 150 | - | 170 | $^oC$ |
| Thermal Shutdown Hysteresis | $T_{SDHYS}$ | (Note 6) | | 5 | 10 | 15 | $^oC$ |
| **TX CMOS/TTL INPUT WITH/PULL DOWN** | | | | | | | |
| Input Bias Current, TX | $I_{TX}$ | $V_{TX}$ = 7V; (Note 7) | | 20 | - | 38 | µA |
| Input Low Voltage | $V_{IL}$ | | | - | - | 0.8 | V |
| Input High Voltage | $V_{IH}$ | | | 2.0 | - | - | V |
| Input Capacitance | $C_{TX}$ | | | 2 | - | 5 | pF |
| **BUS OUT** | | | | | | | |
| BUS OUT High Voltage | $V_{BOH}$ | $V_{TX}$ High | | 6.6 | - | 8.5 | V |
| BUS OUT Low Voltage | $V_{BOL}$ | Bus Load, $R_{BS}$ = 1.5kΩ; $V_{TX}$ Low | | - | - | 0.1 | V |
| BUS OUT Voltage, Low Battery | $V_{BOH(PSL)}$ | $6V \le V_{BATT} < 9V$; $V_{TX}$ High | | Note 13 | - | 8.5 | V |
| Source Current, Bus Low | $I_{BO\_LIMIT}$ | $-20V \le V_{BUS\ OUT} < [V_{BOH}$ (Measured) - 0.8V]; $V_{TX}$ High | | -20 | - | -42 | mA |
| BUS OUT During LOOPBACK | $V_{LOOPBACK}$ | $\overline{LB\ EN}$ Low, $V_{TX}$ High | | - | - | 1 | V |

**Electrical Specifications** $9.0V \leq V_{BATT} \leq 16V$; $R_S = 56.2k\Omega \pm 1\%$; except as noted, $R_{BS} = 500\Omega$ to $1500\Omega$ and $\tau = R_{BS}C_{BS} = 5\mu s$. All voltages are measured with respect to ground and the $T_A$ Range of $-40^oC$ to $125^oC$ shall not be exceeded during test unless otherwise specified. For test detail, refer to the Block Diagram, Figures 3 and 4 Test Circuits and Figures 5 and 6 Waveforms. **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Bus Emissions Voltage Output | $V_{dB\_LIMIT}$ | | -60 | - | - | dBV |
| BUS OUT Leakage Currents<br>Battery Low/Off1 | $I_{BO\_LEAK}$ | $0V \leq V_{BUS\ OUT} \leq 20V$; $0V \leq V_{BATT} \leq 0.8V$; $-0.3V \leq V_{TX} \leq 7V$ | -10 | - | 10 | µA |
| Battery Low/Off2 | | $-20V \leq V_{BUS\ OUT} \leq 0V$; $0V \leq V_{BATT} \leq 0.8V$; $-0.3V \leq V_{TX} \leq 7V$ | -100 | - | 10 | µA |
| Bus High | | $V_{BOH} < V_{BUS\ OUT} \leq 20V$; $6V \leq V_{BATT} \leq 16V$; $2V \leq V_{TX} \leq 7V$ | -10 | - | 10 | µA |
| TX Low1 | | $0V \leq V_{BUS\ OUT} \leq 20V$; $6V \leq V_{BATT} \leq 16V$; $-0.3V \leq V_{TX} \leq 0.8V$ | -10 | - | 10 | µA |
| TX Low2 | | $-20V \leq V_{BUS\ OUT} < 0V$; $9.5V \leq V_{BATT} \leq 16V$; $-0.3V \leq V_{TX} \leq 0.8V$ | -3000 | - | 10 | µA |
| With Loss of Ground1 (Note 11) | | $V_{GND} \leq V_{BUS\ OUT} < 20V$; $0V \leq V_{BATT} \leq 16V$; $-0.3V \leq V_{TX} \leq 7V$; $0V \leq (V_{BATT} - V_{GND}) \leq 0.8V$ | -10 | - | 10 | µA |
| With Loss of Ground2 (Note 11) | | $-20V \leq V_{BUS\ OUT} \leq V_{GND}$; $0V \leq V_{BATT} \leq 16V$; $-0.3V \leq V_{TX} \leq 7V$; $0V \leq (V_{BATT} - V_{GND}) \leq 0.8V$ | -100 | - | 10 | µA |
| TX to BUS OUT Propagation Delays | $t_{DTXHBO}$, $t_{DTXLBO}$ | $R_S = 56.2k\Omega$; $V_{BUS\ OUT} = 3.875V$ (Note 8) | 9 | 16 | 23 | µs |
| BUS OUT Transition Times, Rise and Fall | $t_r$, $t_f$ | $R_S = 56.2k\Omega$; Measured on BUS OUT between 1.5V and 6.25V (Note 8) | 11 | 16 | 19 | µs |
| BUS OUT Noise Rejection | $N_R$ | $f_R$ = 30Hz to 250kHz; $V_{BATT}$ to BUS OUT | 20 | - | - | dB |
| BUS OUT RF Isolation | $N_I$ | $f_I$ = 0.25MHz to 200MHz; $V_{BATT}$ to BUS OUT | 20 | - | - | dB |
| **BUS IN** | | | | | | |
| Input Threshold Voltage | $V_{BIH}$ | | 3.6 | - | 4.15 | V |
| Input Bias Current | $I_{BIN}$ | $-20V \leq V_{BUS\ IN} \leq 20V$ | -5 | - | 5 | µA |
| Input Capacitance | $C_{BIN}$ | | 10 | - | 20 | pF |
| **$\overline{RX}$ OUTPUT** | | | | | | |
| Output Voltage, Low | $V_{IL}$ | $I_{\overline{RX}} = 1.6mA$ | 0.01 | - | 0.4 | V |
| Output Current | $I_{\overline{RX}}$ | $V_{\overline{RX}} = 5V$ (Note 10) | 2 | 5 | 8 | mA |
| Output Leakage Current | $I_{\overline{RX}(LK)}$ | $V_{\overline{RX}} = 5V$, $R_D = 10k\Omega$; $V_{BUSIN}$ Low | -10 | - | 10 | µA |
| Receive Propagation Delay | $t_{D\overline{RX}ON}$, $t_{D\overline{RX}OFF}$ | Measured from BUS IN Threshold Voltage | 1 | - | 3 | µs |
| **$\overline{LB}$ $\overline{EN}$ CMOS/TTL INPUT WITH/PULL DOWN** | | | | | | |
| Input Low Voltage | $V_{IL}$ | | - | - | 0.8 | V |
| Input High Voltage | $V_{IH}$ | | 2.0 | - | - | V |
| Input Bias Current | $I_{LB}$ | $V_{LB} = 7V$; (Note 9) | 5 | - | 12 | µA |
| TX To $\overline{RX}$ Turn ON, OFF; Delay In Loop-Back Mode | $t_{DLBON}$, $t_{DLBOFF}$ | $V_{LB}$ Low; Toggle TX; Meas. $\overline{RX}$ | 12 | - | 26 | µs |
| $\overline{LB}$ $\overline{EN}$ Turn ON, OFF; TX to BUS OUT | $t_{D(LH)}$, $t_{D(HL)}$ | $V_{TX}$ High; Toggle $\overline{LB}$ $\overline{EN}$; Meas. BUS OUT | 1 | - | 10 | µs |

NOTES:

5. In the operating voltage range from 6V to 8.5V the BUS OUT, $V_{BOH}$ is limited by the low power supply. In the operating voltage range from 16V to 24V the maximum bus load is limited by the package power dissipation ratings.
6. Over-temperature shutdown with hysteresis is incorporated to protect the IC under system failure conditions.
7. Measured Current into the TX terminal is determined by Pull-Down Current Sink.
8. Propagation Delay limits are measured at the 3.875V level on BUS OUT. Rise and Fall Times are measured between 1.5V and 6.25V on the BUS OUT terminal.
9. Measured Current into the $\overline{LB}$ $\overline{EN}$ terminal is determined by Pull-Down Current Sink.
10. The $I_{\overline{RX}}$ Output Current test parameter defines Short Circuit protection limits.
11. Loss of Ground refers to loss of module (node) Ground which results in a voltage between the Battery and IC Ground of less than 0.8V. For voltage between Battery and Ground above 0.8V, the Transceiver Bus Output may become active. The module circuit in Figure 3 is used to measure the Loss of Ground leakage.
12. Unless otherwise noted, all Electrical Specification test conditions are as shown in Figure 4.
13. The lower limit is 6.6V or $V_{BATT}$ - 1.7V, whichever is less.

## Test Circuits

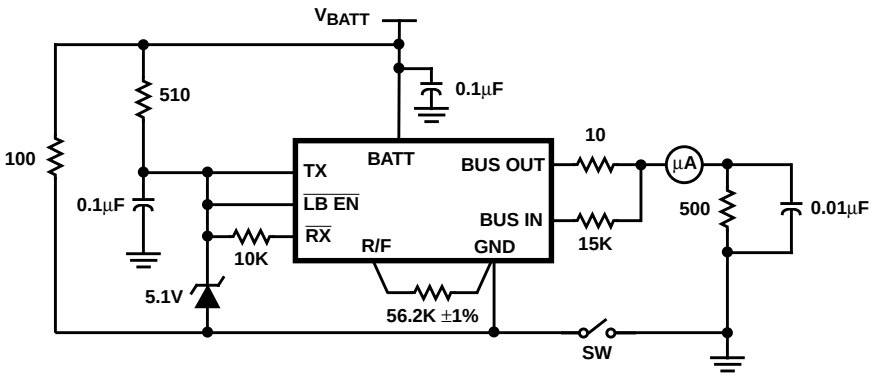



FIGURE 3. LOSS OF GROUND LEAKAGE TEST CIRCUIT

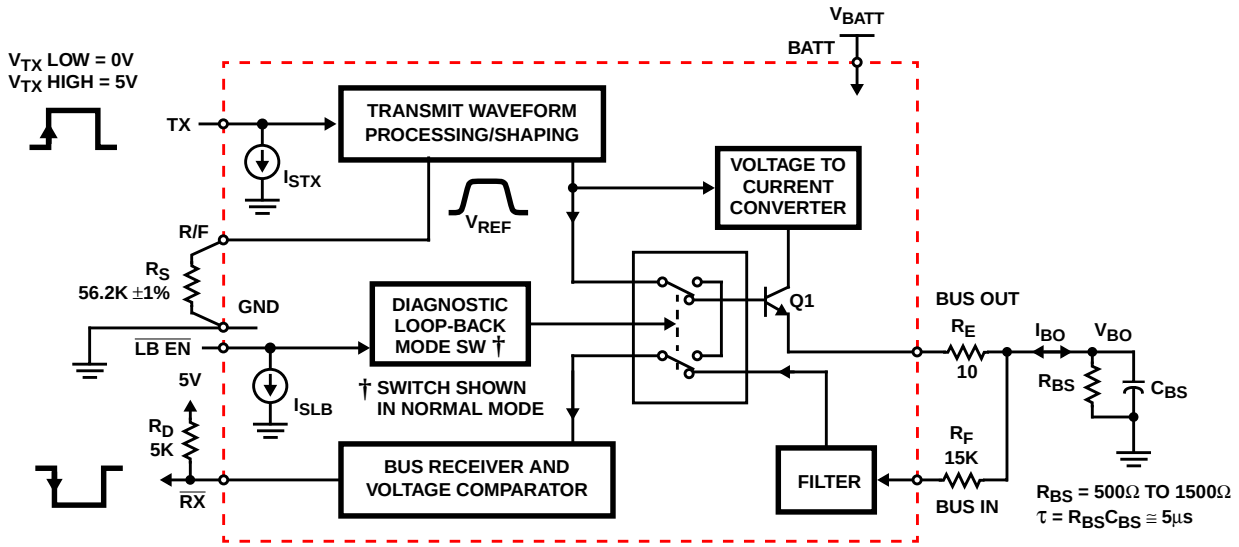



FIGURE 4. ELECTRICAL SPECIFICATION TEST CIRCUIT

## HIP7020 Signal Interface

The HIP7020 is a member of the Intersil family of low cost multiplexed wiring ICs. As a Bus Transceiver IC, it interfaces the module and system control logic to the vehicle signal bus wiring. The integrated functions of the Bus Transceiver serve as an interface for a “Class B” multiplexed communications network. The TX digital interface is designed to accept CMOS/TTL logic levels and convert them to the appropriate J1850 analog serial data levels. This is accomplished using an internally generated reference waveform and voltage driver with a controlled current source to supply an analog signal output to the J1850 bus load of 500Ω (typical). Because of the special wave shaping used to control the J1850 bus waveform, it is regarded as an analog signal.

In the receive mode the incoming bus analog signals are input to the receiver at the BUS IN terminal. The bus data is converted to logic information by comparing it to an on-chip reference voltage. The received signal is provided as digital output from an open collector transistor driver at the $\overline{RX}$ output.

In the transmit mode a CMOS/TTL digital signal is received at the TX input. It is then rise and fall time controlled, wave shaped and level adjusted. A voltage controlled current driver circuit transmits the signal from the BUS OUT terminal to the J1850 Bus with current limiting protection.

## Functional Blocks

The Bus Transceiver IC functional blocks, as shown in the Block Diagram, are as follows:

### TX BUF (Transmit Input Buffer Interface)

The TX Buffer input function is a data interface to the wave-shaper reference circuit. The CMOS/TTL logic levels to be transmitted are input to the TX pin.

### Waveshaper Circuit

This stage defines the transitions of high and low signal levels to provide a uniform rise and fall time. The input signal to the Waveshaper is the TX Buffer output and is an active high signal. In the Waveshaper the Transmit signal is amplified and compared to an internal reference voltage. The Waveshaper also provides waveform corner shaping on both the positive and negative going transitions. The rise and fall time of the serial waveform is set by the Waveshaper circuit and an external programming resistor, $R_S$ that sets an internal current reference at the R/F pin for control of the rise and fall slopes of the waveform. As previously noted, to prevent ground currents of the bus and node from affecting the rise/fall time control of the Wave Shaper, the resistor, $R_S$, should be located as close as possible to the IC. To minimize noise coupling to the R/F pin, the ground connection of $R_S$ should be made directly to the GND pin of the IC with no other current flowing in the connecting line.

### Wave Shaped Voltage Reference Drive, $V_{REF}$

The Wave Shaped Voltage Reference circuit sets a scaled analog signal level and maintains a constant peak-to-peak voltage during worst case battery voltage conditions, including cold cranking. The analog signal from the Wave Shaped Voltage Reference circuit drives the Voltage-to-Current Converter and a Level Shifter Interface to the bus driver transistor, Q1. The Voltage-to-Current Converter, in addition to the waveform leveling, helps to preserve low RFI and drive integrity. The edges of the wave shaped waveform, $V_{REF}$ have well defined rise and fall times and the knees of the waveform are smooth and rounded as signal conditioning to reduce RFI.

### Voltage-to-Current Converter

The Voltage-to-Current Converter determines the maximum current to be sourced out to the J1850 bus and is designed to source current proportional to the input signal from the Wave Shaped Voltage Reference, $V_{REF}$. The output of the Voltage-to-Current Converter maintains drive integrity of the $V_{REF}$ waveform without the use of feedback.

A small quiescent current source is supplied to maintain a fixed minimum for each bus node. This precisely fixes the quiescent current at low input signal drive to the Voltage-to-Current Converter.

### Voltage Controlled Current Driver, Q1

The Voltage Controlled Current Driver, Q1, controls the amount of current sourced out to the J1850 Bus. The Wave Shaped Voltage Reference, $V_{REF}$, drives the base of Q1 and the Voltage-to-Current Converter drives the collector of Q1. Both voltage and current determine the drive level which is supplied to the bus. When the Bus voltage is below the level determined by the Voltage Reference, $V_{REF}$, the Voltage Controlled Current Driver allows more current to be sourced out to the J1850 Bus. Voltage drive may increase as needed until the Bus voltage and the Voltage Reference match or until the maximum current limit is reached, as set by the Voltage-to-Current Converter. When the Bus voltage is above the Voltage Reference the Voltage Controlled Current Drive to the J1850 Bus is decreased. Decreasing correction occurs until the Bus voltage and the Voltage Reference match or until zero current is being sourced.

### Filter, Bus Receiver and Voltage Comparator

The Filter limits the high frequency bandwidth by external resistor, $R_F$, and the input capacitance of the Filter Block. The on-chip Filter network and the external resistor, $R_F$, form a low pass filter to reject high frequency noise that may be present on the bus. Resistor, $R_F$, also provides isolation protection from transients. The analog bus signal is passed to the Bus Receiver and Voltage Comparator which determine when the bus is high or low as referenced to half the nominal bus voltage at the BUS IN pin.

### $\overline{RX}$ BUF (Receiver Output Buffer Interface)

The $\overline{RX}$ BUF function is a buffer for the logic output as determined by the Bus Receiver and Voltage Comparator. An open collector transistor supplies current switched output to an external load resistor, $R_D$. BUS IN data is converted to serial CMOS/TTL logic data which is output at the $\overline{RX}$ pin of the HIP7020. Resistor, $R_D$, is biased from the digital 5V supply for optimum output drive levels to the logic circuits and to avoid power-up of the digital parts via the transceiver.

### Thermal Shutdown

Over-temperature shutdown with hysteresis is incorporated to protect the IC under system failure conditions. Temperature is sensed at the transistor, Q1. Thermal shutdown will occur when the temperature of the chip reaches $150^oC$ (minimum) and will latch-off the HIP7020 Transmitter operation. A reset occurs on the first positive edge transition of the next transmit data bit after ~$10^oC$ decrease in chip temperature. Hysteresis in the thermal shutdown threshold is necessary to allow the temperature to decrease to a safe operating temperature, typically less than $140^oC$.

### Diagnostic Loop-Back Mode Switch

The HIP7020 has an active low Loop-Back Enabled Mode Switch which controls an internal signal path to provide diagnostic information. When Enabled, the Transmit/Receive signals are internally “Looped-Back” independent of the signal conditions on the J1850 Bus. A return path validation indicates proper action of the Bus Transceiver apart from the J1850 Bus. In the Loop-Back Mode, the transistor, Q1 output is forced low, preventing the output from sourcing current to the bus. Loop-Back is not affected by thermal shutdown.

NOTE: The Block Diagram switch position is shown for Loop-Back operation. A pull-down at the $\overline{LB\ EN}$ input forces an active low Loop-Back mode as the default position when no connection is applied.

## Operational Description

### Bus Output Signal

The BUS OUT output drive from the HIP7020 conforms to the SAE Standard **J1850 Class B Data Communication Network Interface** document specifications. It meets these requirements without oscillation, glitches or overshoots. The digital signal to be transmitted is wave shaped and amplitude controlled to produce an analog serial data waveform with precisely defined rise and fall edges. Operational capability covers a wide range of bus load resistances, capacitances and characteristic impedance while complying with the arbitration requirements of the Bus. Transient noise interference

on the bus is minimized by the bus interface filtering and control circuitry of the Bus Transceiver IC.

High Current may exist during noise interference and bus arbitration conditions on the bus. To limit instantaneous current direction change and minimize the level of fluctuating current caused by these conditions, a series resistance is used in the bus output of the HIP7020. (See Figure 1). A small resistor, $R_E$, from the BUS OUT pin to the bus module connection forces a distribution of bus current between transmitting modules and provides load stability to the IC.

The HIP7020 maintains a uniform and consistent bus waveform having specific transition times and propagation delays to preserve a J1850 analog data stream. Transmitted bus data is encoded by a HIP7010 Byte Level IO or HIP7030 J1850 microcontroller, (see Figure 1) where “1s” and “0s” are defined by the length of time in which the bus voltage is high or low. Precise waveform control is necessary for a receiving node to accurately decode the difference between “1s” and “0s” by the time duration of high levels and low levels on the bus. In order to retain bus data integrity, digital information to be transmitted on the bus is wave shaped and amplitude controlled in the Bus Transceiver. The transmitted signal output to the J1850 Bus is a waveform with uniform edge control and precisely defined voltage levels.

### Bus Current and Voltage Control

The Bus Transceiver has a Wave Shaped Voltage Reference which controls both the Voltage-to-Current Converter and the Bus Voltage Driver, Q1. The Voltage-to-Current Converter supplies a limited current feed to the collector of Q1. Together this provides the function of a Voltage Controlled Current Driver which controls the bus voltage drive level while supplying limited current to drive the bus load.

### Wave Shaped Voltage Reference, $V_{REF}$

The output of the Wave Shaped Voltage Reference is a uniform signal which is a scaled waveform of the desired bus signal and is shown as $V_{REF}$ in Block Diagram. This signal controls the output current driver and is the input to the Voltage-to-Current Converter. The internal reference voltage, $V_{REF}$ is isolated from the J1850 Bus and is totally unaffected by the signal conditions on the bus. This isolation provides superior Bus stability in the vehicle environment. The bus drive control interface maintains the integrity of the $V_{REF}$ waveform supplied to the bus. This is done without feedback control which is inherently susceptible to oscillation.

### Voltage-to-Current Converter

The Voltage-to-Current Converter generates a current, $I_{BO}$ which is proportional to the Wave Shaped Voltage Reference magnitude and wave shape. This is the maximum current that can be supplied to the bus and is limited to a value of 30mA typical.

### Voltage Controller Current Driver

The Voltage Controller Current Driver, Q1, is the device which controls the amount of the available current which will be sourced out to the bus as determined by the Voltage Reference and allowed by the Voltage-to-Current Converter.

When the Bus voltage is below the Voltage Reference, Q1 allows more current to be sourced out to the J1850 Bus; until the Bus voltage and the Voltage Reference match or until the maximum current limit is reached as set by the Voltage-to-Current Converter.

When the Bus voltage is above the Voltage Reference, Q1 allows less current sourced out to the J1850 Bus; until the Bus voltage and the Voltage Reference match or until zero current is being sourced from Q1.

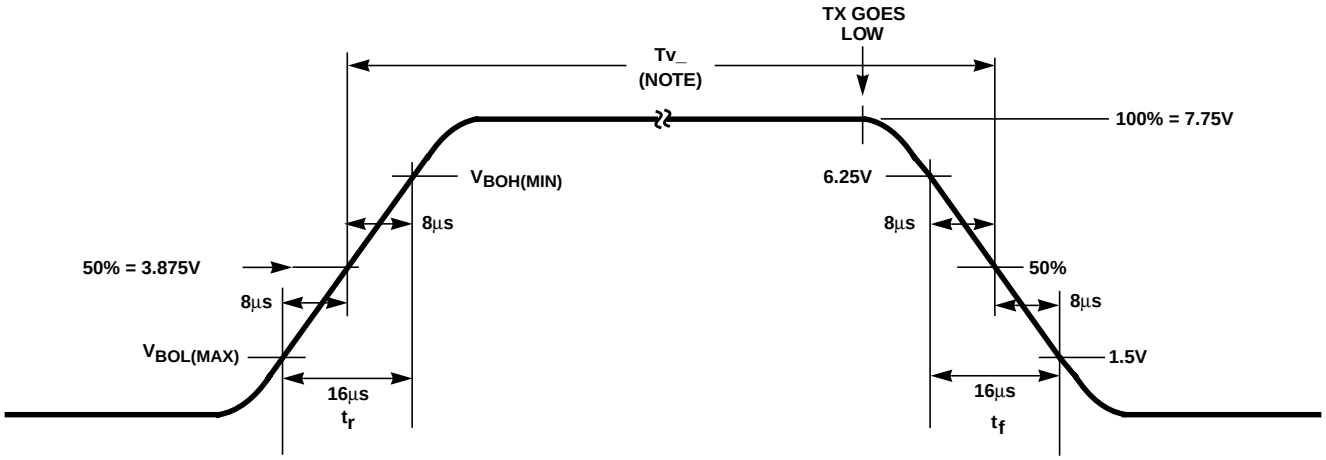
### Bus Output Waveform

The bus output waveform shown in Figure 5 is controlled by the internal Wave Shaper and has a tightly controlled rise and fall time with rounded corners. The rise/fall times, $t_r$ and $t_f$, are defined between $V_{BOL}$ and $V_{BOH}$.

### Constant Propagation Time Delay

There is a constant propagation time delay from TX signal going high or low to the BUS OUT signal (measured at 3.875V). The propagation time delay signals are shown in Figure 6. The timing to reach the 50% voltage level of the bus signal from the start of TX input going high is $t_{DTXHBO}$. The propagation time delay from the start of TX input going low is $t_{DTXLBO}$.

The BUS IN input signals, as shown in Figure 6, are characterized by the $V_{BIH}$ and $V_{BIL}$ specifications which include hysteresis. There is a constant propagation delay for the Bus to $\overline{RX}$ receive channel of the Bus Transceiver. The received propagation delay times are $t_{D\overline{RX}ON}$ and $t_{D\overline{RX}OFF}$ as measured in reference to the 50% voltage level on the rising or falling edge of the BUS IN input signal to the rising or falling edge of the $\overline{RX}$ output signal.




NOTE:
Refer to SAE J1850, Table 5 for definition of Tv_ time duration definitions. i.e. By Definition a Short pulse = Tv1: $t_{TX(NOM)} = t_{\overline{RX}(NOM)} = 64\mu s$.

**FIGURE 5. J1850 BUS WAVEFORM**

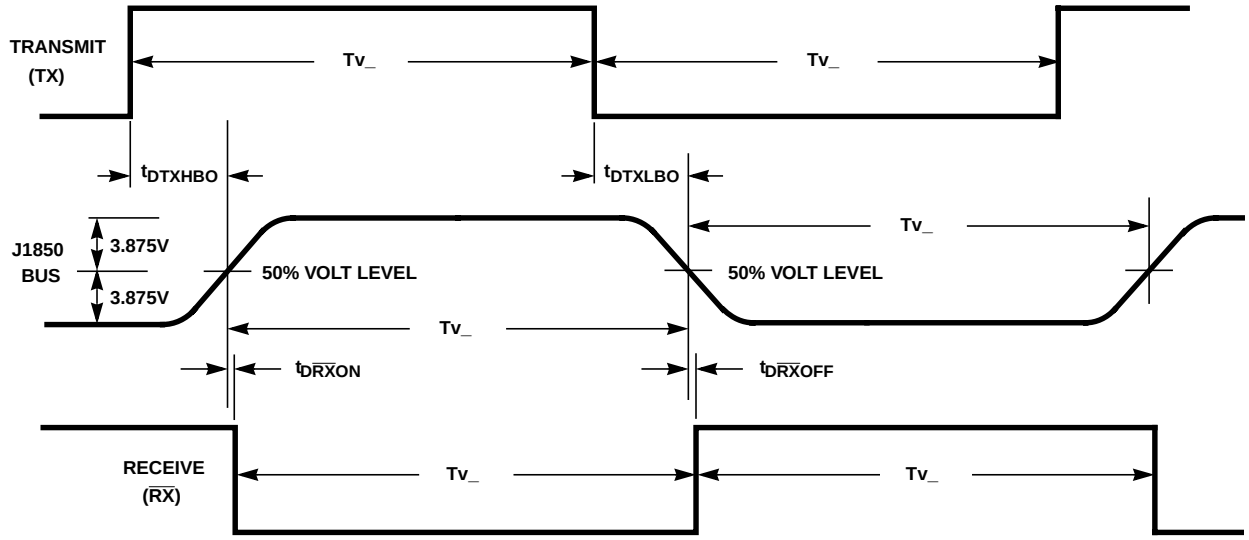



**FIGURE 6. PROPAGATION TIME DELAYS**

### Low Pass Filter Input

The bus input has an on-chip input filter to strip off the unwanted incoming high frequency noise. The 3dB point of this filter is nominally 750kHz.

### Diagnostic Bus-Isolated Loop-Back

An on-chip Bus-Isolated Diagnostic Loop-Back function is controlled by the $\overline{\text{LB EN}}$ pin. The Loop-Back function is a mode switch that is enabled by placing a logic low on the $\overline{\text{LB EN}}$ pin. When activated, the signal flow is cross-switched to open the Bus Receive Input and connect the Voltage Reference, $V_{REF}$ output to the input of the Bus Receiver. This "Loops-Back" the TX signal to the $\overline{\text{RX}}$ output while maintaining isolation from the signal on the J1850 Bus. When the Loop-Back is enabled, diagnostic trouble shooting can be done at each individual node regardless of fault conditions on the bus.

### Thermal Shut Down Protection

On-chip Thermal Shutdown Protection is designed to shut-down source drive to the J1850 bus and protect the Bus Transceiver IC output. The temperature shutdown threshold is set to protect the absolute maximum junction temperature of the chip and is nominally set for $160^oC$ with $10^oC$ of hysteresis. Thermal shutdown may occur when overload conditions exist on the bus. (See Function Blocks - Thermal Shutdown.)

## Package Pinout

### BATT

The BATT pin is connected directly to the vehicle Battery (Ignition) line. The Battery supply connection ($V_{BATT}$) provides voltage for all on-chip functions, including the voltage reference. As such, the BATT input is designed to withstand transient power supply conditions.

### TRANSMIT (TX)

The TRANSMIT pin will accept standard CMOS/TTL logic level input data. Logic level data is input at the TRANSMIT (TX) pin in a serial format, such as provided by a Intersil HIP7030A2 J1850 Controller, and is output on the J1850 Bus at the BUS OUT pin. The TX input has an active pull down current sink to insure that a logic level low will be maintained when no signal drive is present.

### RECEIVE ($\overline{RX}$)

The $\overline{RX}$ pin is the output for J1850 Bus data and interfaces to an open collector transistor output driver. The RX digital data output is inverted from the analog bus data input at the BUSIN pin. The data from the $\overline{RX}$ pin is output to a Intersil HIP7010 Byte Level I/O or a HIP7030A2 J1850 Microcontroller IC where the 10.4 Kbps VPWM messages from the J1850 network are decoded.

### GROUND

This is the HIP7020 Bus Transceiver IC ground reference for all the signals which interface to the control logic and the J1850 bus. It is also the ground return path for the BATTERY power supply to IC.

### R/F TIME

The R/F (Rise/Fall) Time pin connects the external resistor, $R_S$, from the wave shaped voltage reference to ground. The Rise and Fall Time is controlled by the transition slope of the signal waveform. The resistor, $R_S$, sets an internal current reference to control the rise and fall slope. As previously noted, the resistor, $R_S$, should be located as close as possible to the IC to minimize noise coupling to the R/F pin. Also, the ground connection of $R_S$ must be made directly to the GND pin of the IC with no other current flowing in the connecting line.

### BUS IN

The BUS IN pin is the receive input of the SAE J1850 Bus signal. It receives the 10.4kHz VPWM (Variable pulse width modulated) data from the single wire analog serial bus through an external Resistor, $R_F$.

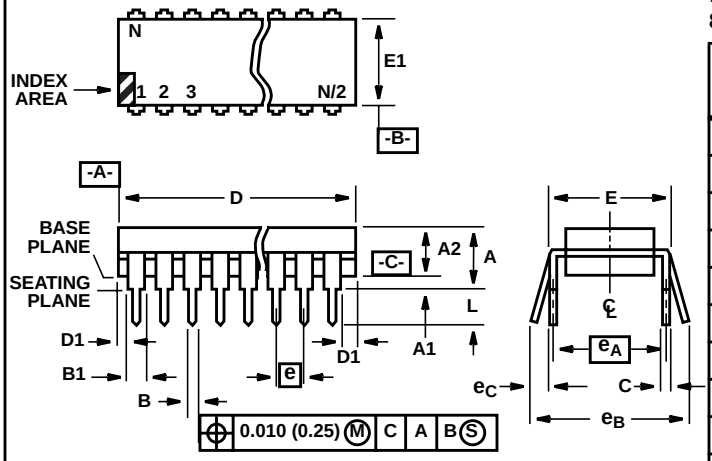
### BUS OUT

The BUS OUT pin transmits the SAE J1850 10.4kHz VPWM (Variable Pulse Width Modulated) data to the serial bus. Data is transmitted to the serial J1850 bus with the same polarity as the TX input signal.

### $\overline{LB\ EN}$

The $\overline{LB\ EN}$ Loop-Back Enable pin controls the Diagnostic Loop-Back Mode Switch function. A logic low on the $\overline{LB\ EN}$ pin connects the output of the Wave Shaped Voltage Reference to the Bus Receiver and Voltage Comparator while disconnecting the filtered input of J1850 Bus. This feature provides the means to trouble shoot system problems.

## Dual-In-Line Plastic Packages (PDIP)




**E8.3 (JEDEC MS-001-BA ISSUE D)**
**8 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.210 | - | 5.33 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.115 | 0.195 | 2.93 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.045 | 0.070 | 1.15 | 1.77 | 8, 10 |
| C | 0.008 | 0.014 | 0.204 | 0.355 | - |
| D | 0.355 | 0.400 | 9.01 | 10.16 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.300 | 0.325 | 7.62 | 8.25 | 6 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| $e_A$ | 0.300 BSC | | 7.62 BSC | | 6 |
| $e_B$ | - | 0.430 | - | 10.92 | 7 |
| L | 0.115 | 0.150 | 2.93 | 3.81 | 4 |
| N | 8 | | 8 | | 9 |

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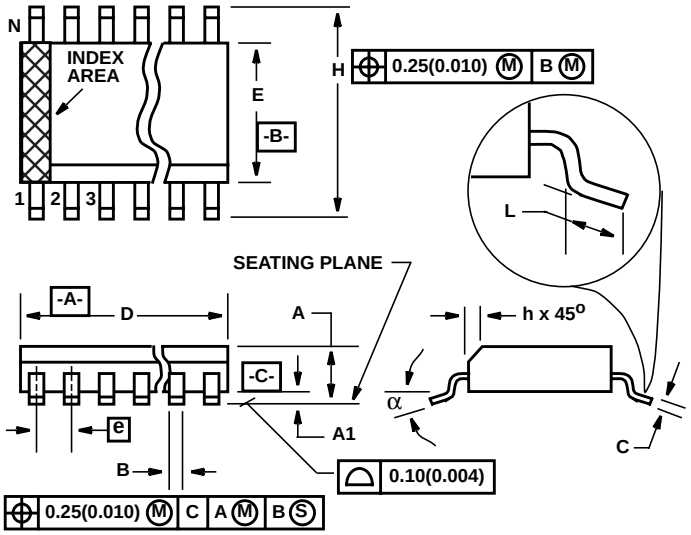
NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $e_A$ are measured with the leads constrained to be perpendicular to datum -C-.
7. $e_B$ and $e_C$ are measured at the lead tips with the leads unconstrained. $e_C$ must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

## Small Outline Plastic Packages (SOIC)




**M8.15 (JEDEC MS-012-AA ISSUE C)**
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| α | $0^o$ | $8^o$ | $0^o$ | $8^o$ | - |

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.



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