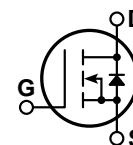


## POWER MOS V

Power MOS V is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V also achieves faster switching speeds through optimized gate layout.



- **Faster Switching**
- **100% Avalanche Tested**
- **Lower Leakage**
- **Surface Mount D³PAK Package**




### MAXIMUM RATINGS

All Ratings:  $T_C = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	APT5024SVR	UNIT
$V_{DSS}$	Drain-Source Voltage	500	Volts
$I_D$	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	22	Amps
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	88	
$V_{GS}$	Gate-Source Voltage Continuous	$\pm 20$	Volts
$V_{GSM}$	Gate-Source Voltage Transient	$\pm 30$	
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	280	Watts
	Linear Derating Factor	2.24	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$T_L$	Lead Temperature: 0.063" from Case for 10 Sec.	300	
$I_{AR}$	Avalanche Current <sup>①</sup> (Repetitive and Non-Repetitive)	22	Amps
$E_{AR}$	Repetitive Avalanche Energy <sup>①</sup>	30	mJ
$E_{AS}$	Single Pulse Avalanche Energy <sup>④</sup>	1210	

### STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-Source Breakdown Voltage ( $V_{GS} = 0V, I_D = 250\mu\text{A}$ )	500			Volts
$I_{D(on)}$	On State Drain Current <sup>②</sup> ( $V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$ )	22			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance <sup>②</sup> ( $V_{GS} = 10V, 0.5 I_{D(Cont.)}$ )			0.24	Ohms
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{DS} = V_{DSS}, V_{GS} = 0V$ )			25	$\mu\text{A}$
	Zero Gate Voltage Drain Current ( $V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$ )			250	
$I_{GSS}$	Gate-Source Leakage Current ( $V_{GS} = \pm 20V, V_{DS} = 0V$ )			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 1.0\text{mA}$ )	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

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**DYNAMIC CHARACTERISTICS**

**APT5024SVR**

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
$C_{iss}$	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		3400		pF
$C_{oss}$	Output Capacitance			470		
$C_{rss}$	Reverse Transfer Capacitance			180		
$Q_g$	Total Gate Charge <sup>③</sup>	$V_{GS} = 10V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_{D[Cont.]} @ 25^\circ C$		138		nC
$Q_{gs}$	Gate-Source Charge			19		
$Q_{gd}$	Gate-Drain ("Miller") Charge			65		
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_{D[Cont.]} @ 25^\circ C$ $R_G = 1.6\Omega$		11		ns
$t_r$	Rise Time			10		
$t_{d(off)}$	Turn-off Delay Time			44		
$t_f$	Fall Time			7		

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$I_S$	Continuous Source Current (Body Diode)			22	Amps
$I_{SM}$	Pulsed Source Current <sup>①</sup> (Body Diode)			88	
$V_{SD}$	Diode Forward Voltage <sup>②</sup> ( $V_{GS} = 0V, I_S = -I_{D[Cont.]}$ )			1.3	Volts
$t_{rr}$	Reverse Recovery Time ( $I_S = -I_{D[Cont.]}, di_S/dt = 100A/\mu s$ )		415		ns
$Q_{rr}$	Reverse Recovery Charge ( $I_S = -I_{D[Cont.]}, di_S/dt = 100A/\mu s$ )		6.6		$\mu C$

**THERMAL CHARACTERISTICS**

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.45	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
- ② Pulse Test: Pulse width < 380  $\mu s$ , Duty Cycle < 2%
- ③ See MIL-STD-750 Method 3471
- ④ Starting  $T_j = +25^\circ C$ ,  $L = 5.00mH$ ,  $R_G = 25\Omega$ , Peak  $I_L = 22A$

APT Reserves the right to change, without notice, the specifications and information contained herein.

**D<sup>3</sup>PAK Package Outline**

