DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR
2SK3408

N-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

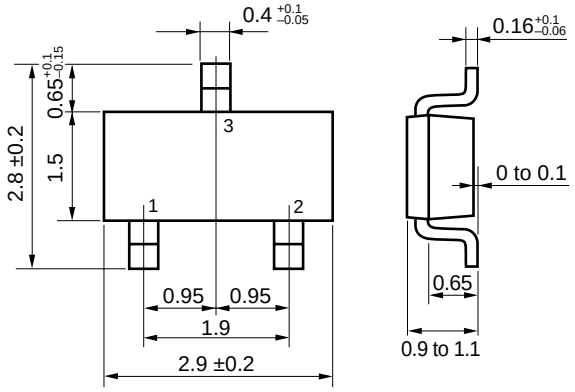
The 2SK3408 is a switching device which can be driven directly by a 4-V power source.

The 2SK3408 features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of dynamic clamp of relay and so on.

FEATURES

- Can be driven by a 4-V power source
- Low on-state resistance
  $R_{DS(on)1}$ = 195 mΩ MAX. (V_{GS} = 10 V, I_D = 0.5 A)
  $R_{DS(on)2}$ = 250 mΩ MAX. (V_{GS} = 4.5 V, I_D = 0.5 A)
  $R_{DS(on)3}$ = 260 mΩ MAX. (V_{GS} = 4.0 V, I_D = 0.5 A)
- Built-in G-S protection diode against ESD.

PACKAGE DRAWING (Unit : mm)

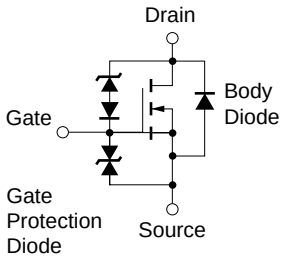


1 : Gate
2 : Source
3 : Drain

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3408	SC-96 Mini Mold (Thin Type)

EQUIVALENT CIRCUIT



Marking: XF

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	43±5	V
Drain to Gate Voltage (V_{GS} = 0 V)	V_{DGS}	43±5	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±1.0	A
Drain Current (pulse) **Note1**	$I_{D(pulse)}$	±4.0	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	0.2	W
Total Power Dissipation (T_A = 25°C) **Note2**	P_{T2}	1.25	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%
2. Mounted on FR-4 Board, t ≤ 5 sec.

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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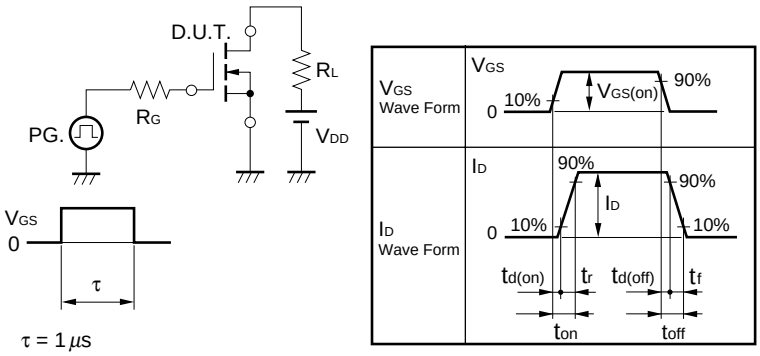
The mark ★ shows major revised points.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

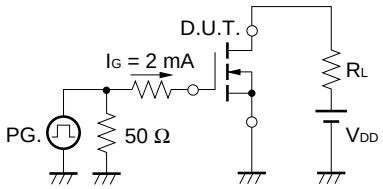
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30.4 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 0.5 A	1	2.0		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 0.5 A		155	195	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 0.5 A		185	250	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 0.5 A		195	260	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		230		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		50		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		30		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 20 V		18		ns
Rise Time	t_r	I_D = 0.5 A		14		ns
Turn-off Delay Time	$t_{d(off)}$	$V_{GS(on)}$ = 10 V		115		ns
Fall Time	t_f	R_G = 10 Ω		38		ns
Total Gate Charge	Q_G	V_{DS} = 30.4 V		4.0		nC
Gate to Source Charge	Q_{GS}	I_D = 1.0 A		1.0		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		1.0		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 1.0 A, V_{GS} = 0 V		0.81		V
Reverse Recovery Time	t_{rr}	I_F = 1.0 A, V_{GS} = 0 V		25		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		16		nC

TEST CIRCUIT 1 SWITCHING TIME



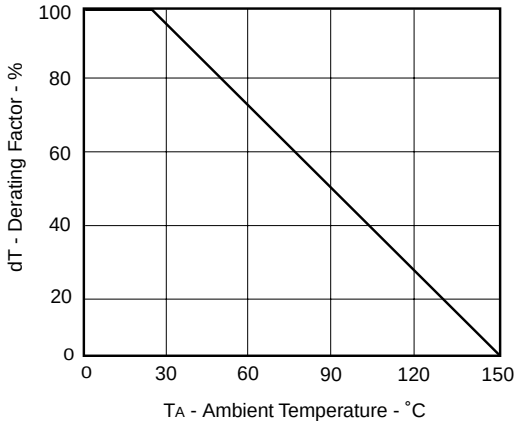
τ = 1 μs
Duty Cycle ≤ 1%

TEST CIRCUIT 2 GATE CHARGE

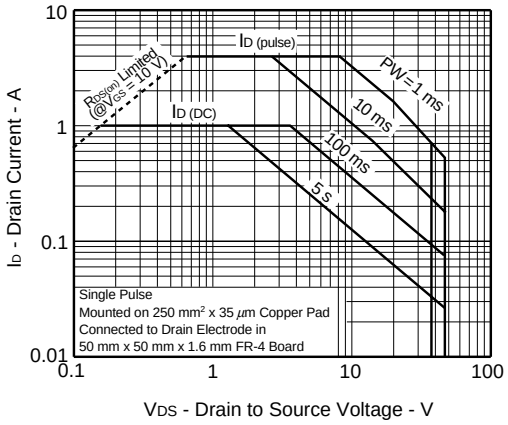


TYPICAL CHARACTERISTICS (T_A = 25°C)

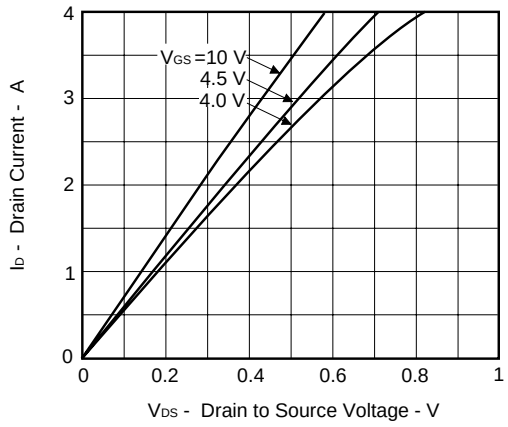
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



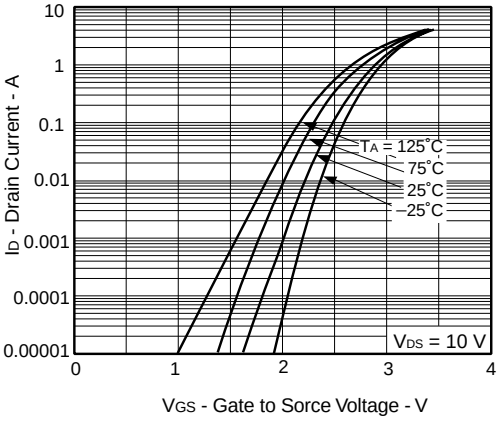
★ FORWARD BIAS SAFE OPERATING AREA



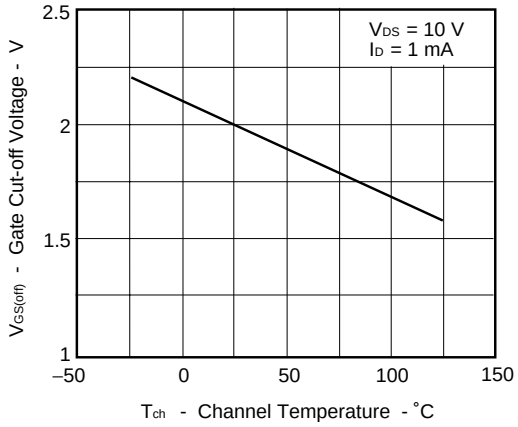
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



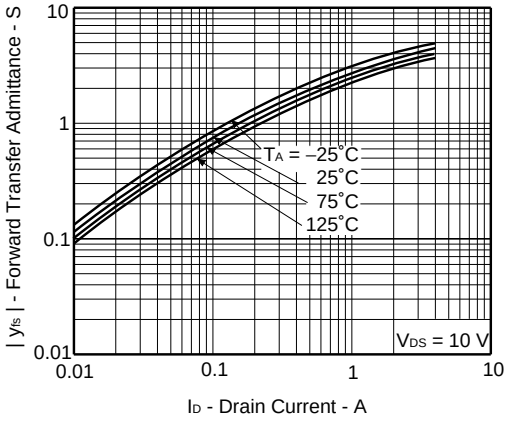
FORWARD TRANSFER CHARACTERISTICS



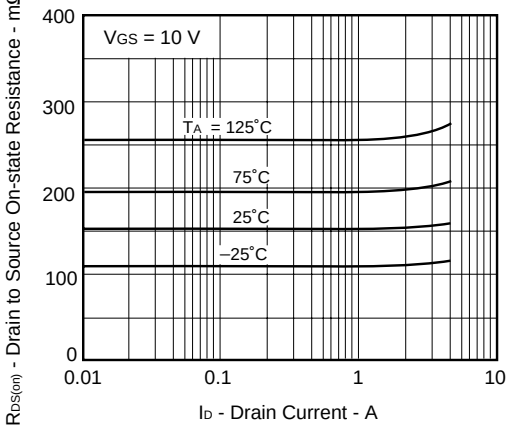
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



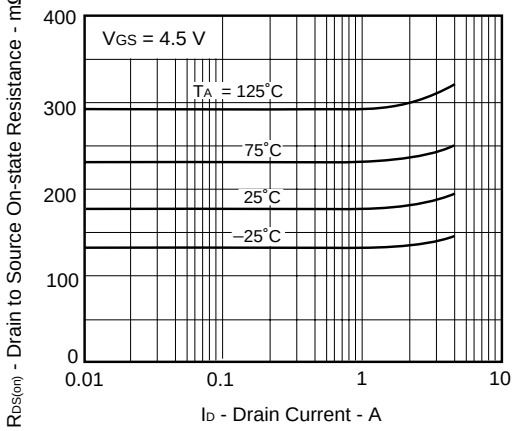
FORWARD TRANSFER ADMITTANCE Vs. DRAIN CURRENT



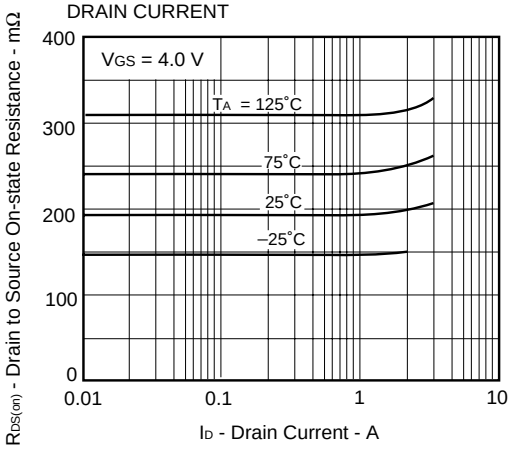
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



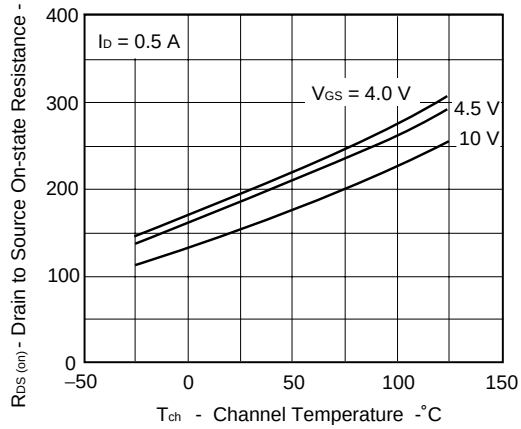
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



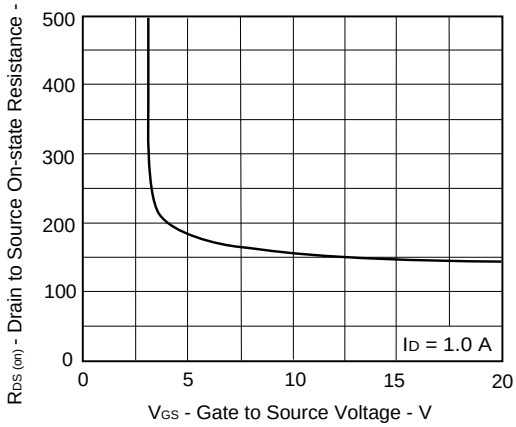
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



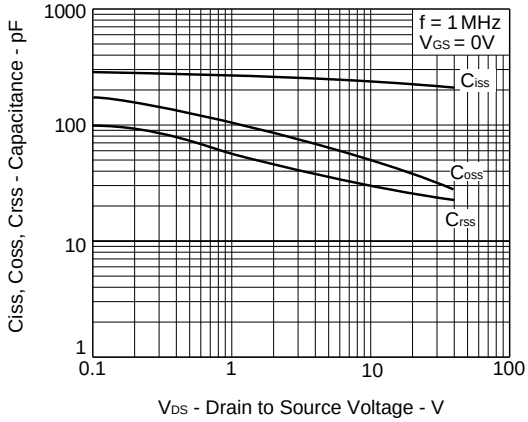
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



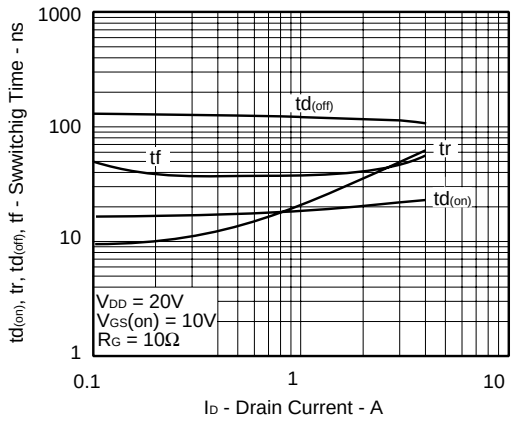
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



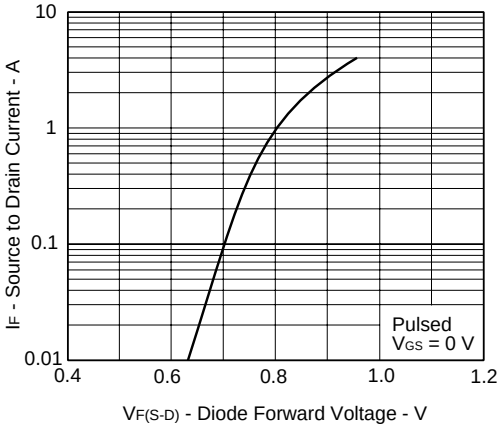
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



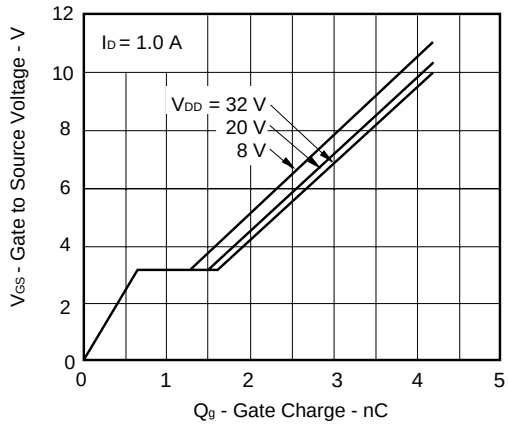
SWITCHING CHARACTERISTICS



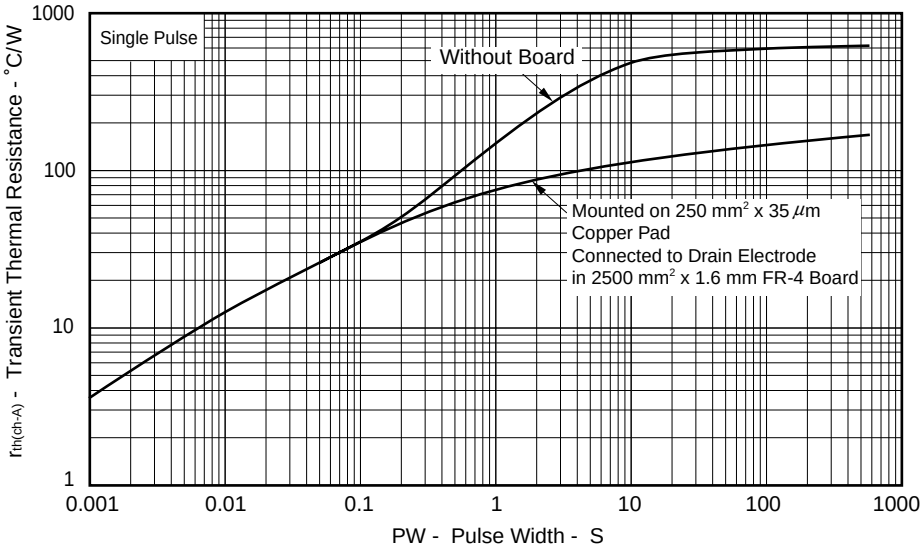
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



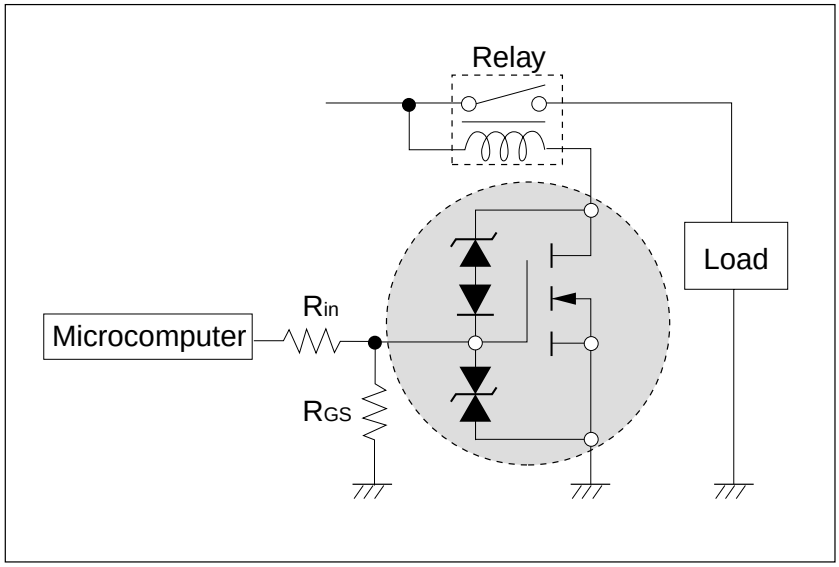
DYNAMIC INPUT CHARACTERISTICS



★ TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



DYNAMIC CLAMP APPLICATION



Remarks **1.** Input resistance is necessary to Gate terminal.
(Range ; 1kΩ to 10kΩ, Recommend ; 3kΩ)

2. Pull down resistance is necessary between Gate to Source**.**
(Several 10kΩ)

[MEMO]

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