

CUSTOMER PRODUCT SPECIFICATION

Z86C27-ROM Z86C97-ROMLESS CMOS Z8® 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The Z86C27 and Z86C97 Digital Television Controller (DTC) introduce a new level of sophistication to single-chip architecture. The Z86C27/C97 are members of the Z8 single-chip microcontroller family with 8 Kbytes of ROM (Z86C27), ROMIess (Z86C97) and 236 bytes of RAM. Both devices are housed in a 64-pin DIP package, and are CMOS compatible. Having the ROM/ROMless selectivity, the DTC offers both external memory and pre-programmed ROM which enables the Z8 microcontroller to be used in a high volume production application device embedded with a custom program (customer supplied program). The Z86C97 ROMIess offers the use of external memory rather than a preprogrammed ROM. This enables the Z8 microcontroller to be used in prototyping, low volume applications or where code flexibility is required. Zilog's DTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z86C27/C97 architecture is characterized by utilizing Zilog's advanced Superintegration[™] design methodology. The devices have an 8-bit internal data path controlled by a Z8 microcontroller, and On Screen Display (OSD) logic circuits/Pulse Width Modulators (PWM). Onchip peripherals include two register mapped I/O ports (Ports 2 and Port 3), Interrupt control logic (1 software, 2 external and 3 internal interrupts) and a standby mode recovery input port (Port 3, pin P30).

The OSD control circuits support 8 rows by 20 columns for 128 kinds of characters. The character color is specified

by row. One of the 8 rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying either low resolution (5x7 dot pattern) or high resolution (11x15 dot pattern) characters. The Z86C97 currently supports high resolution characters only.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Seven 6-bit PWM ports are used for controlling audio signal level. Five 8-bit PWM ports are used to vary picture levels.

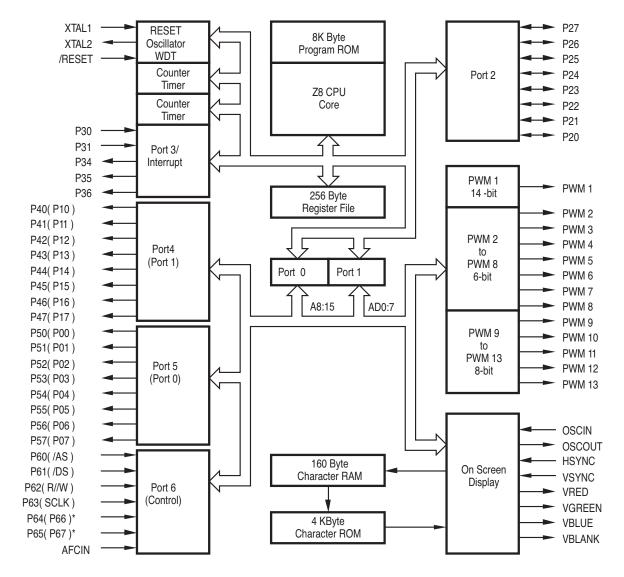
The DTC applications demand powerful I/O capabilities. The Z86C27/C97 fulfills this with 35 I/O pins dedicated to input and output. These lines are grouped into five ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Register File and Data Memory. The Register File is composed of 236 bytes of general purpose register, two I/O Port registers and 15 control and status registers.

To unburden the program from coping with the real-time problems such as counting/timing and data communication, the DTC's offer two on-chip counter/timers with a large number of user selectable modes (see block diagram).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

GENERAL DESCRIPTION (Continued)



* () Denotes Z86C97 signal differences.

Functional Block Diagram

PIN CONFIGURATION

PWM5 🔲 1	U	64 🗆	PWM6	PWM5		1	U	64	PWM6
PWM4 🗌 2		63 🗆	PWM7	PWM4		2		63	PWM7
PWM3 🗆 3		62 🗆	PWM8	PWM3		3		62	PWM8
PWM2 🗆 4		61 🗆	PWM9	PWM2		4		61	PWM9
PWM1 🛛 5		60 🗆	PWM10	PWM1		5		60	PWM10
P35 🗖 6		59 🗆	PWM11	P35		6		59	PWM11
P36 🗌 7		58 🗆	PWM12	P36		7		58	PWM12
P34 🗖 8		57 🗆	PWM13	P34		8		57	PWM13
P31 🗖 9		56 🗆	P27	P31		9		56] P27
P30 🗌 10		55 🗆	P26	P30		10		55] P26
XTAL1 🗖 11		54 🗆	P25	XTAL1		11		54] P25
XTAL2 🔲 12		53 🗆	P24	XTAL2		12		53] P24
/RESET 🗆 13		52 🗆	P23	/RESET		13		52] P23
P60 🗌 14		51 🛛	GND	/AS		14		51] GND
GND 🗆 15	Z86C27	50 🗆	P22	GND		15		50	P22
P61 🔲 16	200021	49 🗆	P21	/DS		16	Z86C97	49] P21
P62 🔲 17		48 🗆	VCC	R//W		17		48	
VCC 🗆 18		47 🗆	P20	VCC		18		47] P20
P63 🗖 19		46 🗆	P47	SCLK		19		46] P17
P64 🗖 20		45 🗆	P46	P66		20		45] P16
P65 🗖 21		44 🗆	P45	P67		21		44	P15
AFCIN 🗖 22		43 🗆	P44	AFCIN		22		43] P14
P50 🗌 23		42 🗆	P43	P00		23		42] P13
P51 🗖 24		41 🗆	P42	P01		24		41] P12
P52 🗖 25		40 🗆	P41	P02		25		40] P11
P53 🗖 26		39 🗆	P40	P03		26		39] P10
P54 🗖 27		38 🗆	VBLANK	P04		27		38] VBLANK
P55 🗖 28		37 🗆	VBLUE	P05		28		37	VBLUE
P56 🗖 29		36 🗆	VGREEN	P06		29		36	VGREEN
P57 🗖 30		35 🗆	VRED	P07		30		35	VRED
OSCIN 🗖 31		34 🗆	VSYNC	OSCIN	Ц	31		34	VSYNC
OSCOUT 🛛 32		33 🗆	HSYNC	OSCOUT	Ц	32		33] HSYNC
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Z86C27 Mask-ROM Plastic DIP

Z86C97 ROMIess Plastic DIP

ABSOLUTE MAXIMUM RATINGS

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters	Min	Max	Units	Notes
V _{cc}	Power Supply Voltage †	-0.3	+7	V	
V	Input Voltage	-0.3	V _{cc} +0.3	V	
V	Input Voltage	-0.3	V _{cc} +0.3	V	[1]
V _o	Output Voltage	-0.3	V _{cc} +8.0	V	[2]
I _{он}	Output Current High		-10	mA	1 pin
I _{он}	Output Current High		-100	mA	all total
I _{OL}	Output Current Low		20	mA	1 pin
I _{OL}	Output Current Low		40	mA	[3] (1 pin)
1	Output Current Low,all total		200	mA	
T _A	Operating Temperature	++			
T _{STG}	Storage Temperature	-65	+150	С	

Notes:

[1] Port 2 open-drain

[2] PWM open-drain outputs

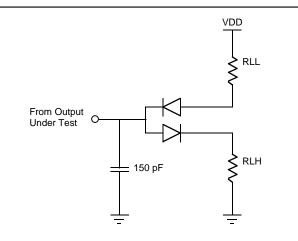
[3] Port 5

+ Voltage on all pins with respect to GND.

++ See Ordering Information

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Test Load Diagram).





CAPACITANCE

 $T_A = 25^{\circ}C$, $V_{CC} = GND = 0$ V, Freq=1.0 MHz, unmeasured pins to GND.

Parameter	Мах	Units
Input capacitance	10	рF
Output capacitance	20	рF
I/O capacitance	25	рF
AFC _{IN} input capacitance	10	pF

DC CHARACTERISTICS $T_A=0^{\circ}C$ to +70°C; $V_{CC}=+4.5$ V to +5.5 V; $F_{OSC}=4$ MHz

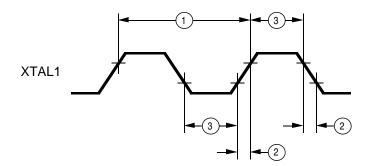
Symbo	ol Parameter	T _A =0°C Min	to +70°C Max	Typical @ 25°C	Units	Conditions
V _{IL} V _{ILC} V _{IH} V _{IHC}	Input Voltage Low Input XTAL/Osc In Low Input Voltage Input XTAL/Osc in High	0 0.7 V _{cc} 0.8 V _{cc}	$\begin{array}{c} 0.2 \ V_{\mathrm{cc}} \\ 0.07 \ V_{\mathrm{cc}} \\ V_{\mathrm{cc}} \\ V_{\mathrm{cc}} \end{array}$	1.48 0.98 3.0 3.2	V V V V	External Clock Generator Driven External Clock Generator Driven
V _{HY} V _{PU} V _{OL}	Schmitt Hysteresis Maximum Pull-up Voltage Output Voltage Low	0.1 V _{cc}	12 0.4 0.4	0.8 0.16 0.19	V V V V	[2] I _{oL} =1.00 mA I _{oL} =3.2 mA, [1]
V ₀₀₋₀₁ V ₀₁₋₁₁	AFC Level 01 In AFC Level 11 In	0.5 V _{cc}	0.4 1.5 0.45 V _{cc} 0.75 V _{cc}	0.19 1.00 1.9 3.12	V V V V	I _{oL} =0.75 mA [2] I _{oL} =10 mA [1]
V _{OH} I _{IR} I _{IL} I _{OL}	Output Voltage High Reset Input Current Input Leakage Tri-State Leakage	V _{cc} -0.4 -3.0 -3.0	-80 3.0 3.0	4.75 -46 0.01 0.02	ν μΑ μΑ	I _{OH} = -0.75 mA V _{RL} =0 V 0 V,V _{CC} 0 V,V _{CC}
I _{CC} I _{CC1} I _{CC2}	Supply Current		20 6 10	13.2 3.2 0	mA mA μA	All inputs at rail All inputs at rail All inputs at rail

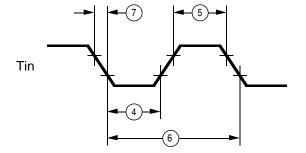
Notes:

[1] Port 5 [2] PWM Open-Drain

AC CHARACTERISTICS

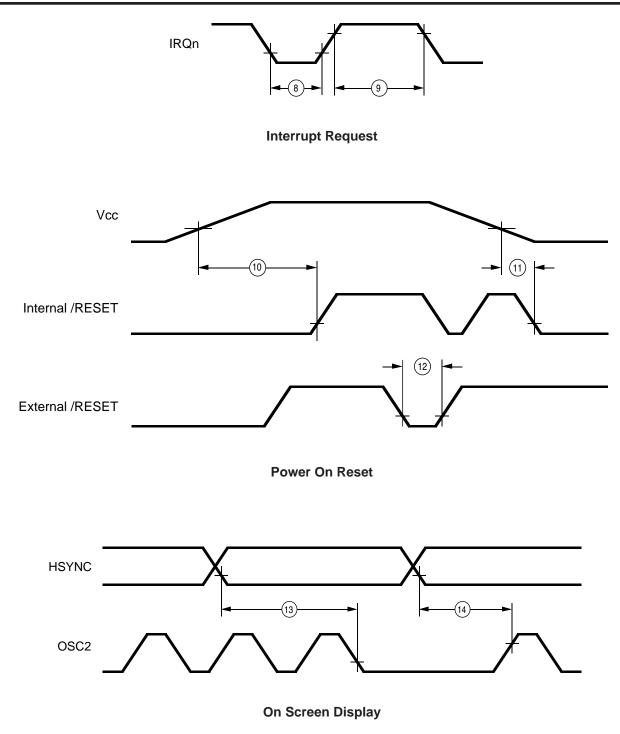
Timing Diagrams





External Clock

Counter Timer



AC CHARACTERISTICS $T_A=0^{\circ}$ C to +70° C; $V_{cc}=+4.5$ V to +5.5 V; $F_{osc}=4$ MHz,

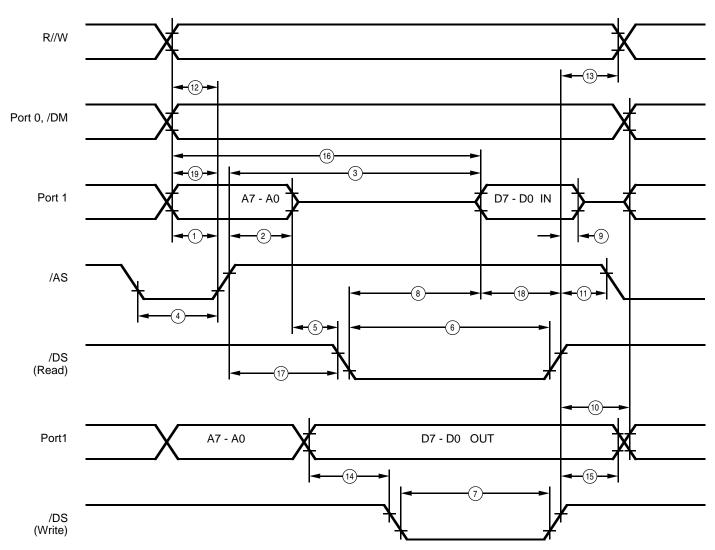
No	Symbol	Parameter	Min	Max	Unit
1	ТрС	Input clock period	250	1000	ns
2	TrC,TfC	Clock input raise and fall		15	ns
3	TwC	Input clock width	125		ns
4	TwTinL	Timer input low width	70		ns
5	TwTinH	Timer input high width	3 TpC		
6	TpTin	Timer input period	8 TpC		
7	TrTin,TfTin	Timer input raise and fall		100	ns
8A	TwIL	Int req input low	70		ns
8B	TwIL		3 TpC		
9	TwIH	Int request input high	3 TpC		
10	TdPOR	Power On Reset delay	25	100	ms
11	TdLVIRES	Low voltage detect to In- Internal RESET condition	200		ns
12	TwRES	Reset minimum width	5 TpC		
13	TdHsOI	Hsync start to Vosc stop	2 TpV	3 TpV	
14	TdHsOh	Hsync end to Vosc start		1 TpV	
15	TdWDT	WDT Refresh Time		12	ms

Notes:

[1] Refer to DC Characteristics for details on switching levels.

* Units in nanoseconds

AC CHARACTERISTICS Unique to Z86C97 External Memory Read/Write Timing Diagram



Z86C97 External Memory Read/Write Timing

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AC CHARACTERISTICS

Unique to Z86C97, $T_A = 0^{\circ}$ C to +70°C; $V_{cc} = +4.5$ V to +5.5 V; $F_{osc} = 4$ MHz

1TdA(AS)Address Valid to /AS High Delay352TdAS(AS)/AS High to Address Float Delay453TdAS(DR)/AS High to Read Data Required Valid2504TwAS/AS Low Width555TdAZ(DS)Address Float to /DS Low06TwDSR/DS (Read) Low Width1857TwDSWDS (Write) Low Width1108TdDSR(DR)/DS Low to Read Data Required Valid1309ThDR(DS)Read Data to /DS High Hold5		Notes
3TdAS(DR)/AS High to Read Data Required Valid2504TwAS/AS Low Width555TdAZ(DS)Address Float to /DS Low06TwDSR/DS (Read) Low Width1857TwDSWDS (Write) Low Width1108TdDSR(DR)/DS Low to Read Data Required Valid1309ThDR(DS)Read Data to /DS High Hold5	ns	[2]
4TwAS/AS Low Width555TdAZ(DS)Address Float to /DS Low06TwDSR/DS (Read) Low Width1857TwDSWDS (Write) Low Width1108TdDSR(DR)/DS Low to Read Data Required Valid1309ThDR(DS)Read Data to /DS High Hold5	ns	[2]
5TdAZ(DS)Address Float to /DS Low06TwDSR/DS (Read) Low Width1857TwDSWDS (Write) Low Width1108TdDSR(DR)/DS Low to Read Data Required Valid1309ThDR(DS)Read Data to /DS High Hold5	ns	[1,2]
6TwDSR/DS (Read) Low Width1857TwDSWDS (Write) Low Width1108TdDSR(DR)/DS Low to Read Data Required Valid1309ThDR(DS)Read Data to /DS High Hold5	ns	[2]
7TwDSWDS (Write) Low Width1108TdDSR(DR)/DS Low to Read Data Required Valid1309ThDR(DS)Read Data to /DS High Hold5	ns	[2]
8TdDSR(DR)/DS Low to Read Data Required Valid1309ThDR(DS)Read Data to /DS High Hold5	ns	[1,2]
9 ThDR(DS) Read Data to /DS High Hold 5	ns	[1,2]
	ns	[1,2]
	ns	
10 TdDS(A) /DS High to Address Active Delay 55	ns	[2]
11 TdDS(AS) /DS High to /AS Low Delay 55	ns	[2]
12 TdR/W(AS) R//W Valid to /AS High Delay 35	ns	[2]
13 TdDS(R/W) /DS High to R//W Not Valid 55	ns	[2]
14 TdDW(DSW) Write Data Valid to /DS Low Delay 35	ns	[2]
15 TdDS(DW) /DS High to Write Data Not Valid 55	ns	[2]
16TdA(DR)Address Valid to Read Data Required Valid330	ns	[1,2]
17 TdAS(DS) /AS High to /DS Low Delay 65	ns	[2]
18 TdDI(DS) Data Input Setup to /DS High 75	ns	[1]

Notes:

[1] When using extended memory timing, for parameters 3, 6, 7, 8, and 16, add 2 TpC (250 ns @ 4.0 MHz).

[2] Min and Max times are in nanoseconds unless otherwise noted.

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